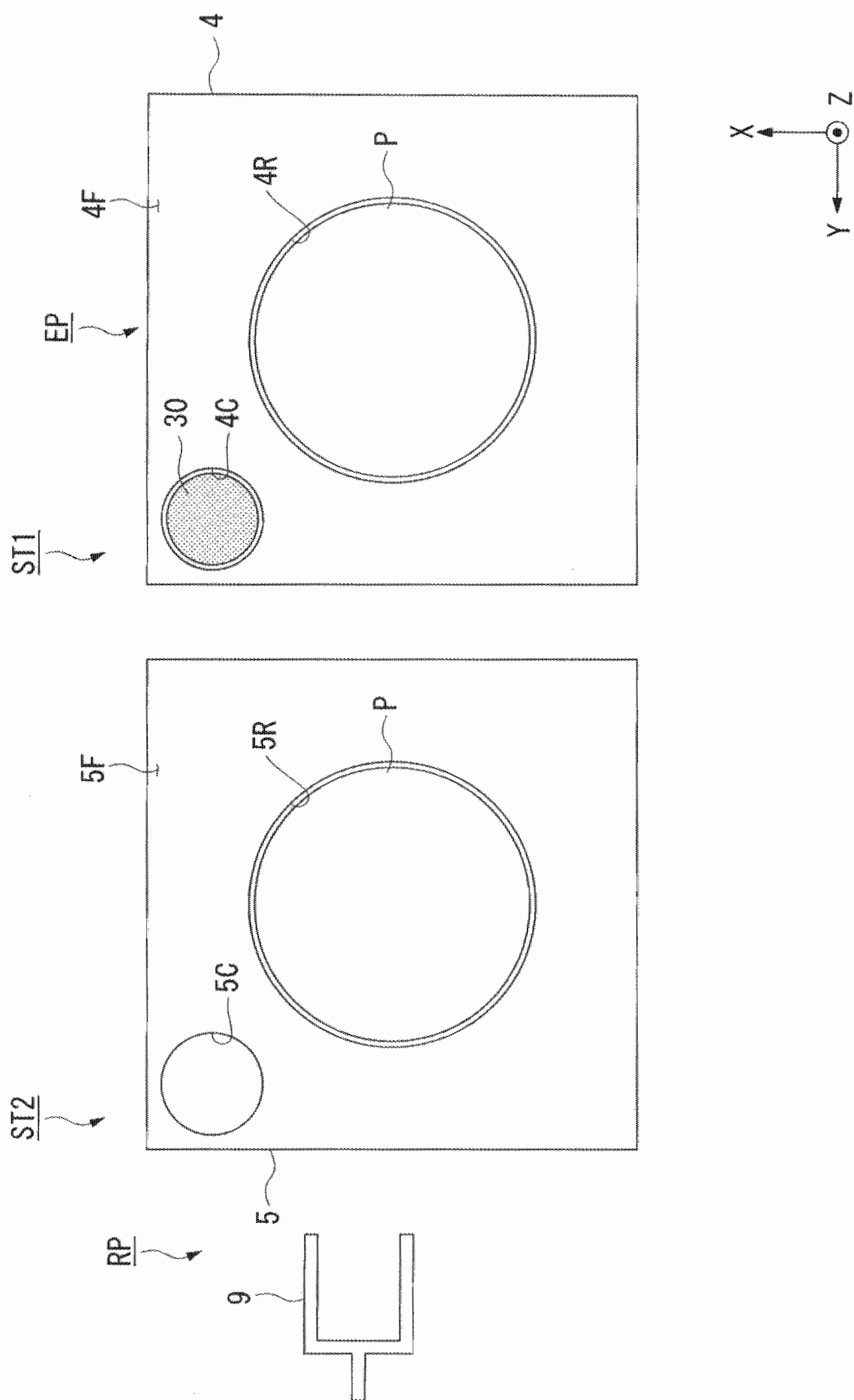


FIG. 2



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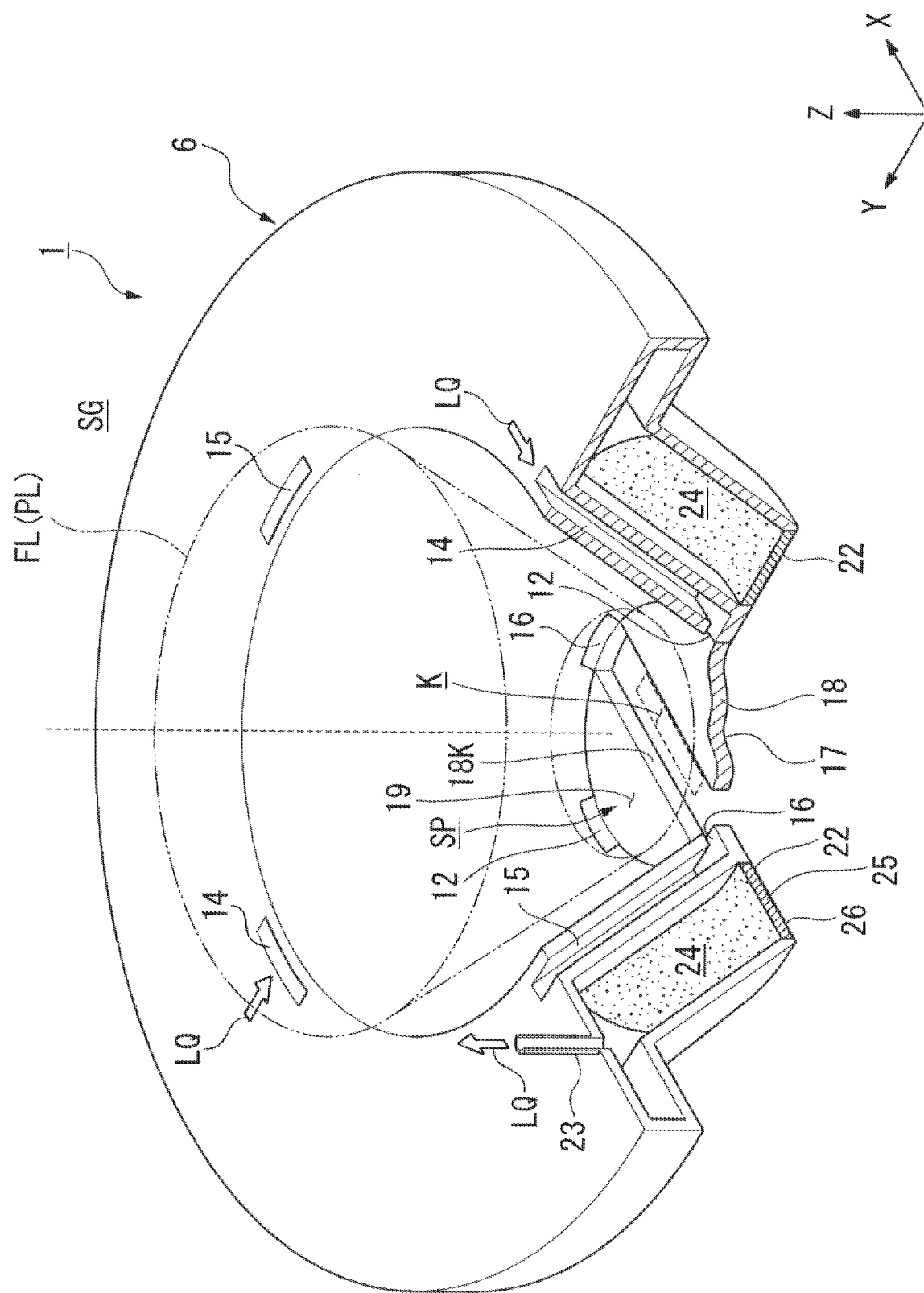


FIG. 4

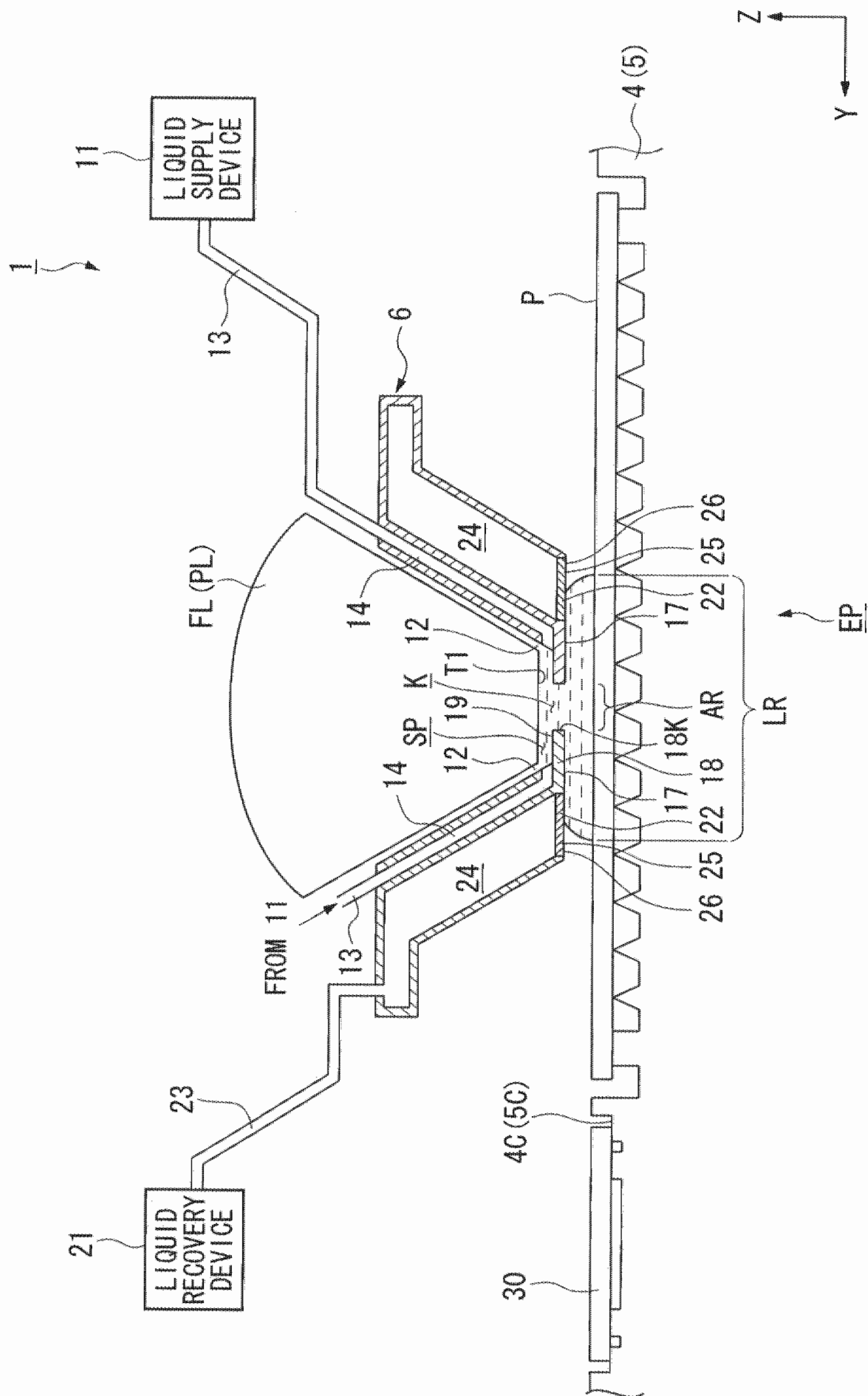


FIG. 5

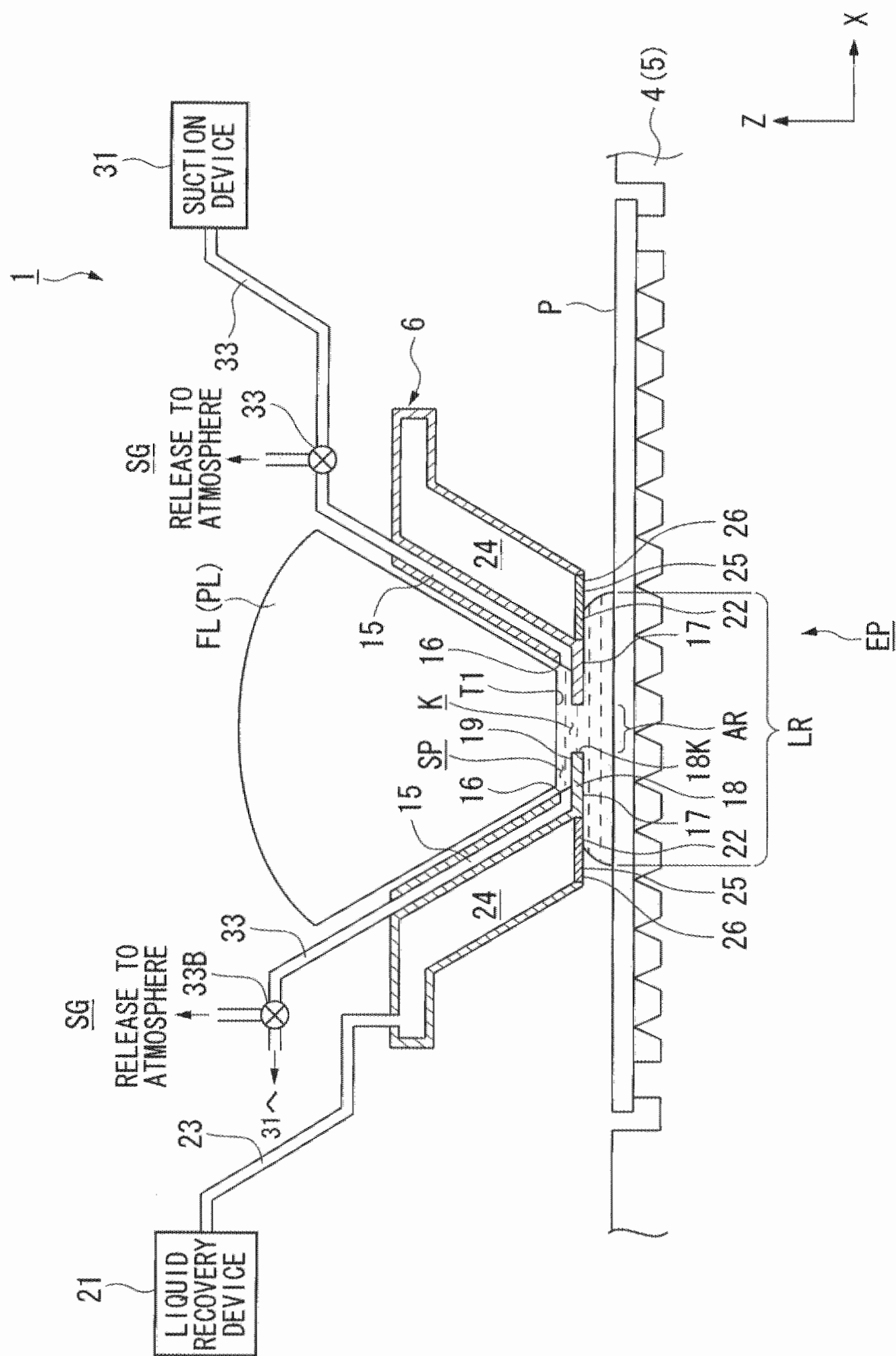


FIG. 6

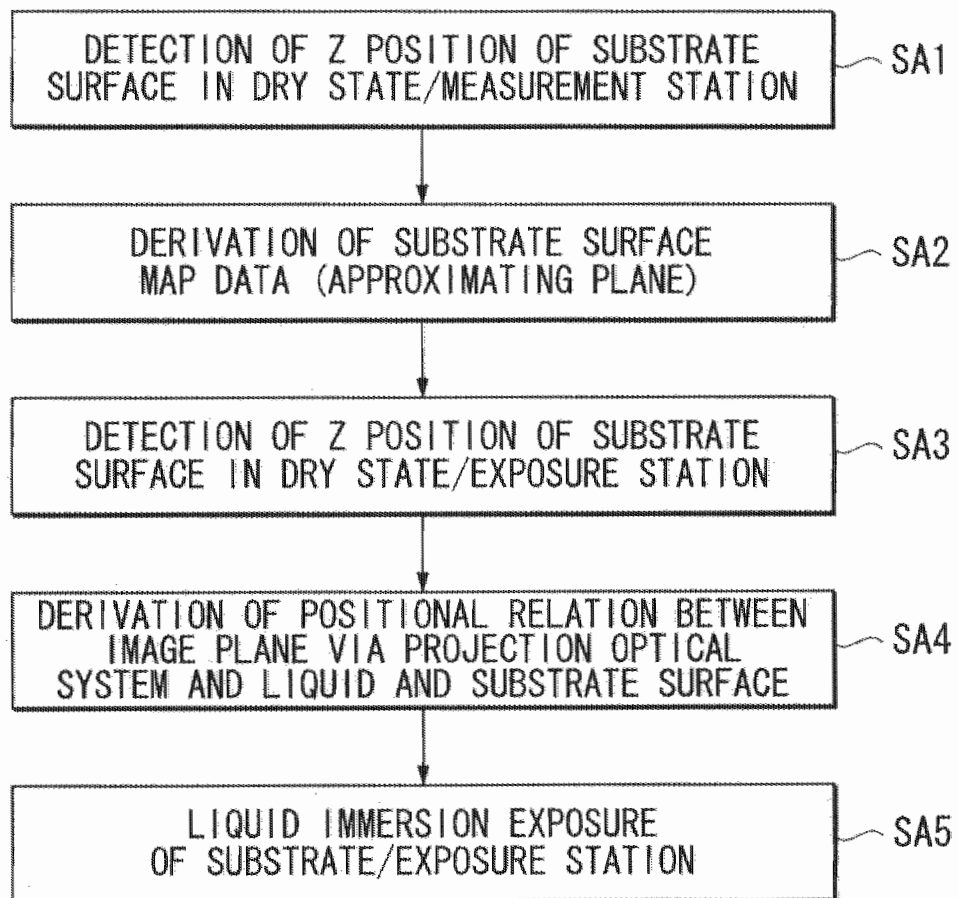


FIG. 7

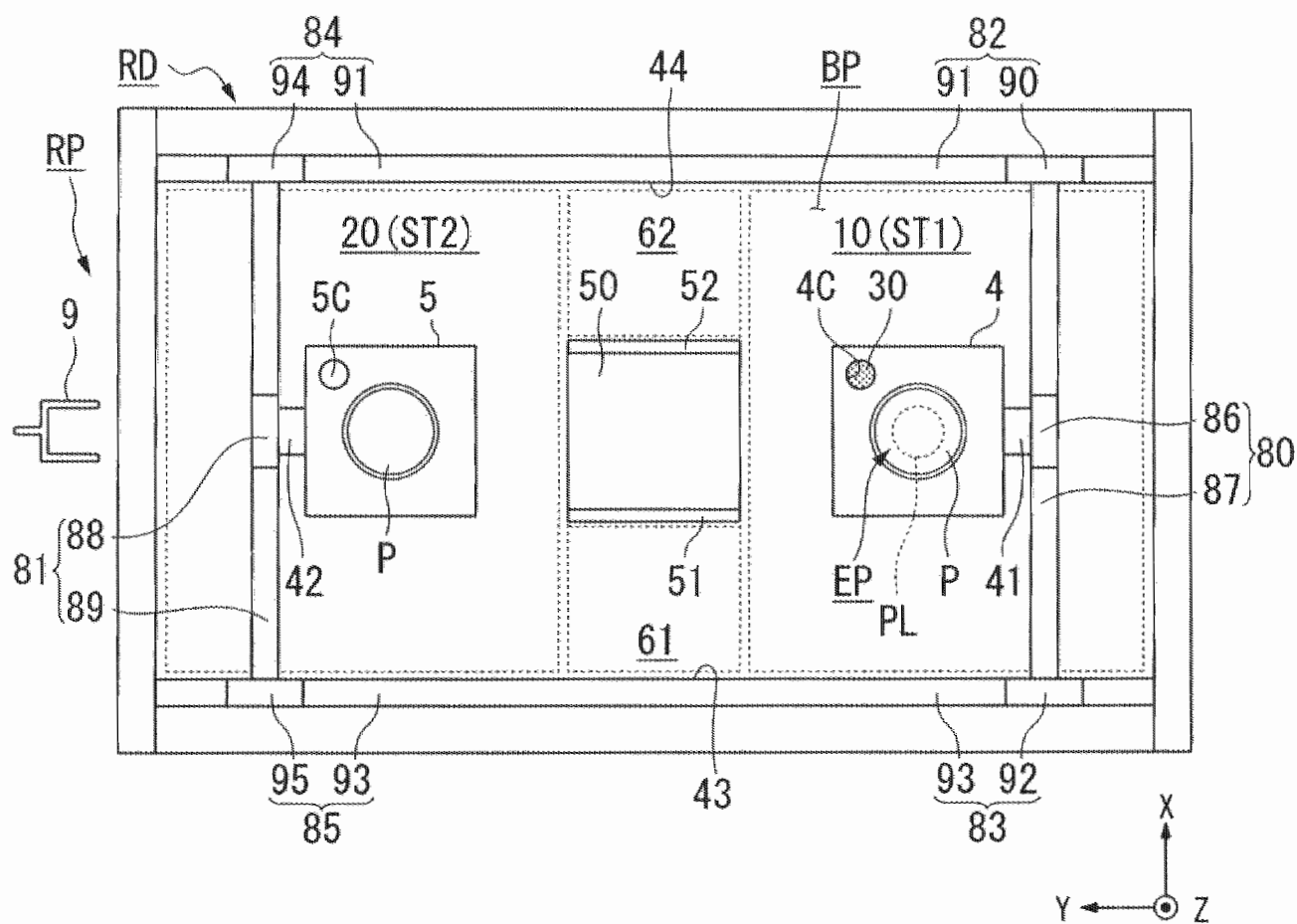


FIG. 8

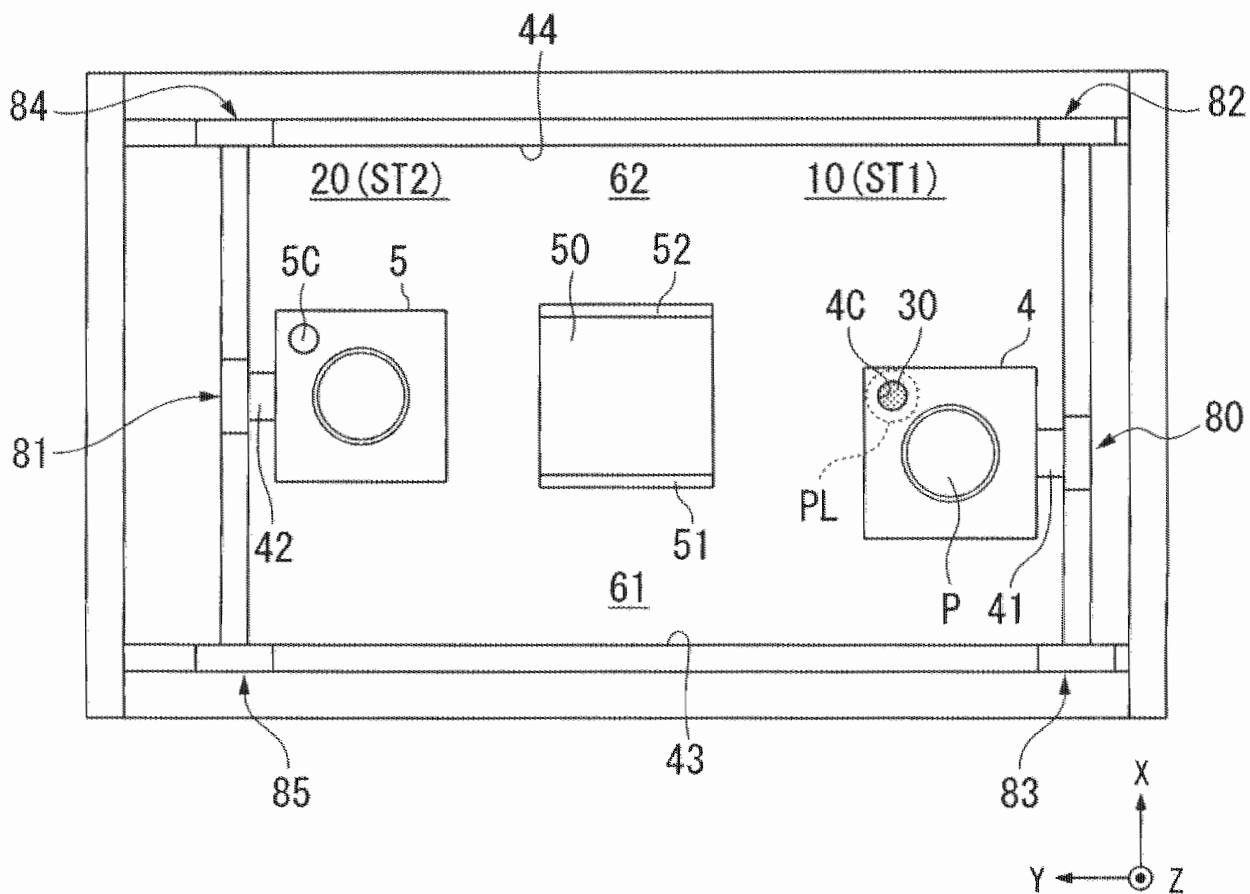


FIG. 9

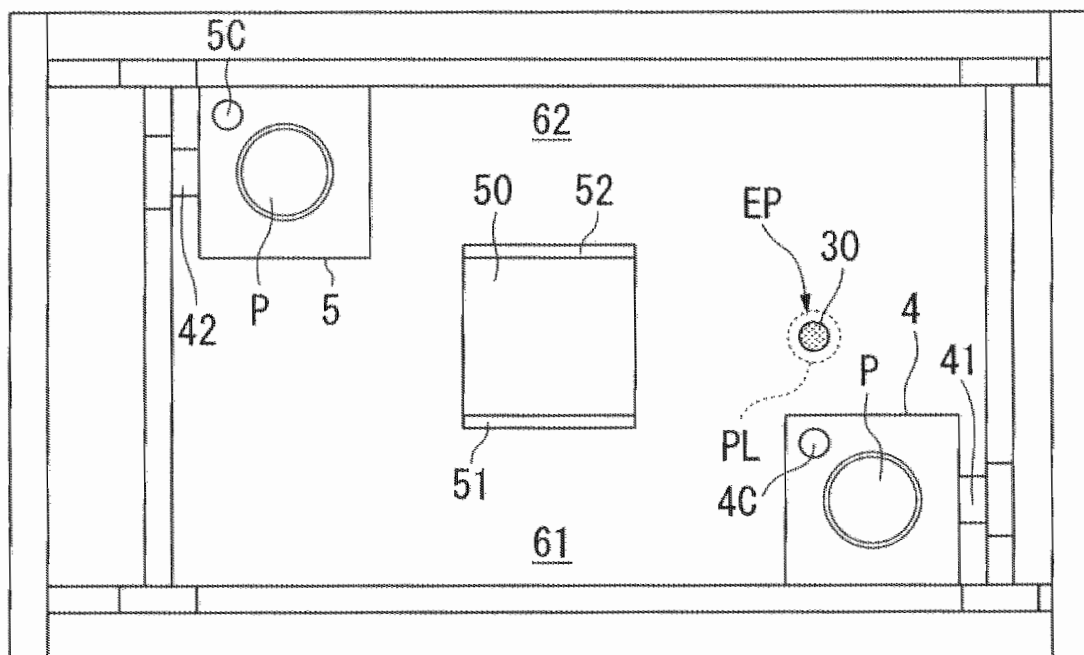


FIG. 10

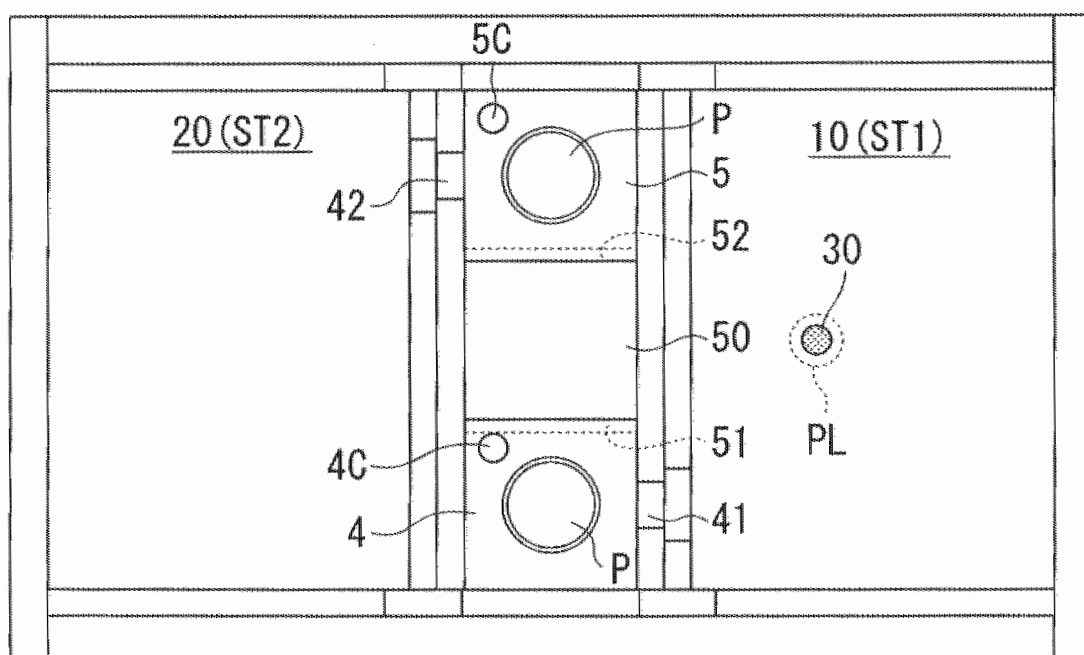


FIG. 11

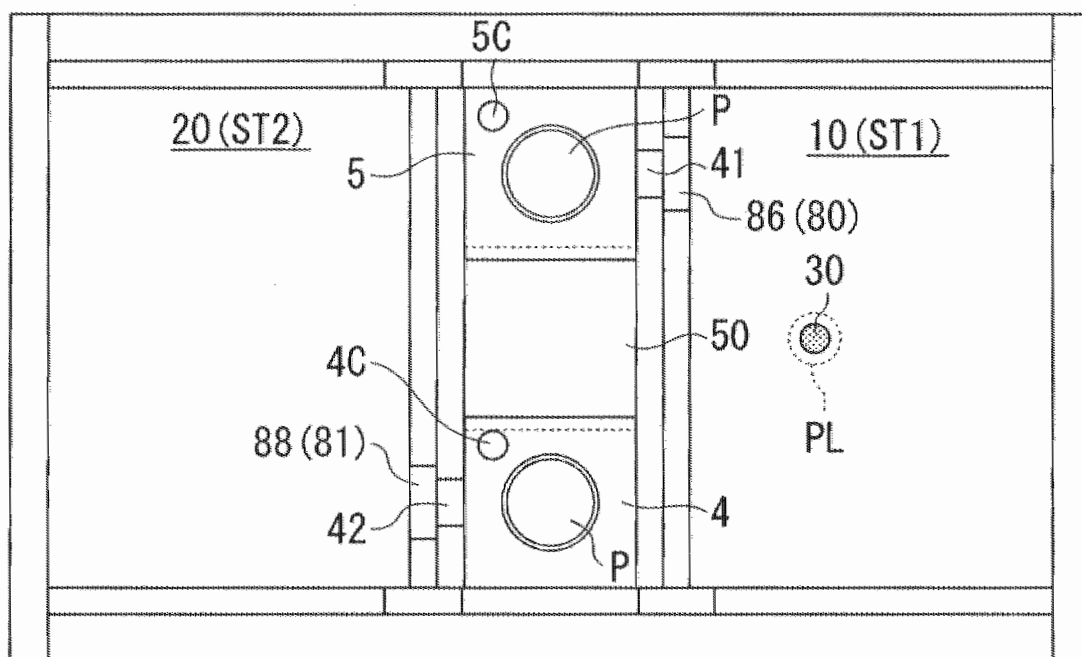


FIG. 12

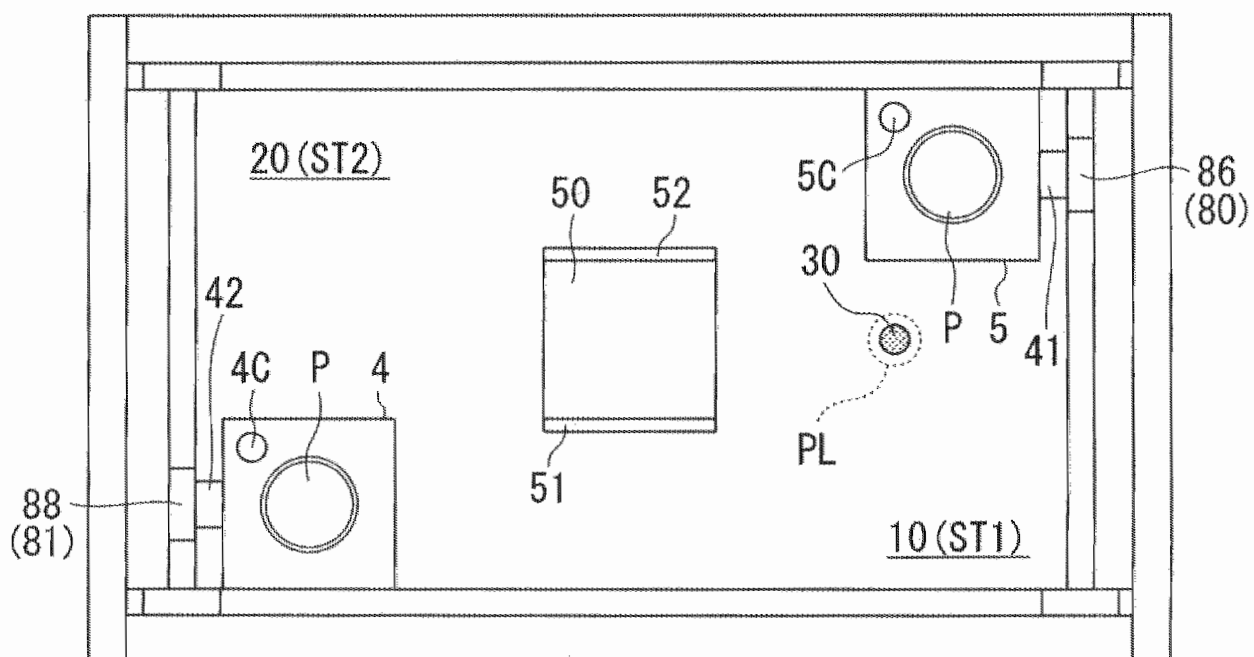


FIG. 13

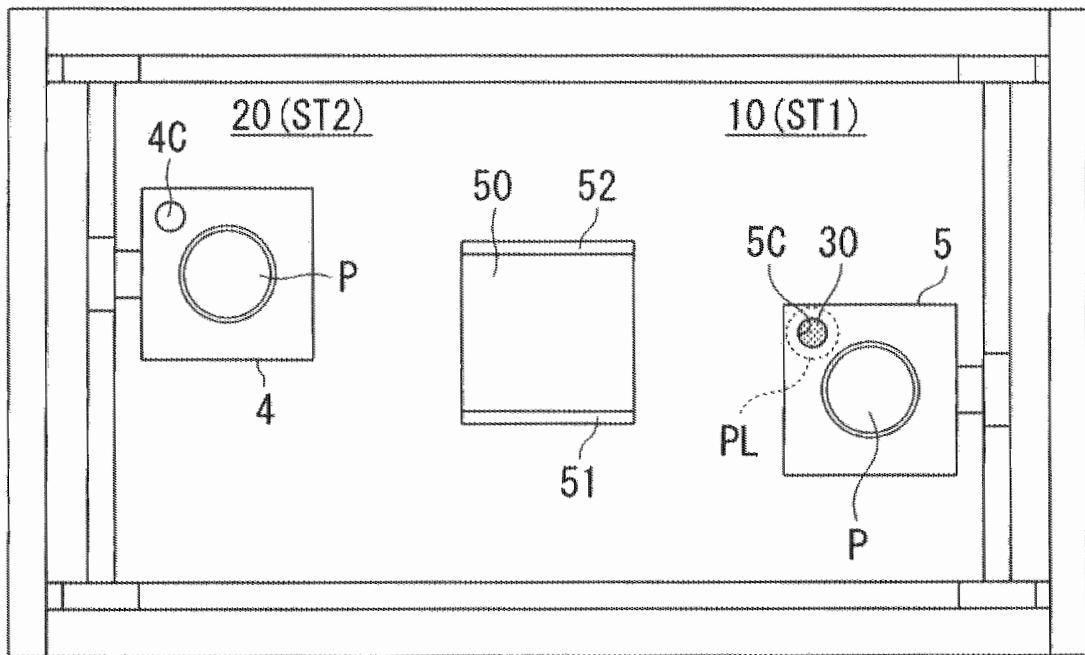


FIG. 14

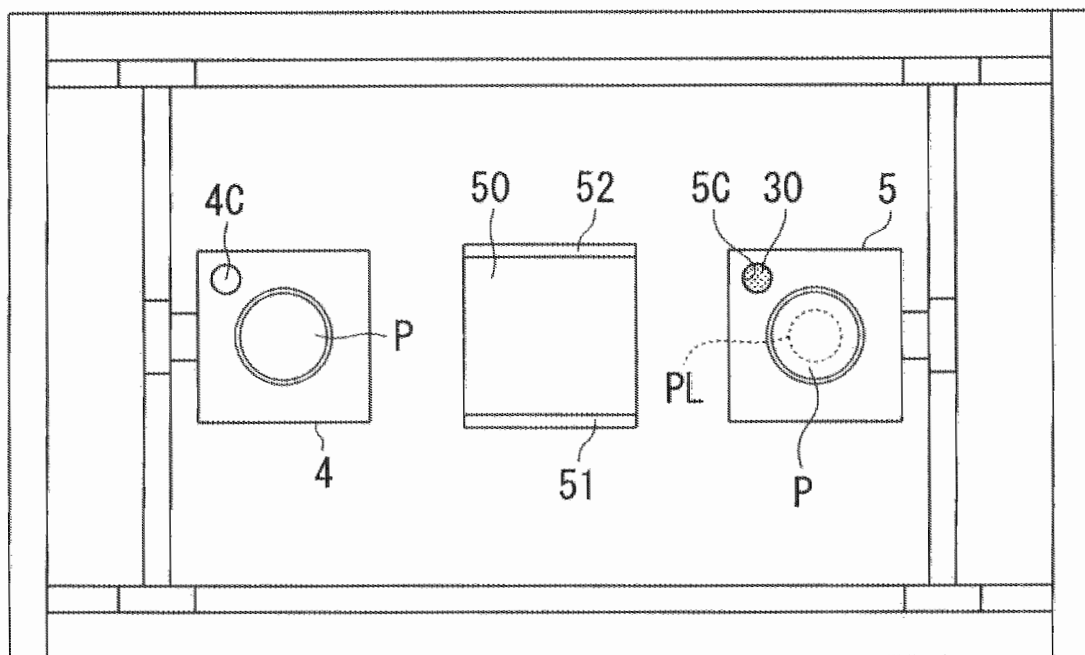


FIG. 15

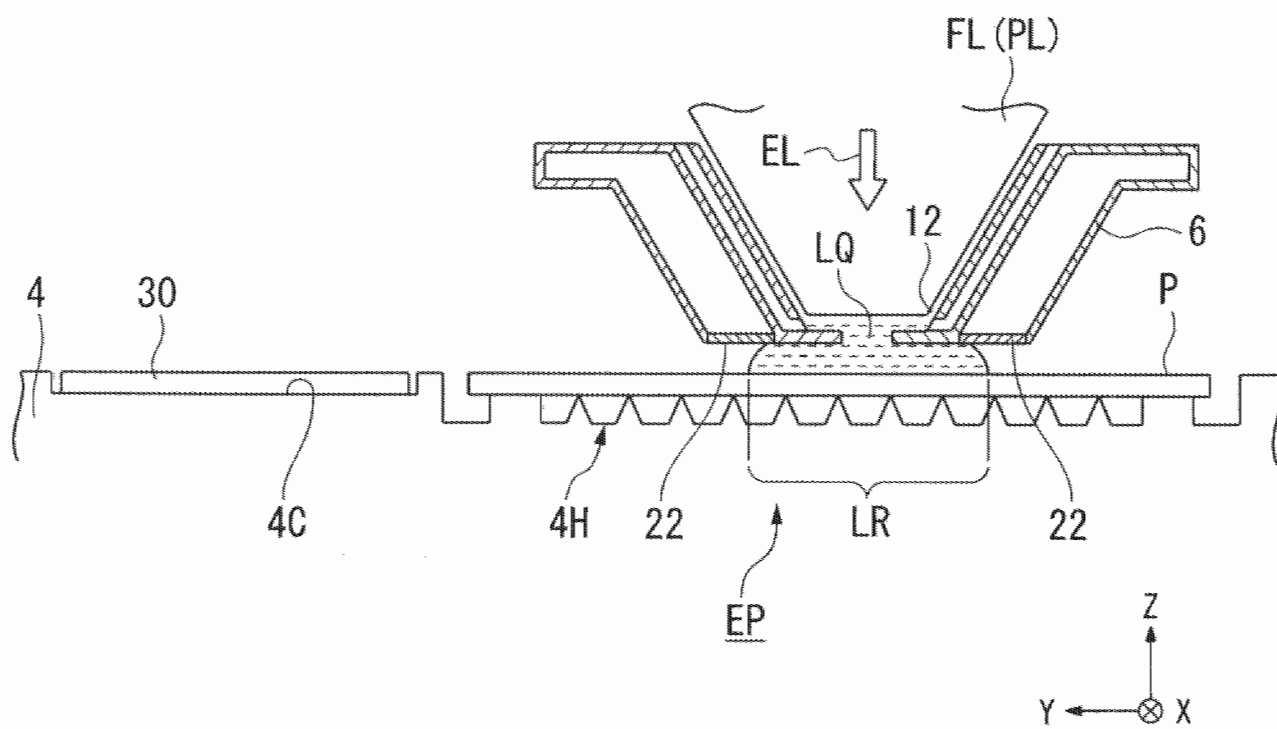


FIG. 16

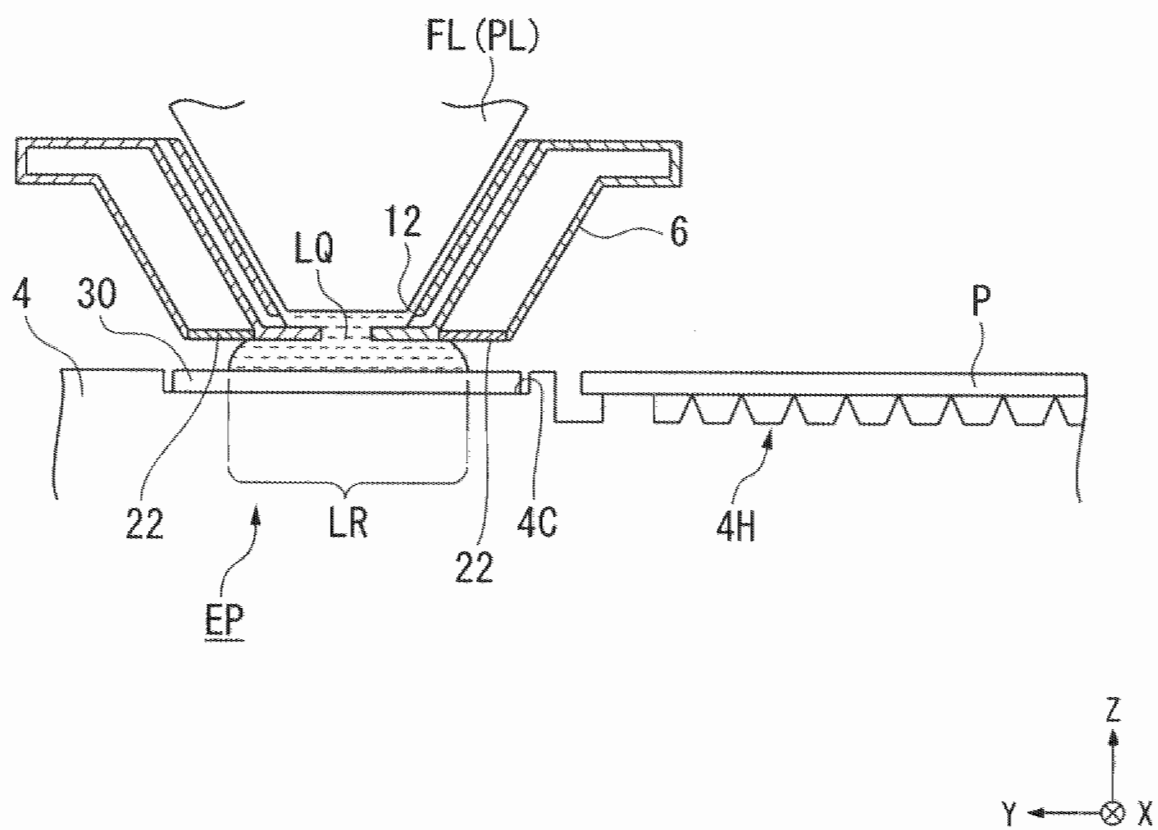


FIG. 17

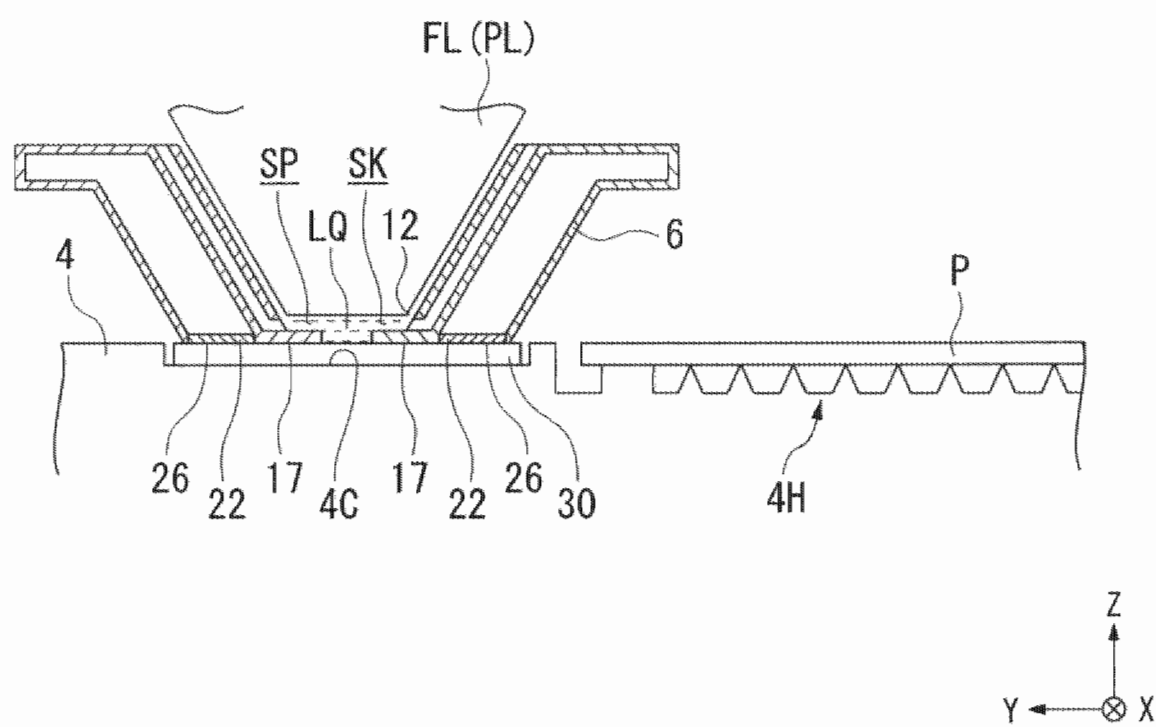


FIG. 18

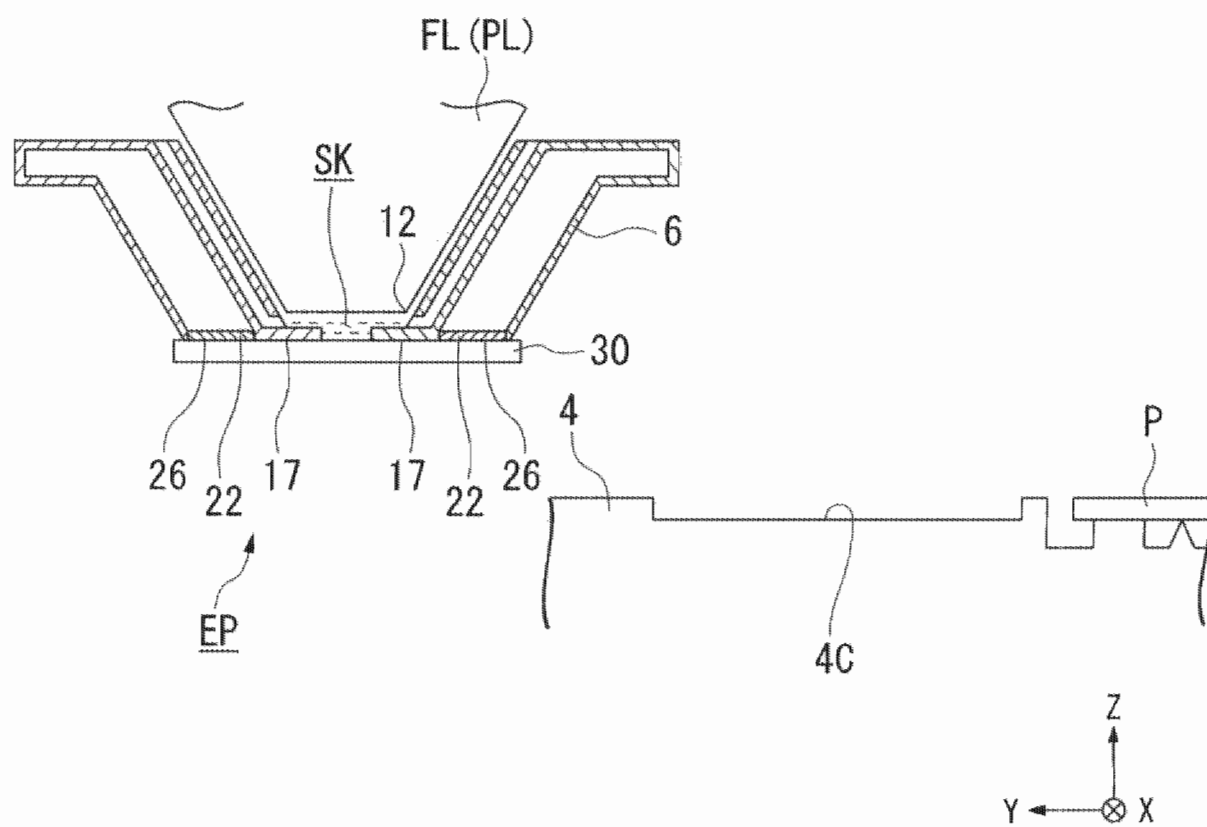


FIG. 9.

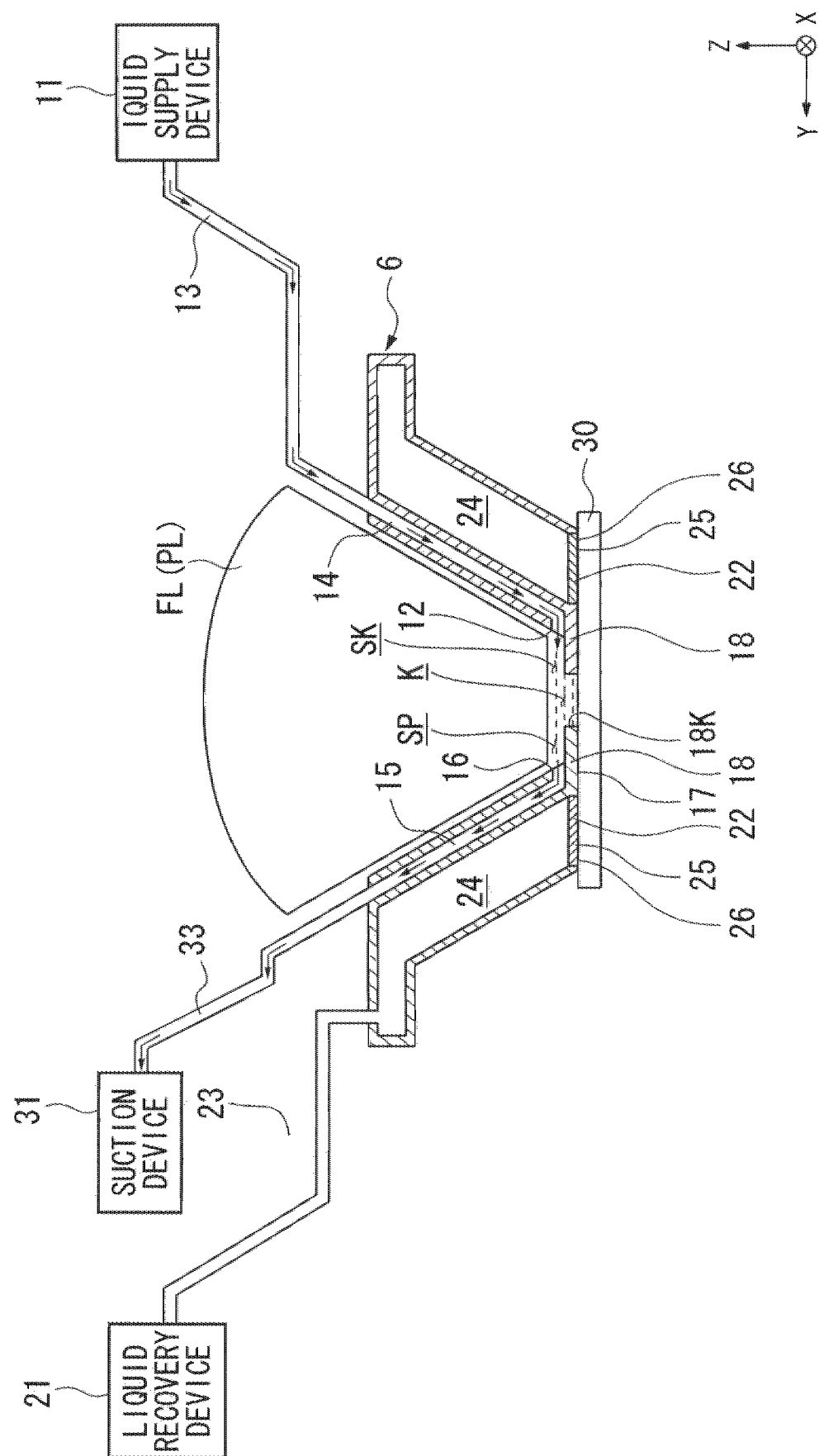


FIG. 20

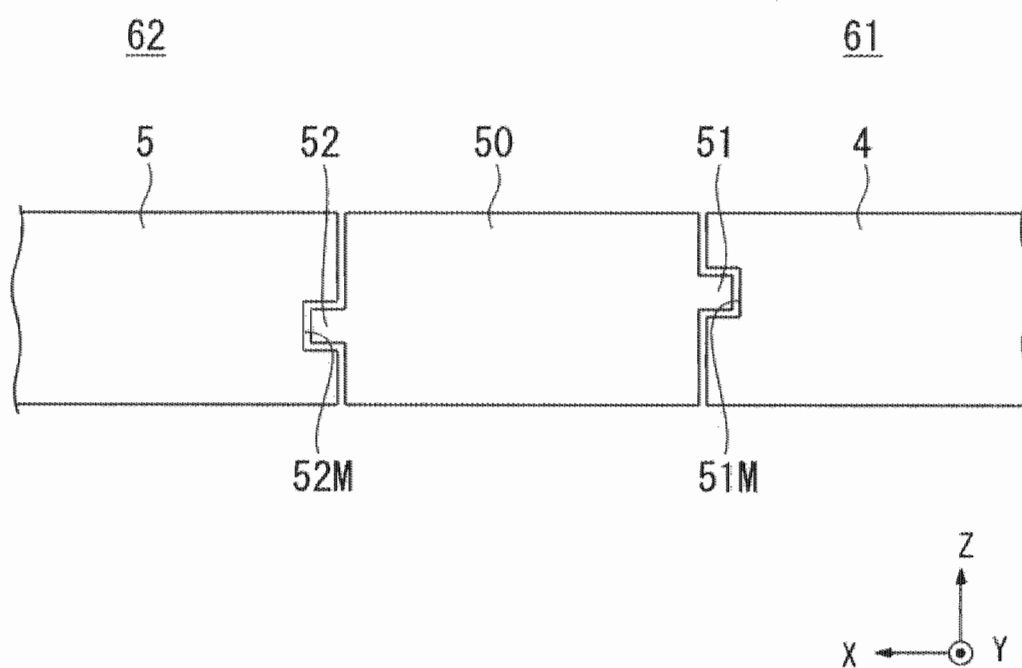


FIG. 21

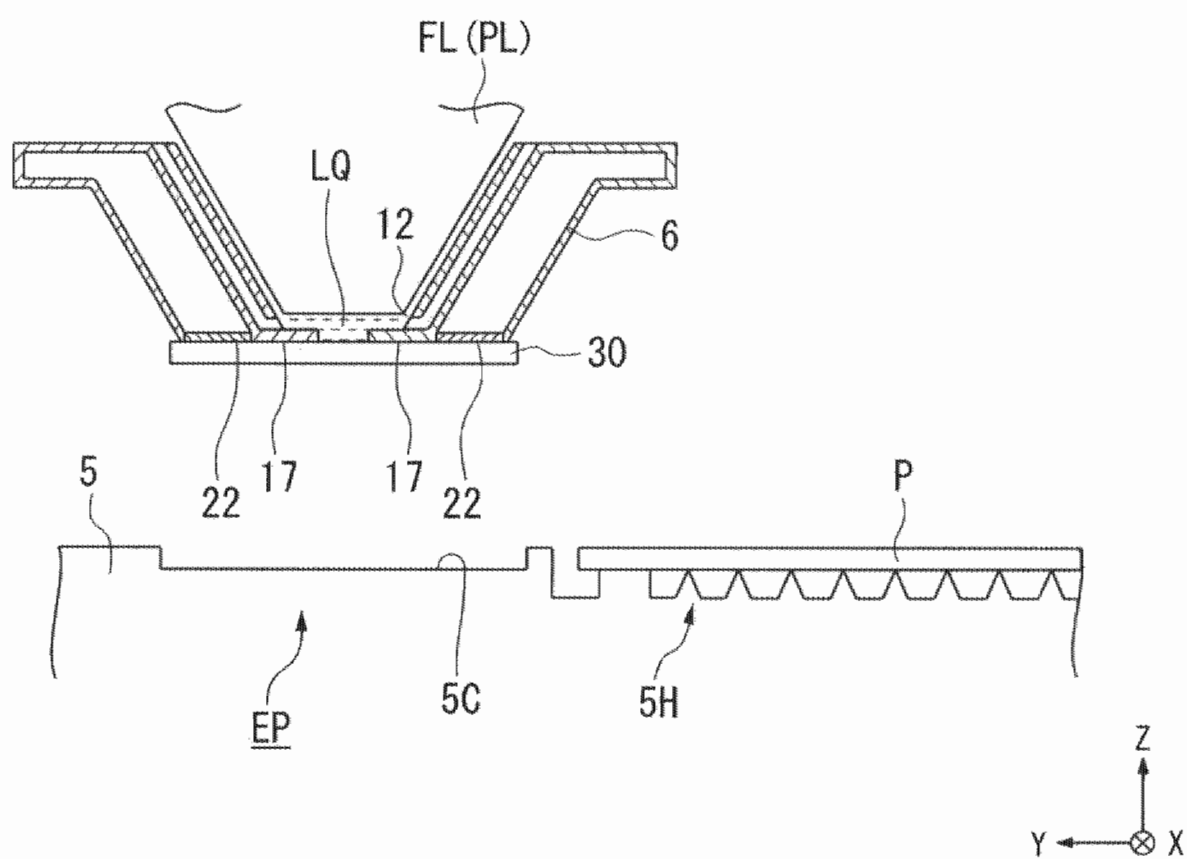
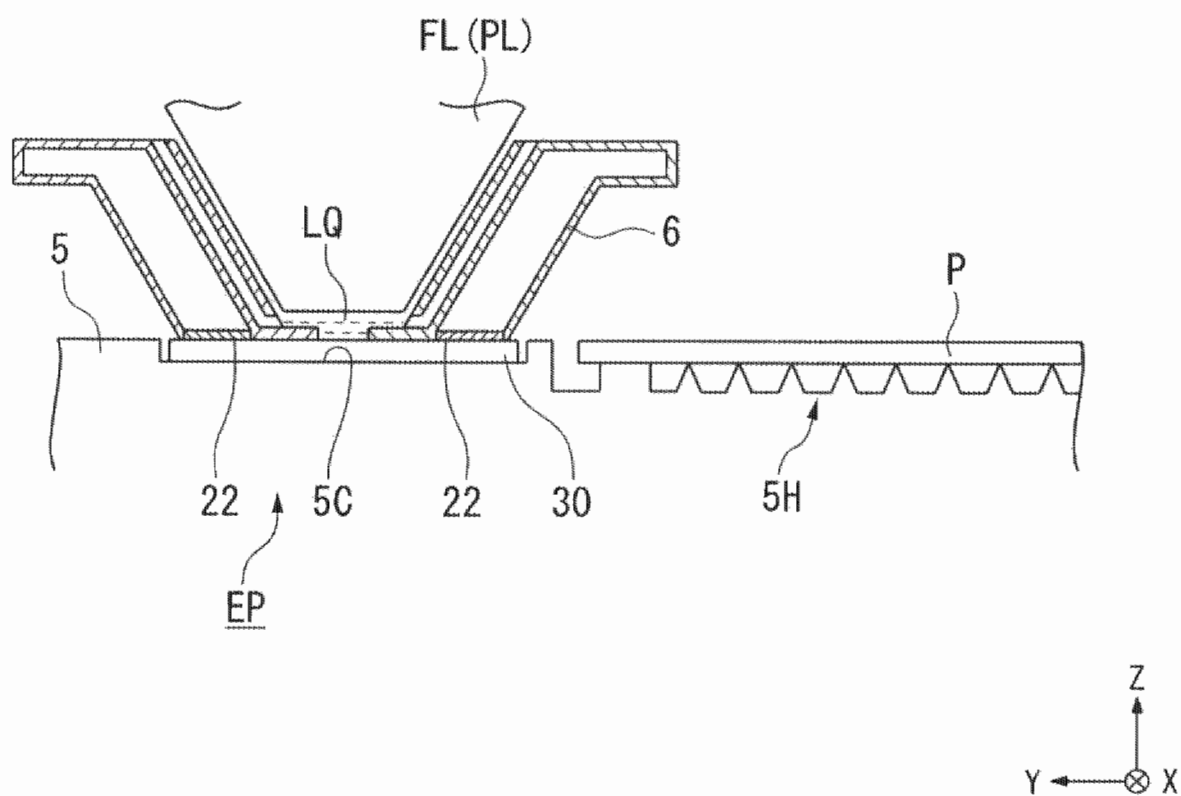


FIG. 22



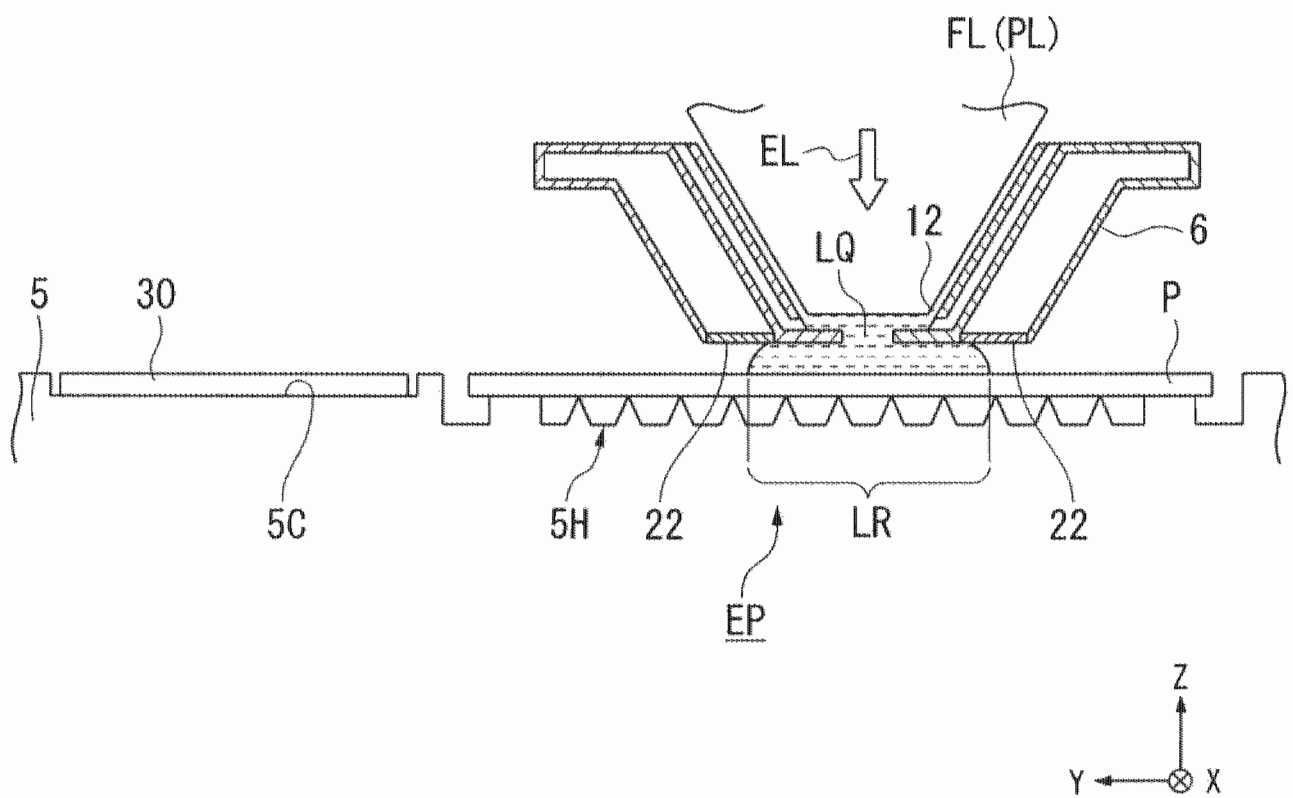


FIG. 25A

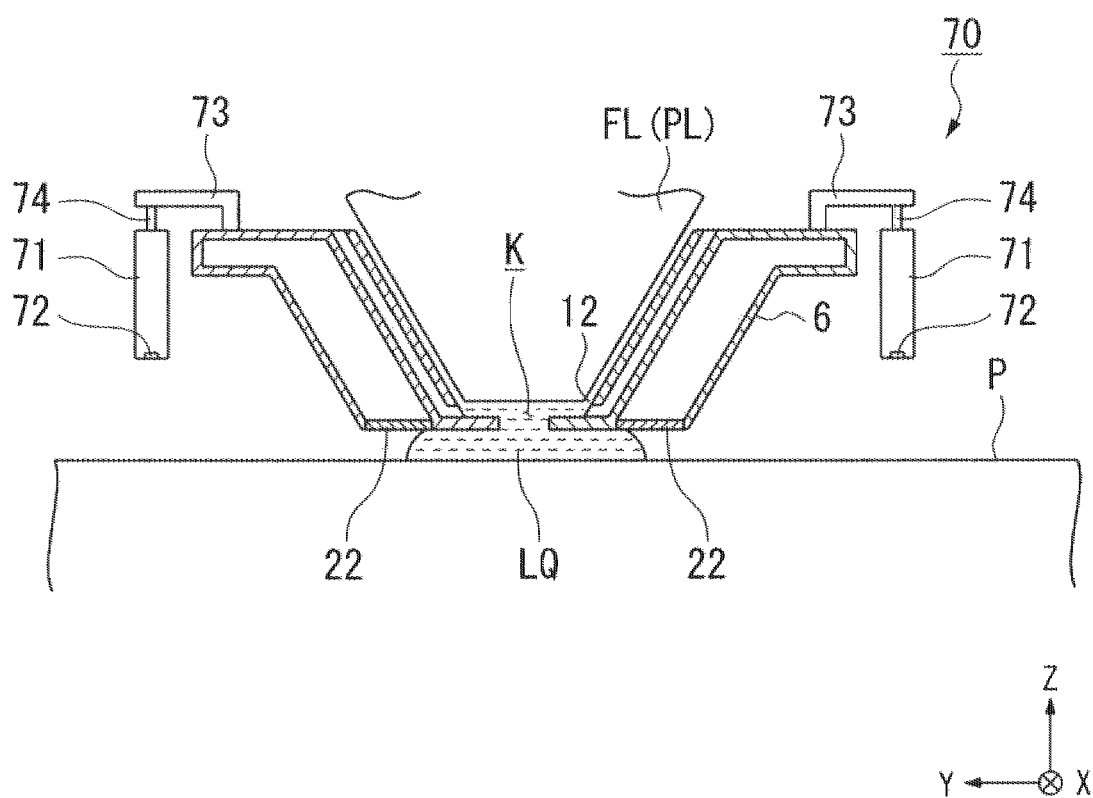


FIG. 25B

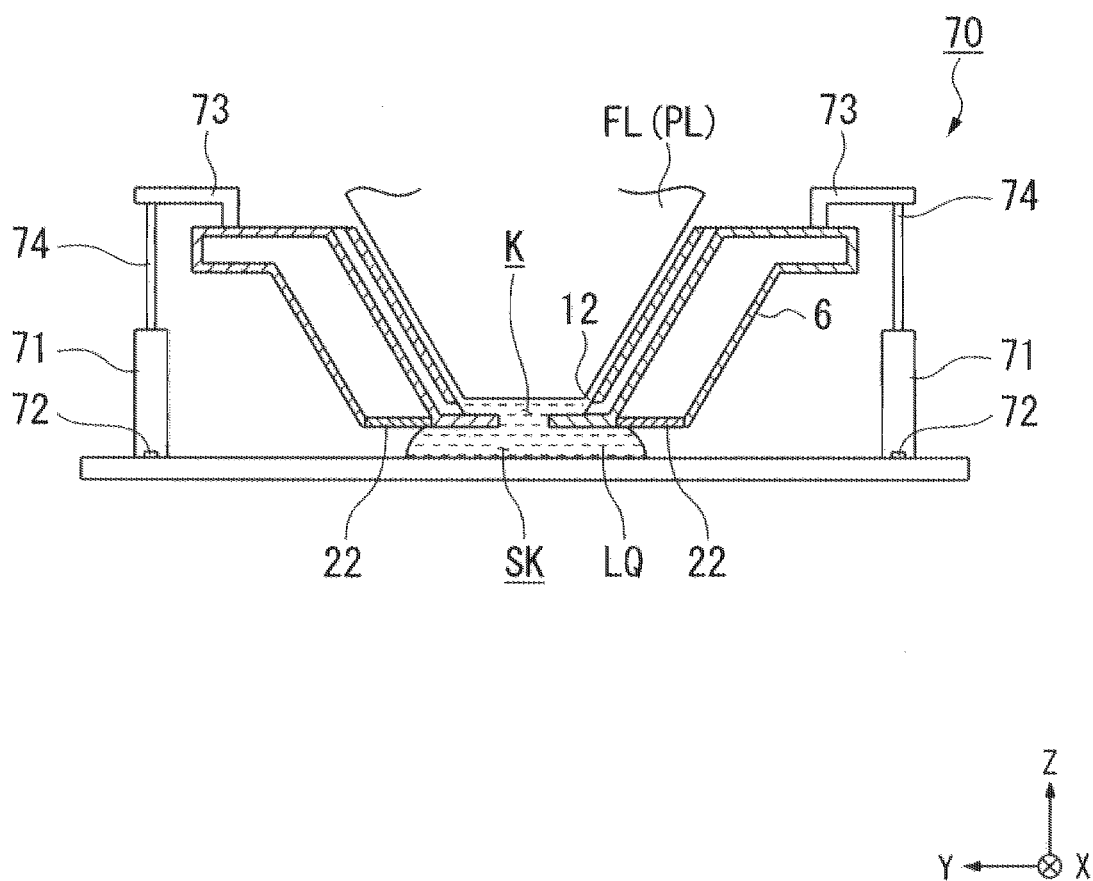


FIG. 26

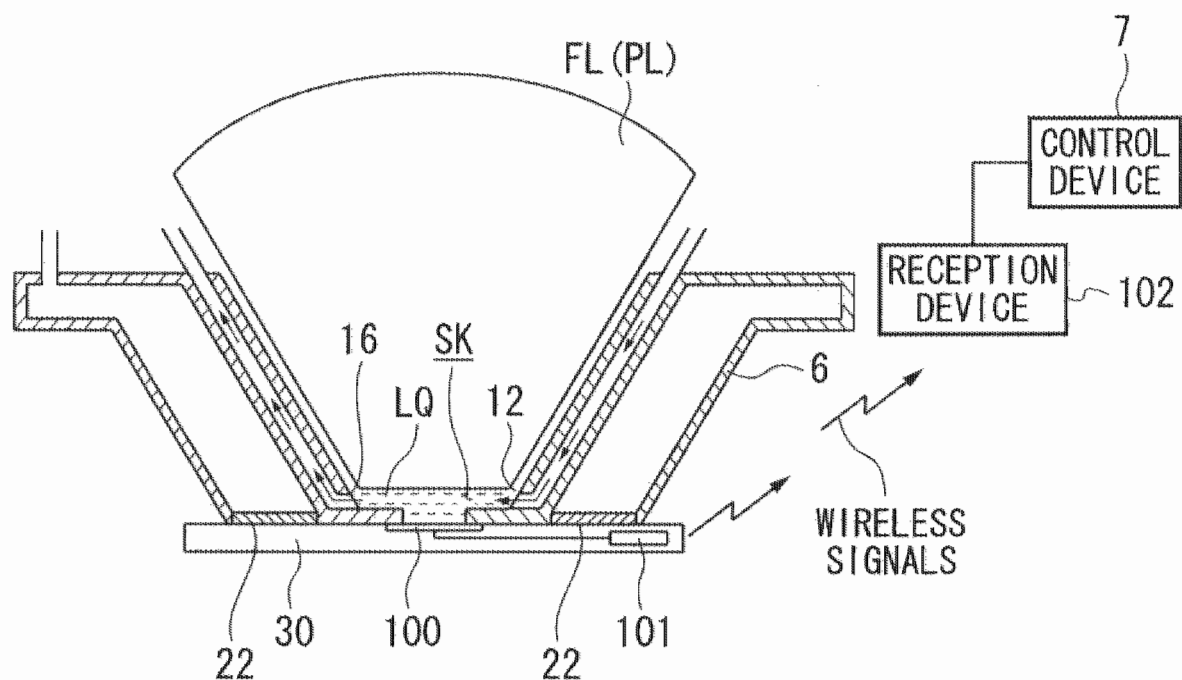


FIG. 27

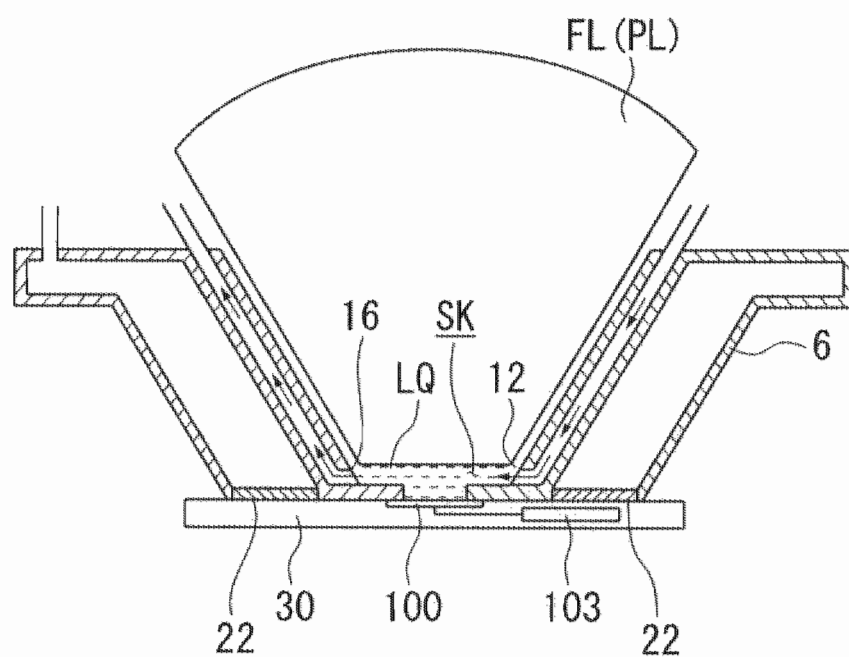


FIG. 28

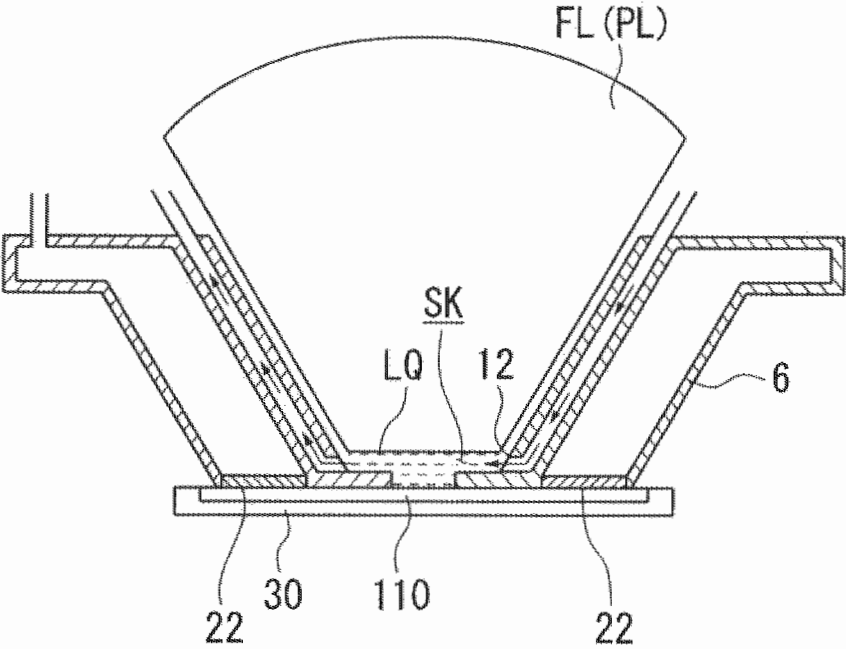


FIG. 29

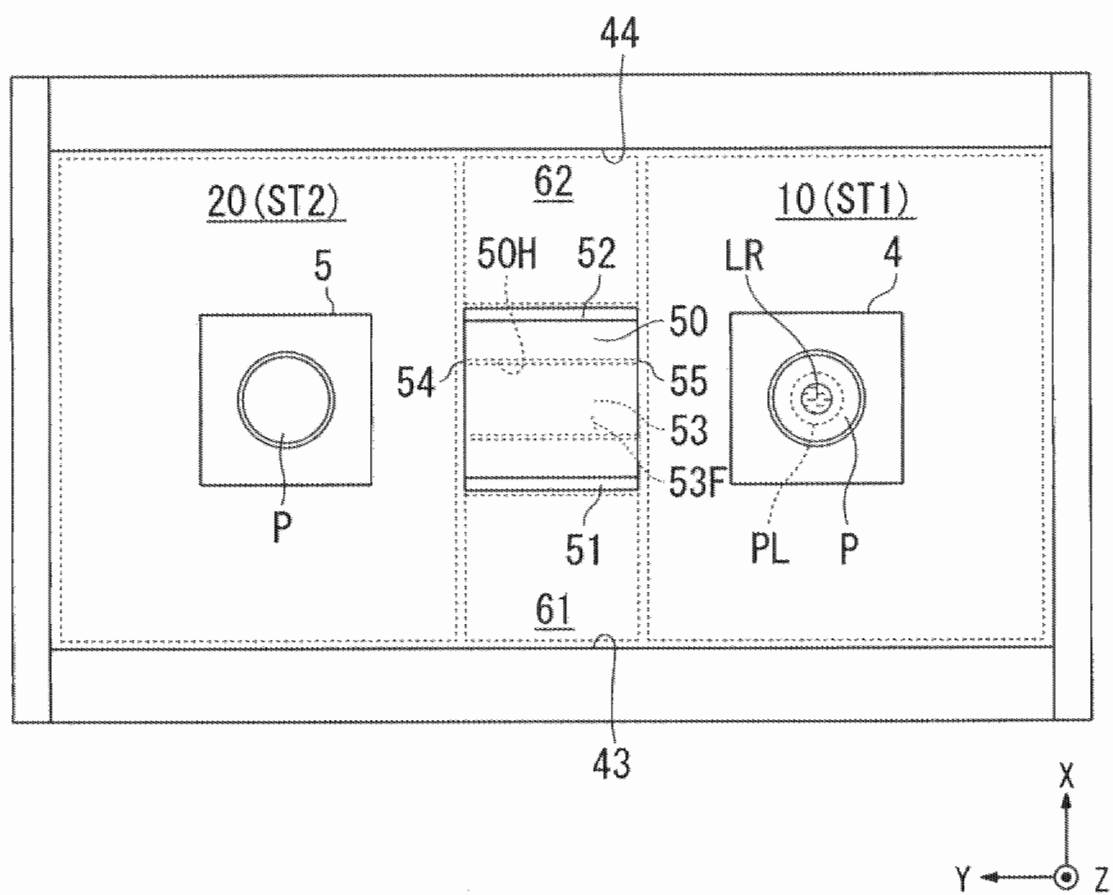


FIG. 30

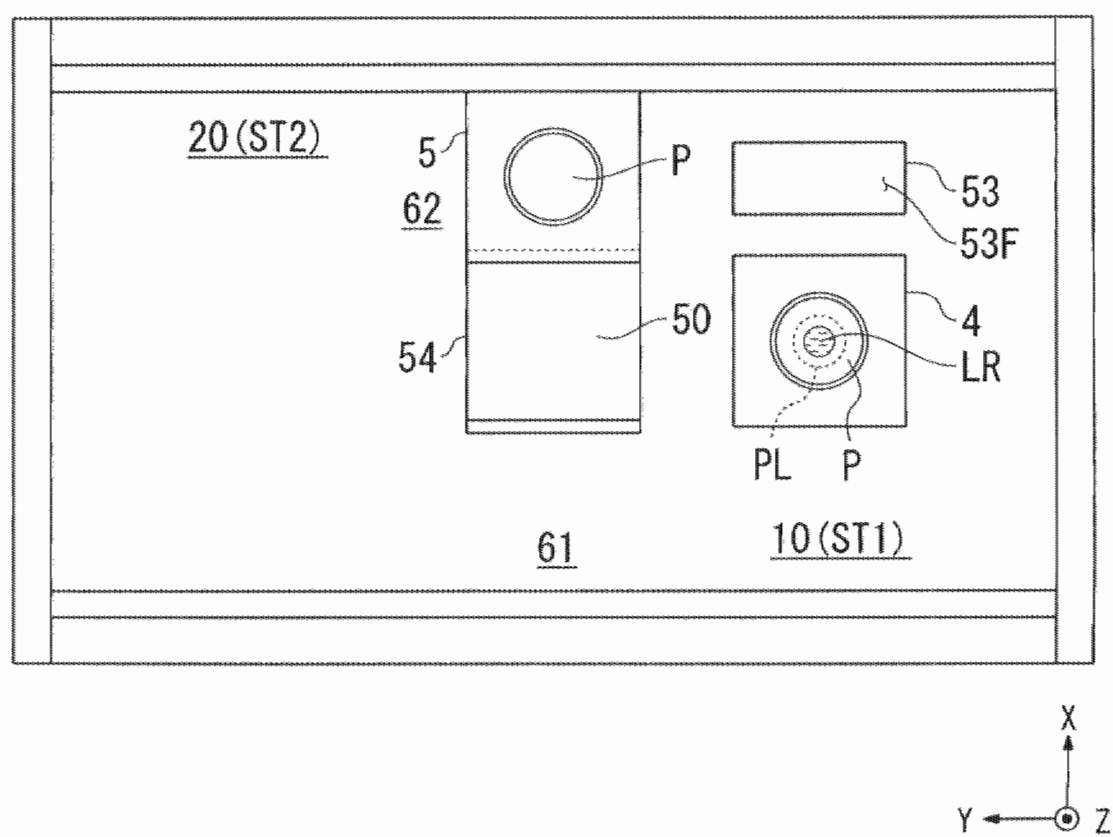


FIG. 31

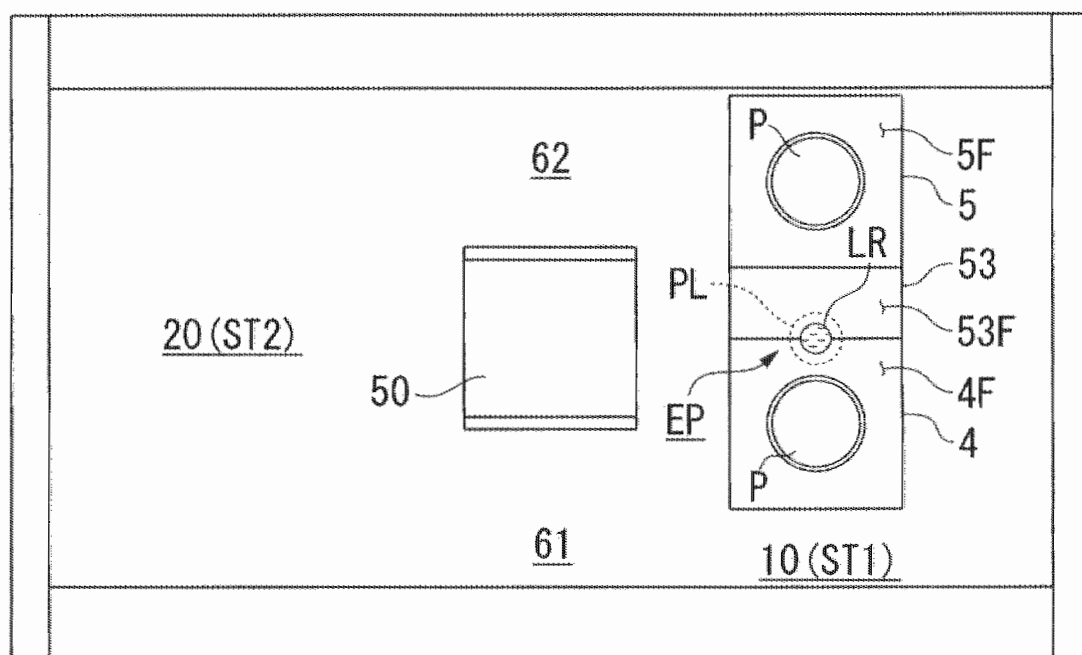


FIG. 32

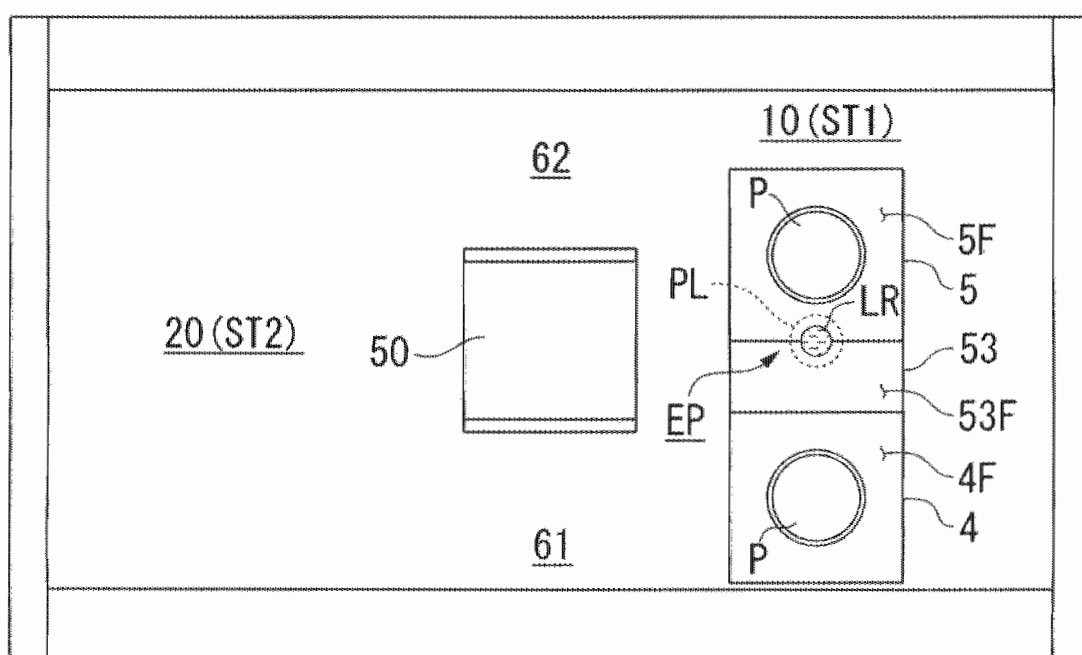


FIG. 33

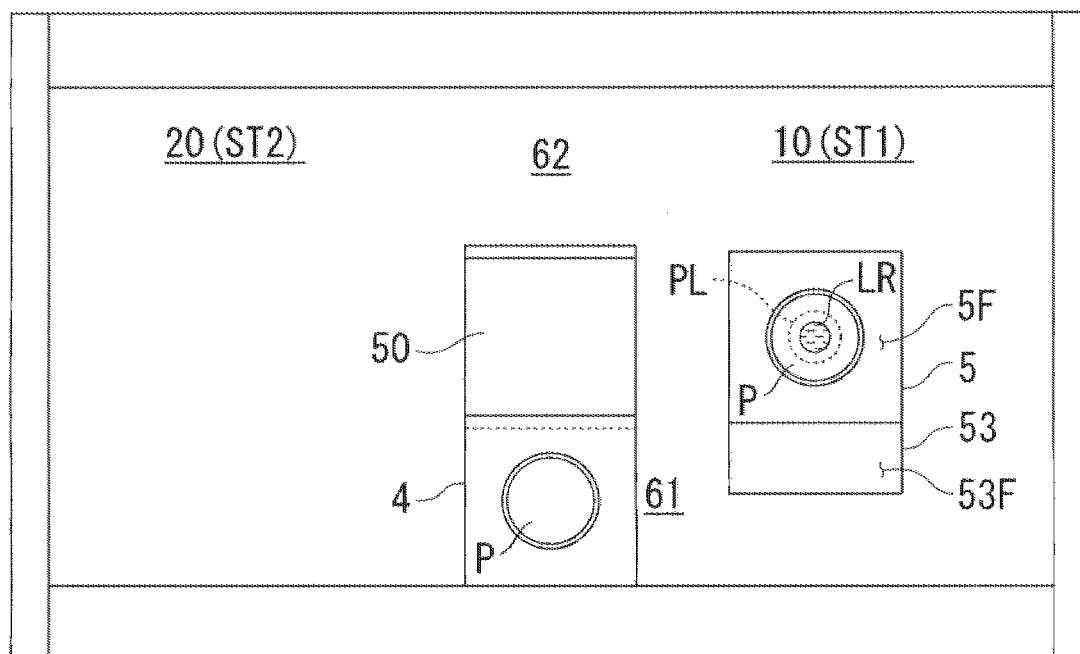


FIG. 34

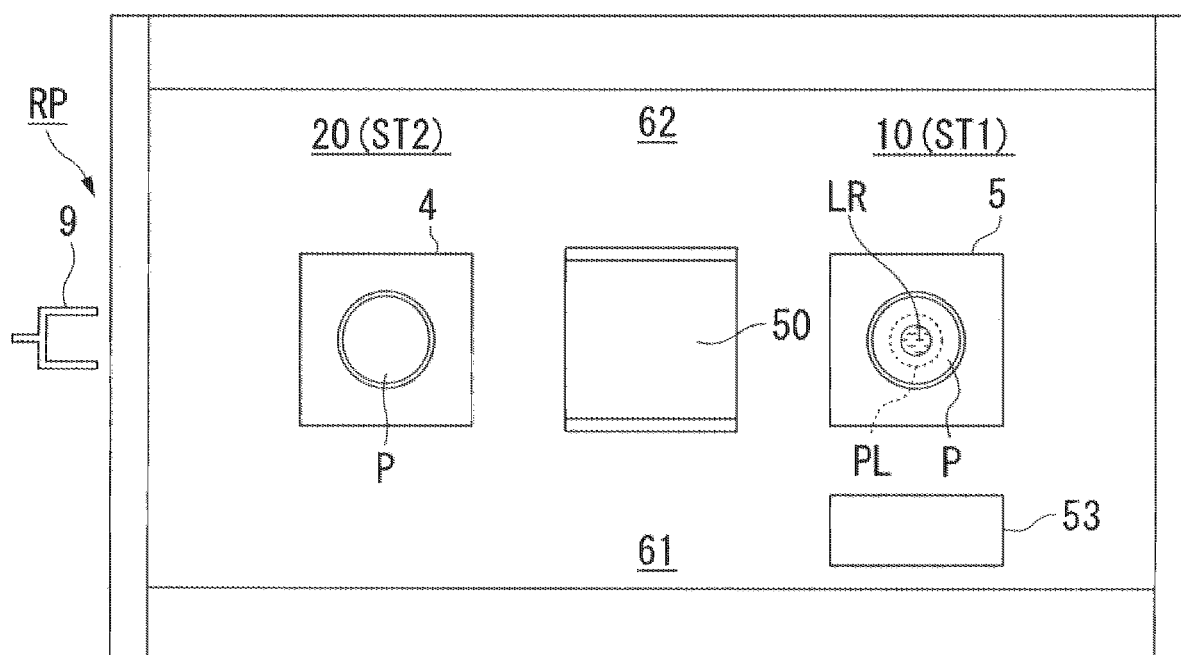


FIG. 35

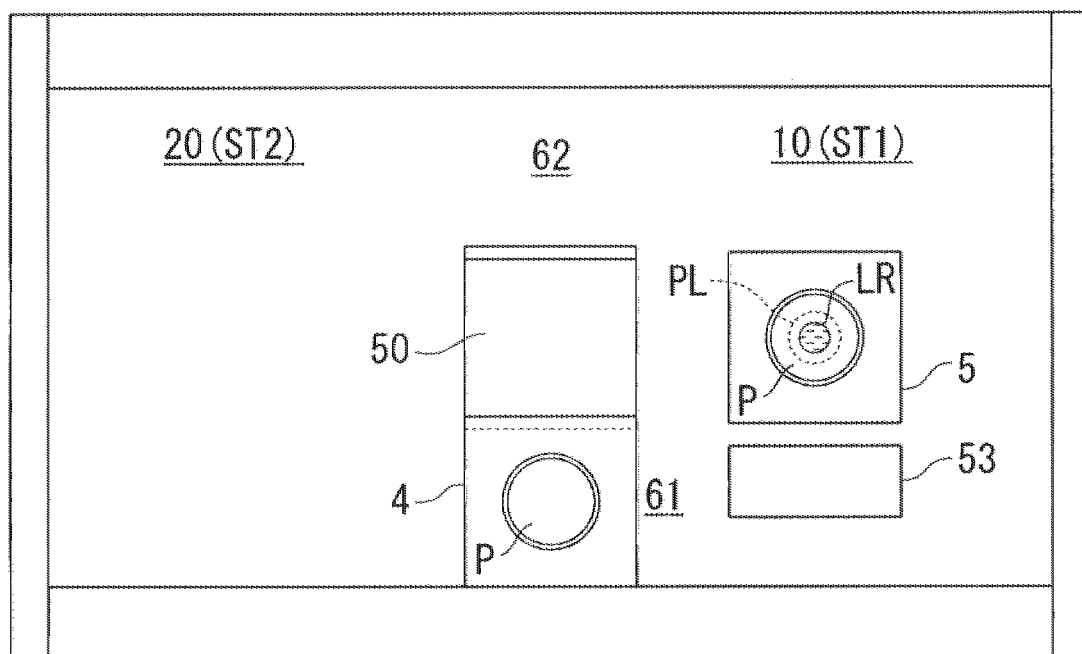


FIG. 36

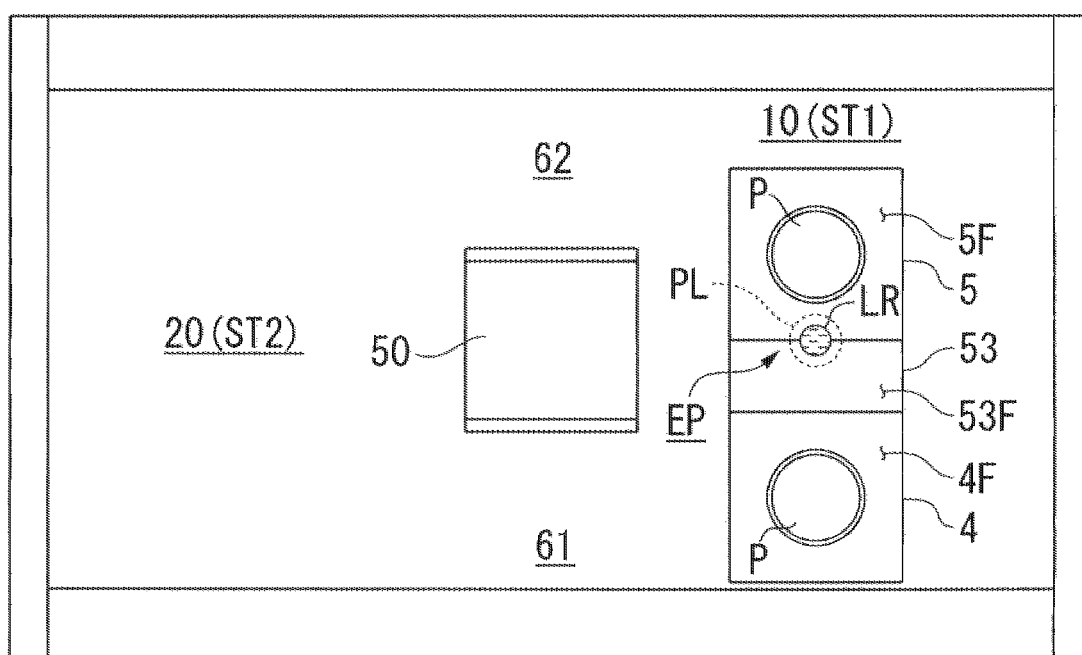


FIG. 37

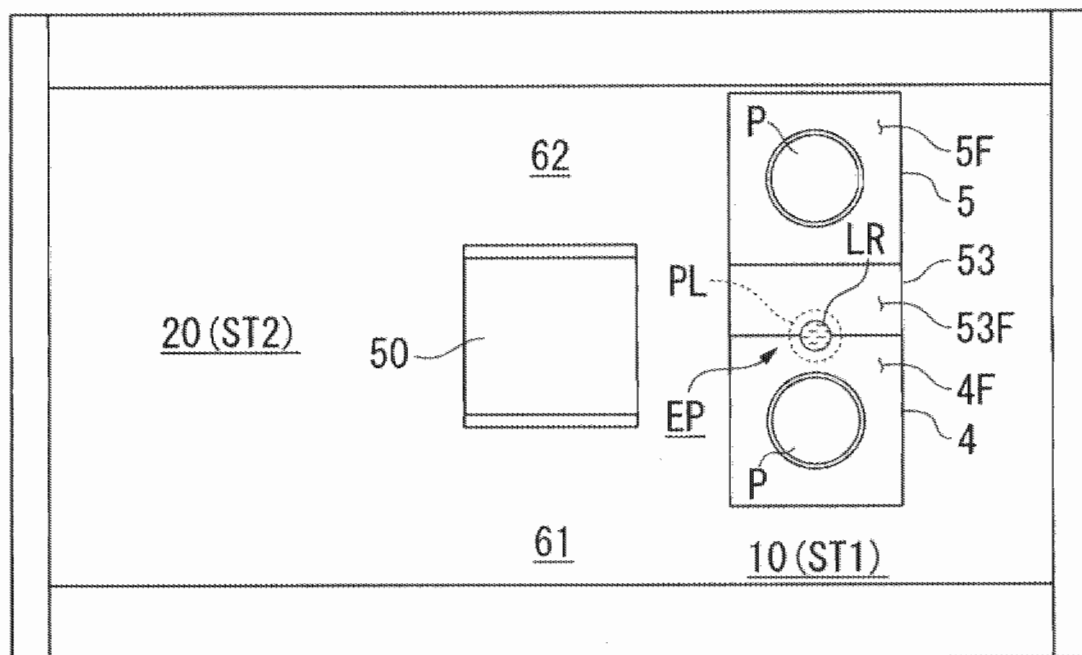


FIG. 38

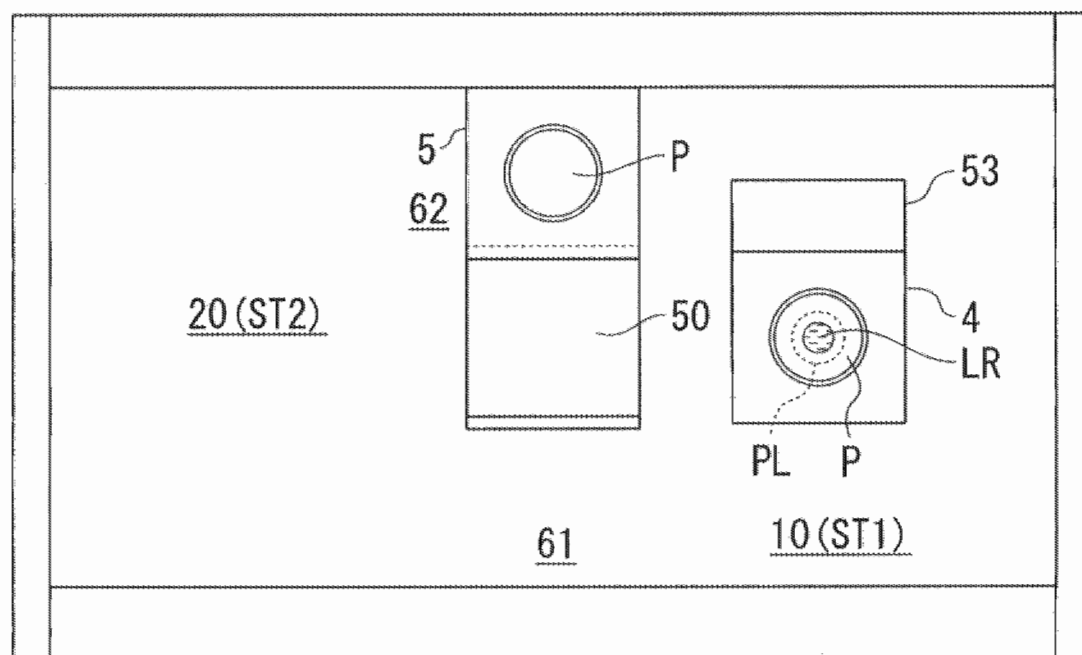


FIG. 39

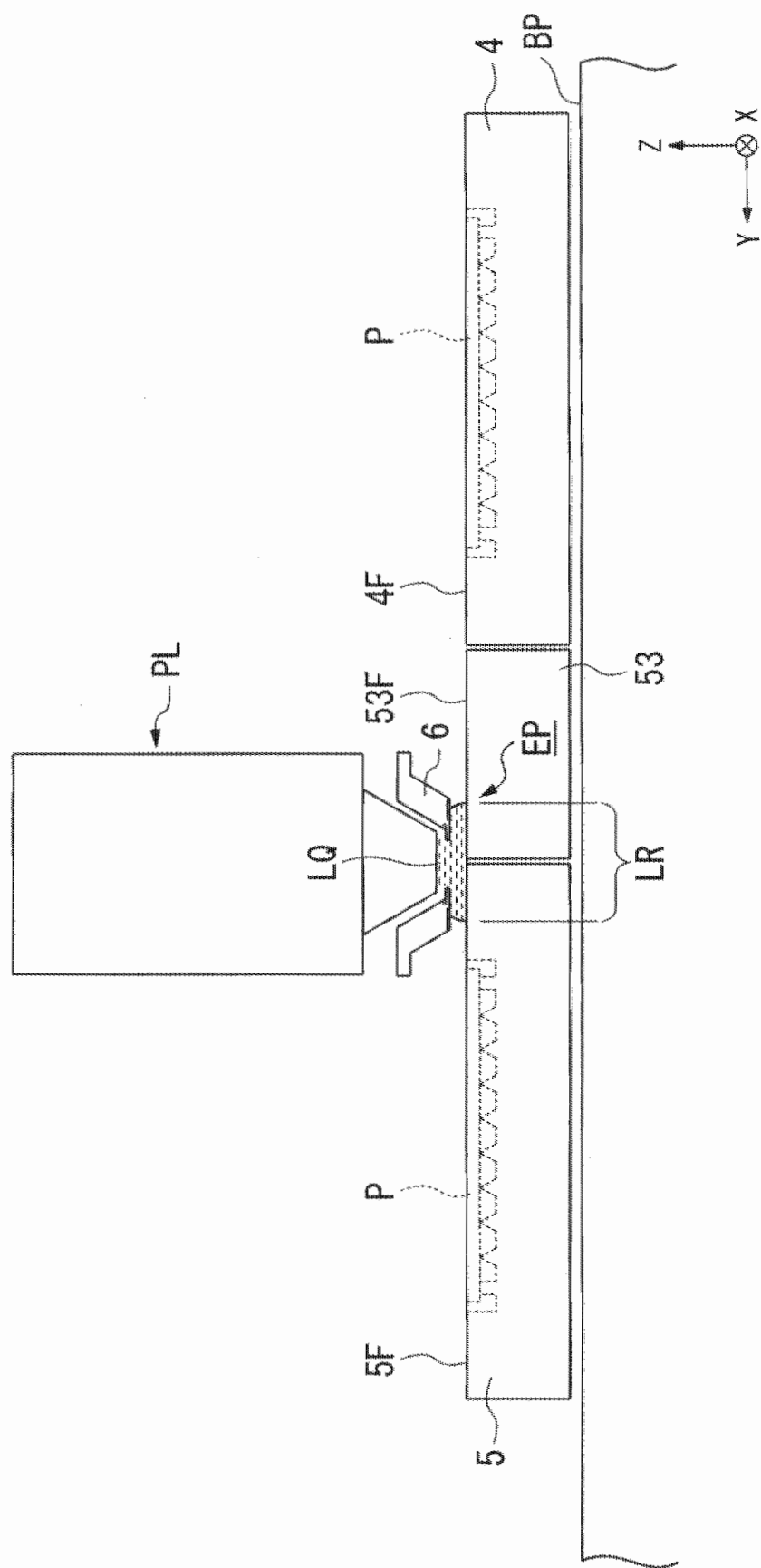


FIG. 40

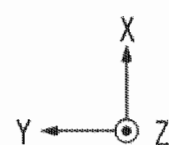
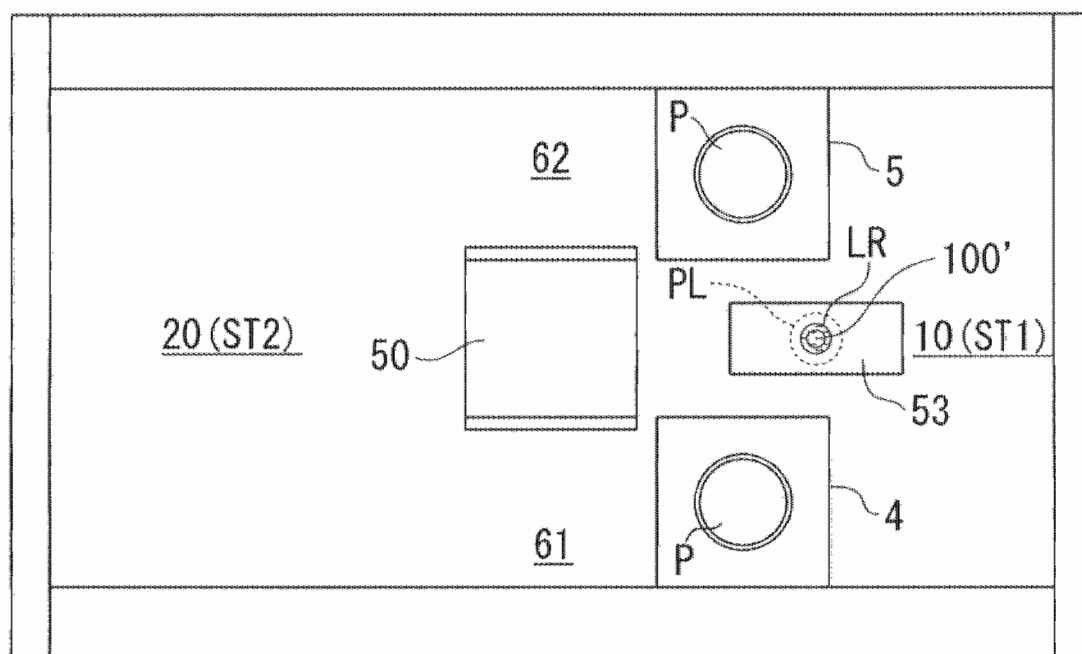


FIG. 41

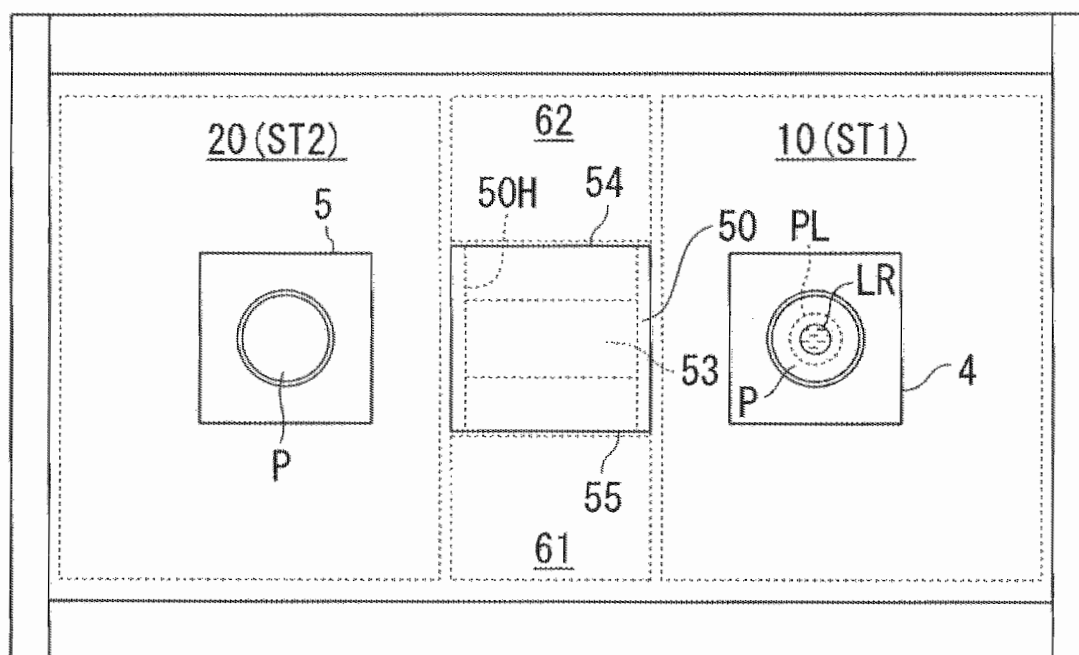


FIG. 42

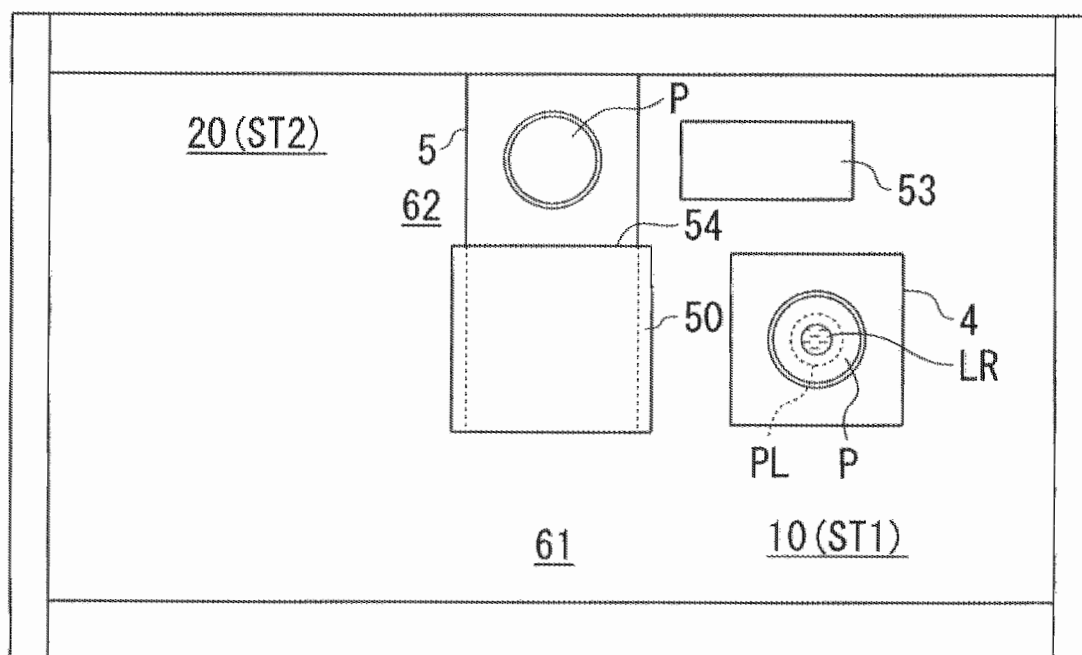


FIG. 43

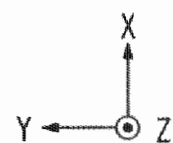
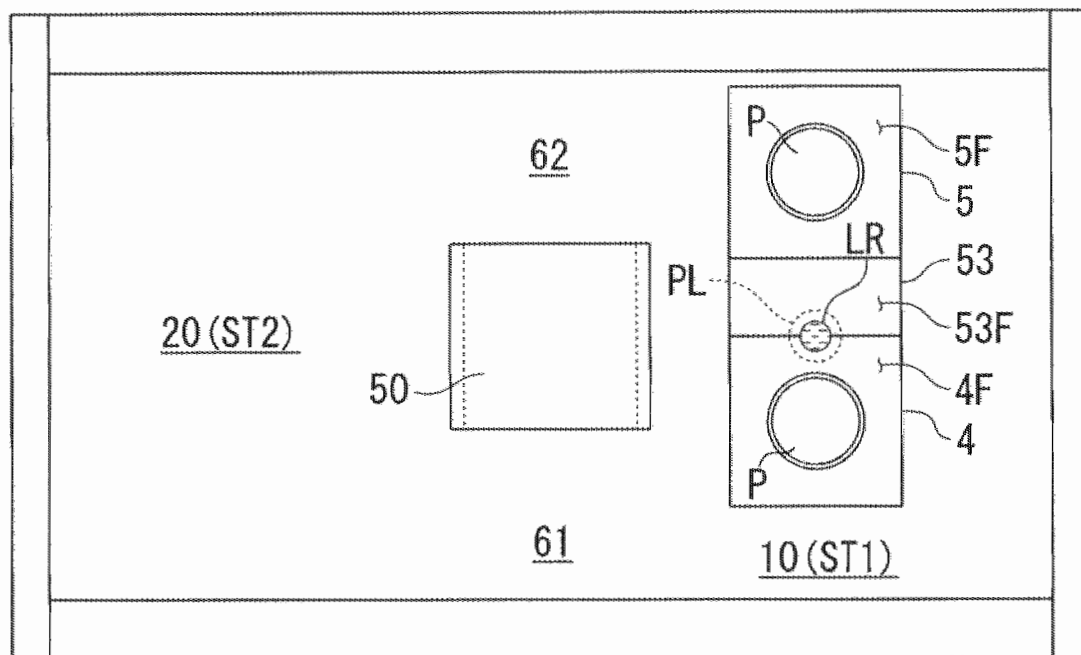


FIG. 44

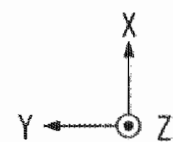
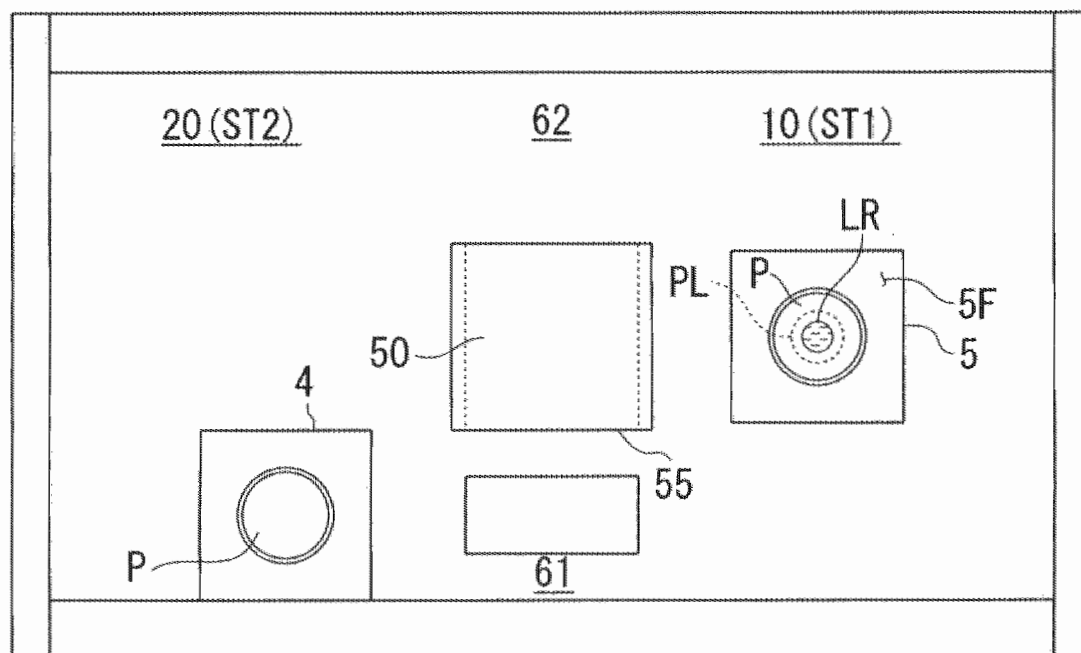


FIG. 45

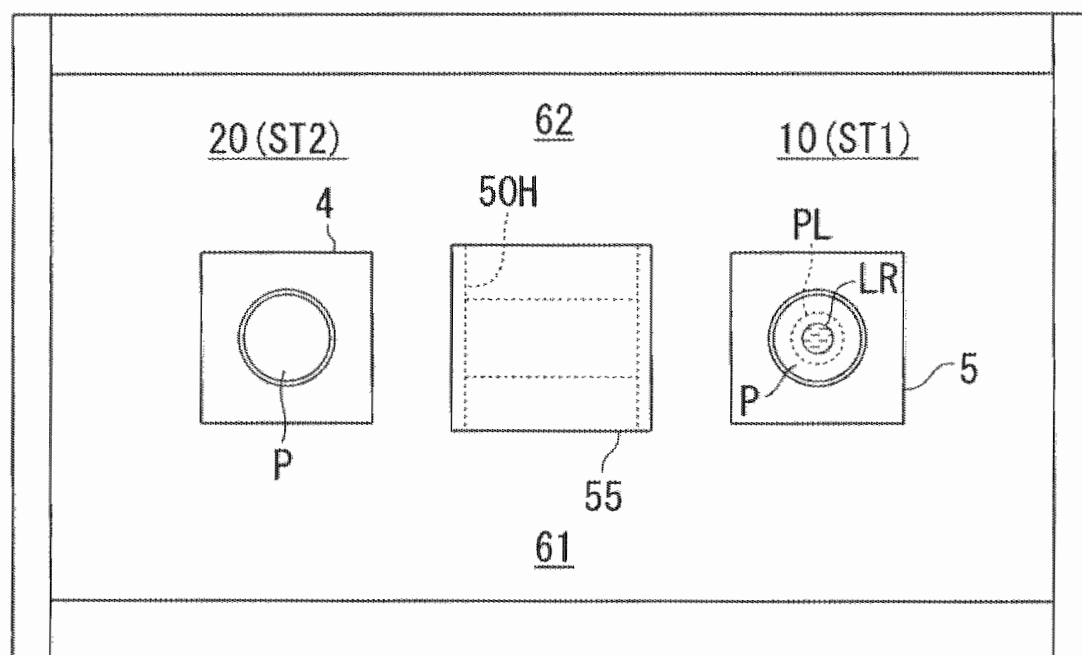


FIG. 46

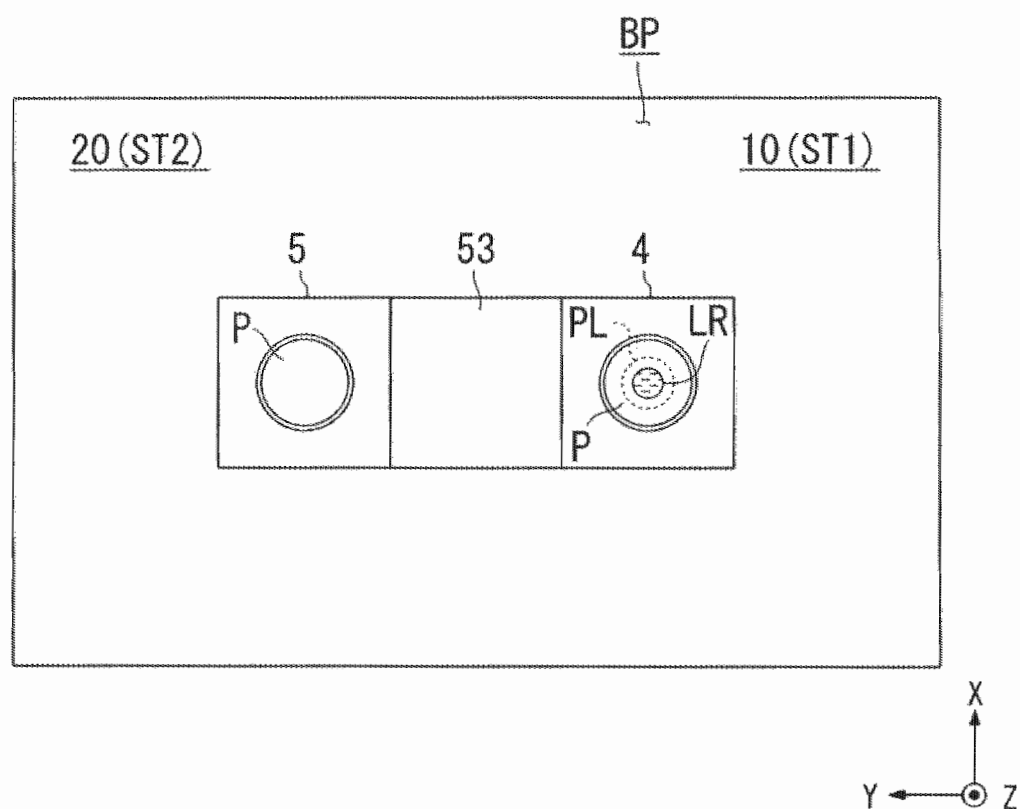


FIG. 47

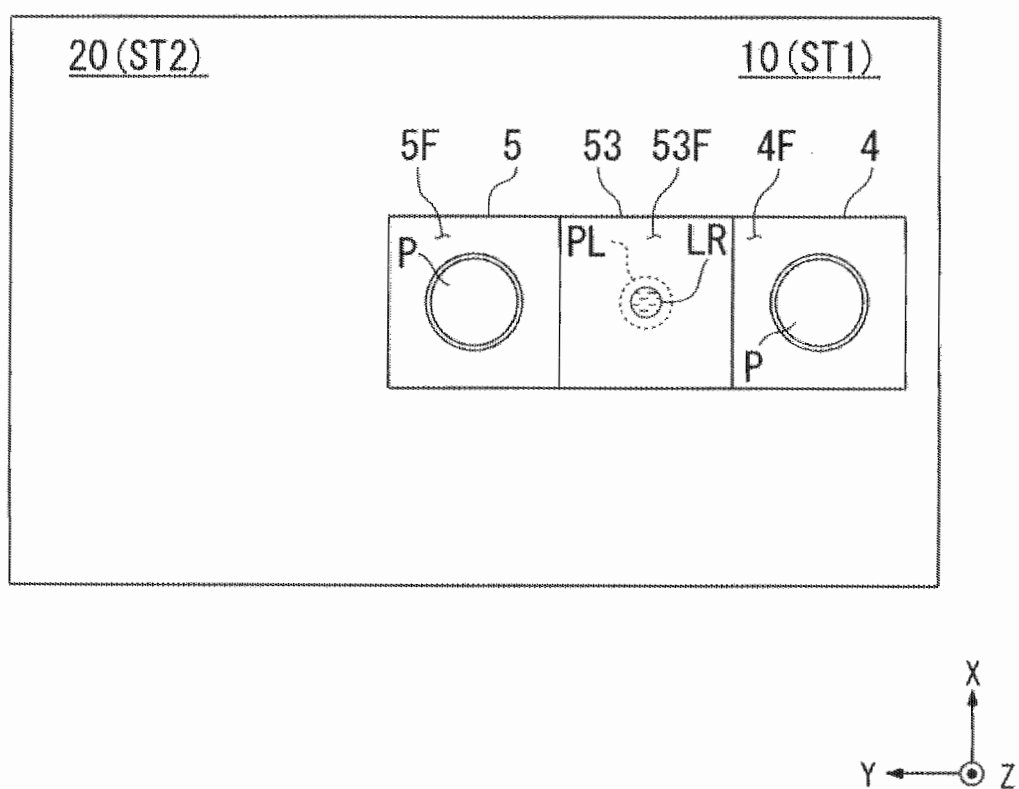


FIG. 48

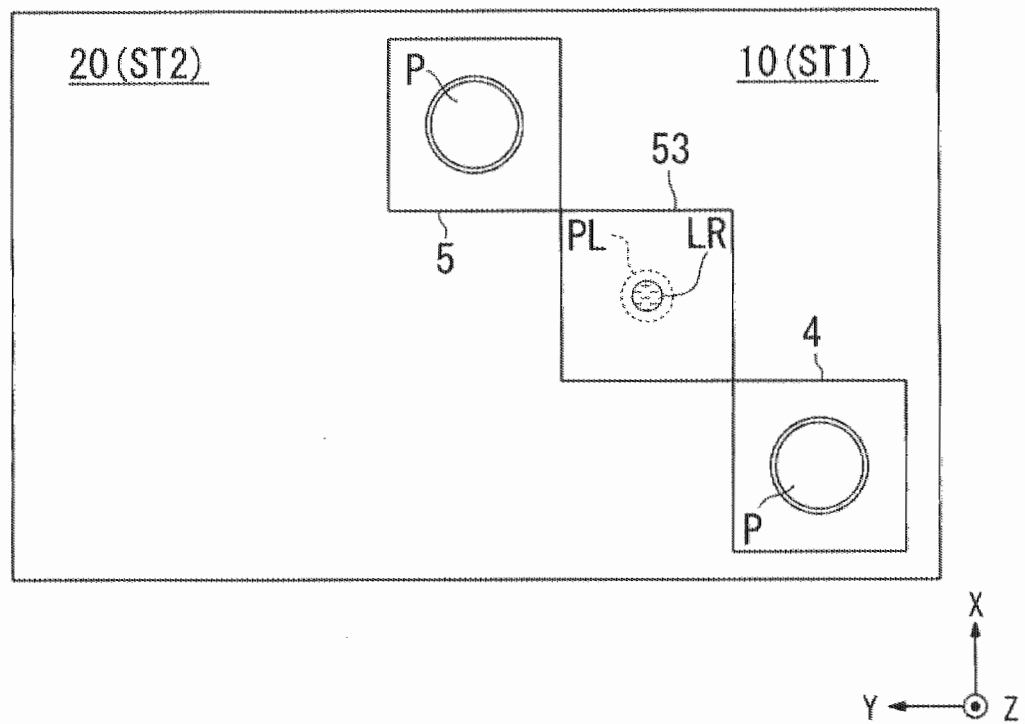


FIG. 49

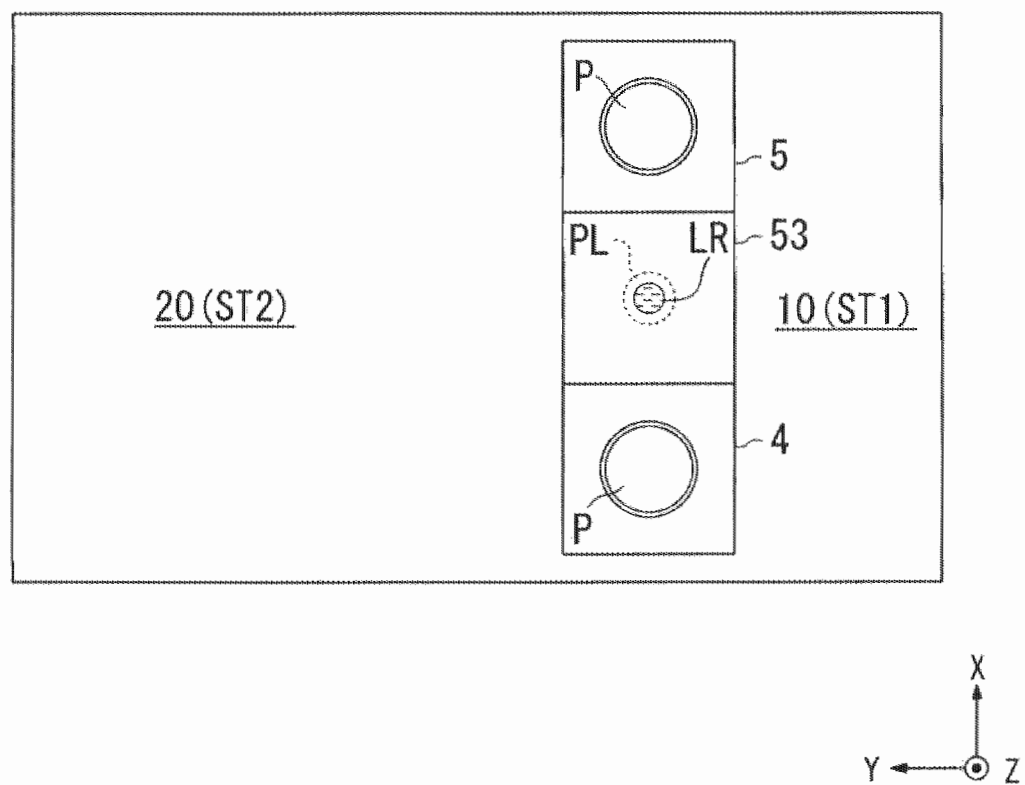


FIG. 50

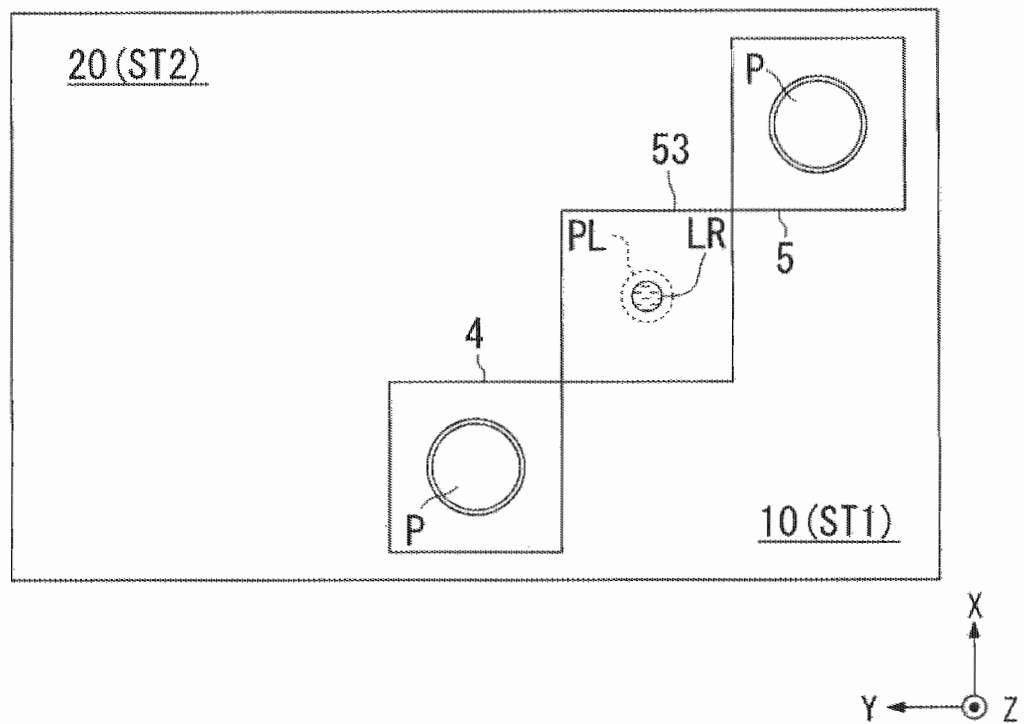


FIG. 51

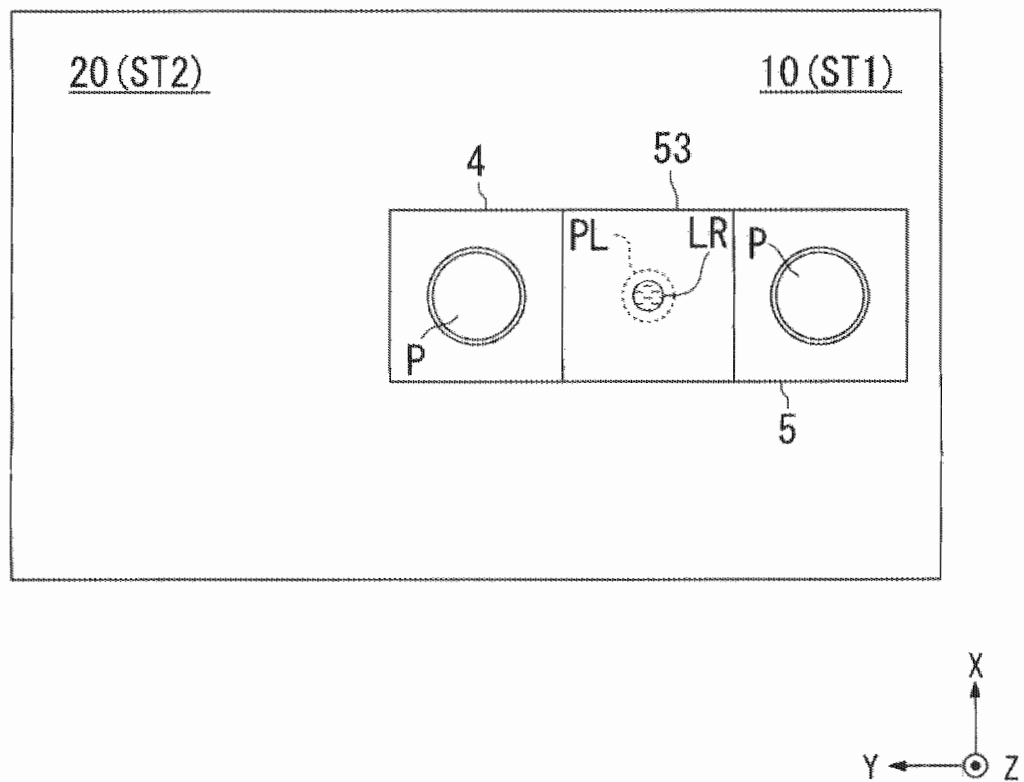


FIG. 52

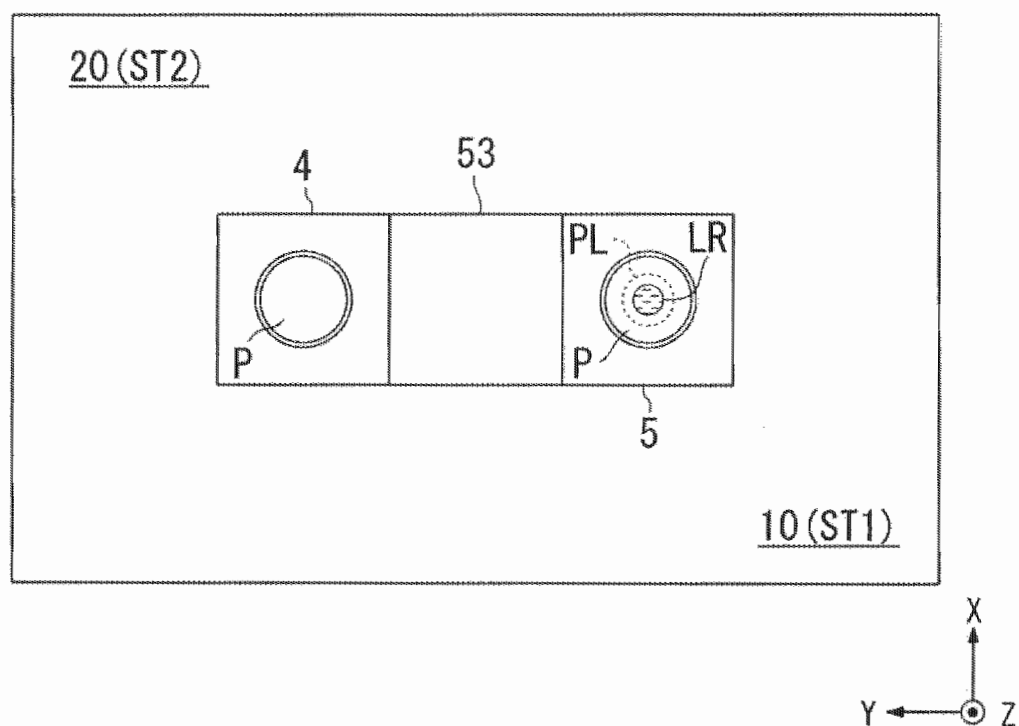


Fig. 53

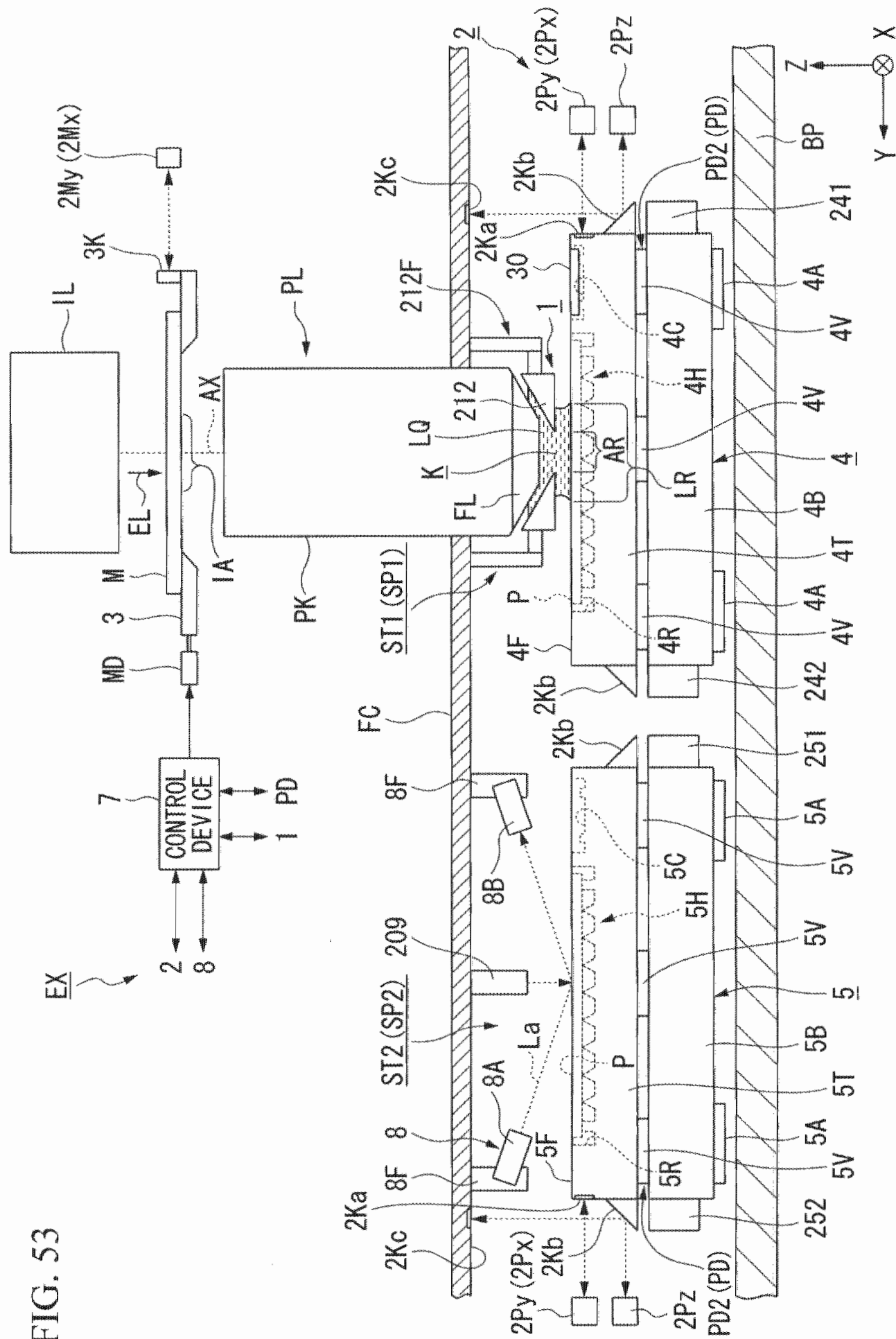


Figure 54 is a schematic diagram of a semiconductor device 500, showing two processing stages, SP2 (ST2) and SP1 (ST1), within a central block 50. The diagram includes various components and labels:

- Central Block 50:** The main body of the device, containing a central region (PL) and a peripheral region (BP).
- Processing Stages:**
 - SP2 (ST2):** The first stage, located on the left. It includes a central region (PL) and a peripheral region (BP). The central region (PL) is defined by a dashed line and contains a central feature (30). The peripheral region (BP) is defined by a dashed line and contains a central feature (30).
 - SP1 (ST1):** The second stage, located on the right. It includes a central region (PL) and a peripheral region (BP). The central region (PL) is defined by a dashed line and contains a central feature (30). The peripheral region (BP) is defined by a dashed line and contains a central feature (30).
- Electrodes and Features:**
 - E1, E2, E3, E4:** Electrodes or features located around the central region (PL) in both stages.
 - 271, 272, 273 (270), 274A (274), 274B (274):** Various features or regions within the peripheral region (BP) of both stages.
 - 251, 252, 253 (270), 254A (275), 254B (275):** Various features or regions within the peripheral region (BP) of both stages.
 - 271, 272, 273 (270), 274A (274), 274B (274):** Various features or regions within the peripheral region (BP) of both stages.
- Coordinate System:** A coordinate system (X, Y, Z) is shown in the top right corner, indicating the orientation of the device.
- Scale Bar:** A scale bar (80) is shown in the top right corner, indicating the size of the device.

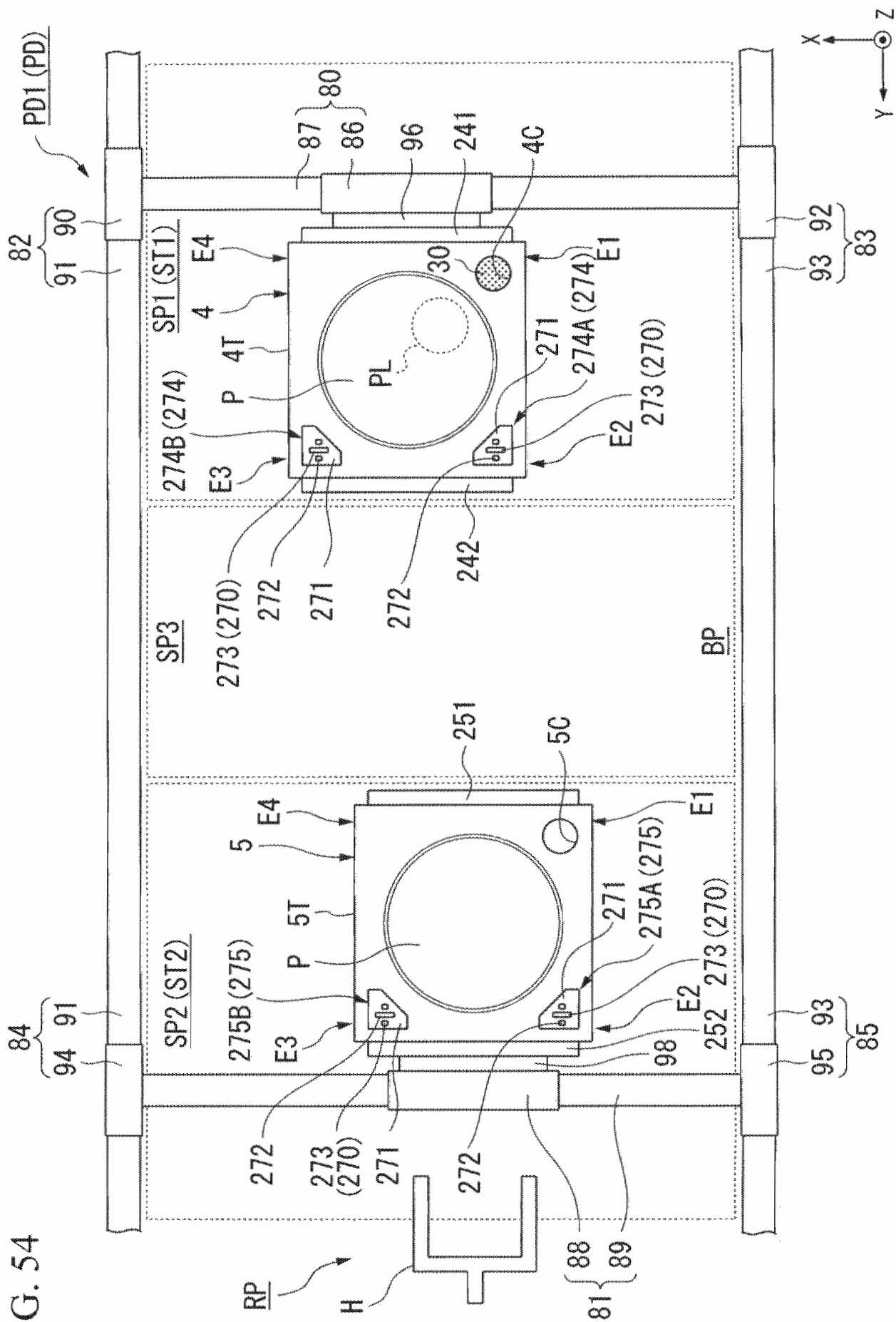


FIG. 55

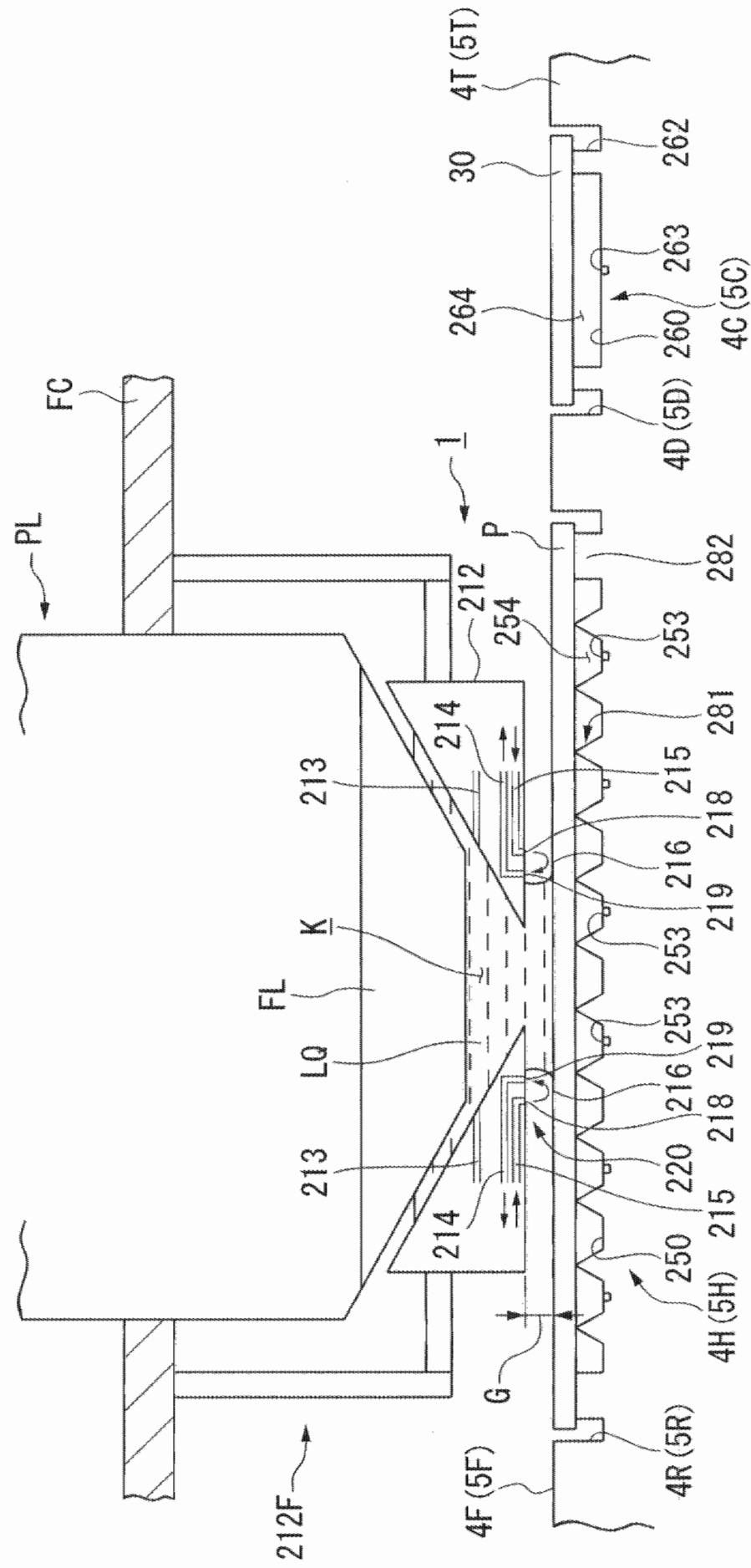


FIG. 56

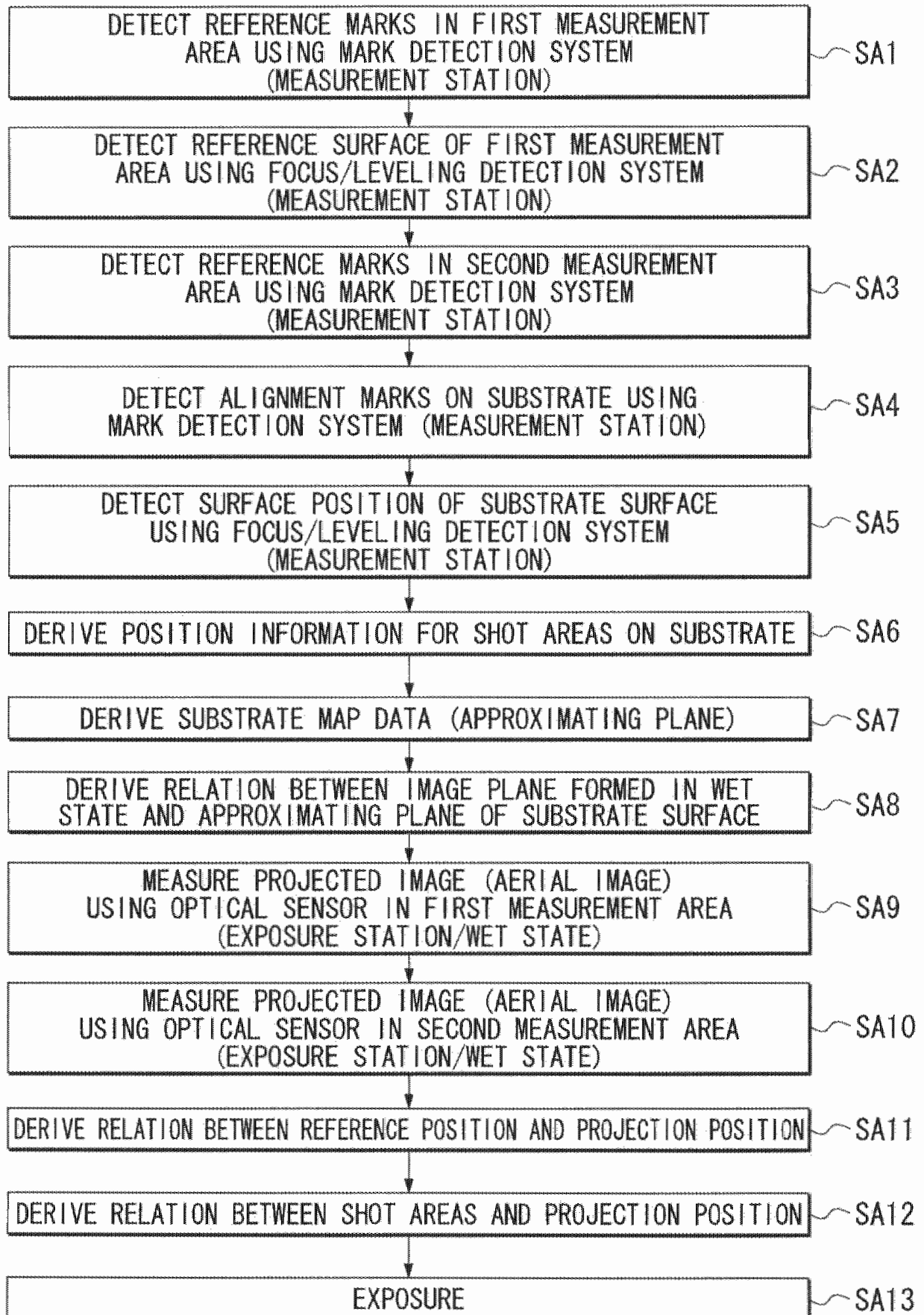


FIG. 57

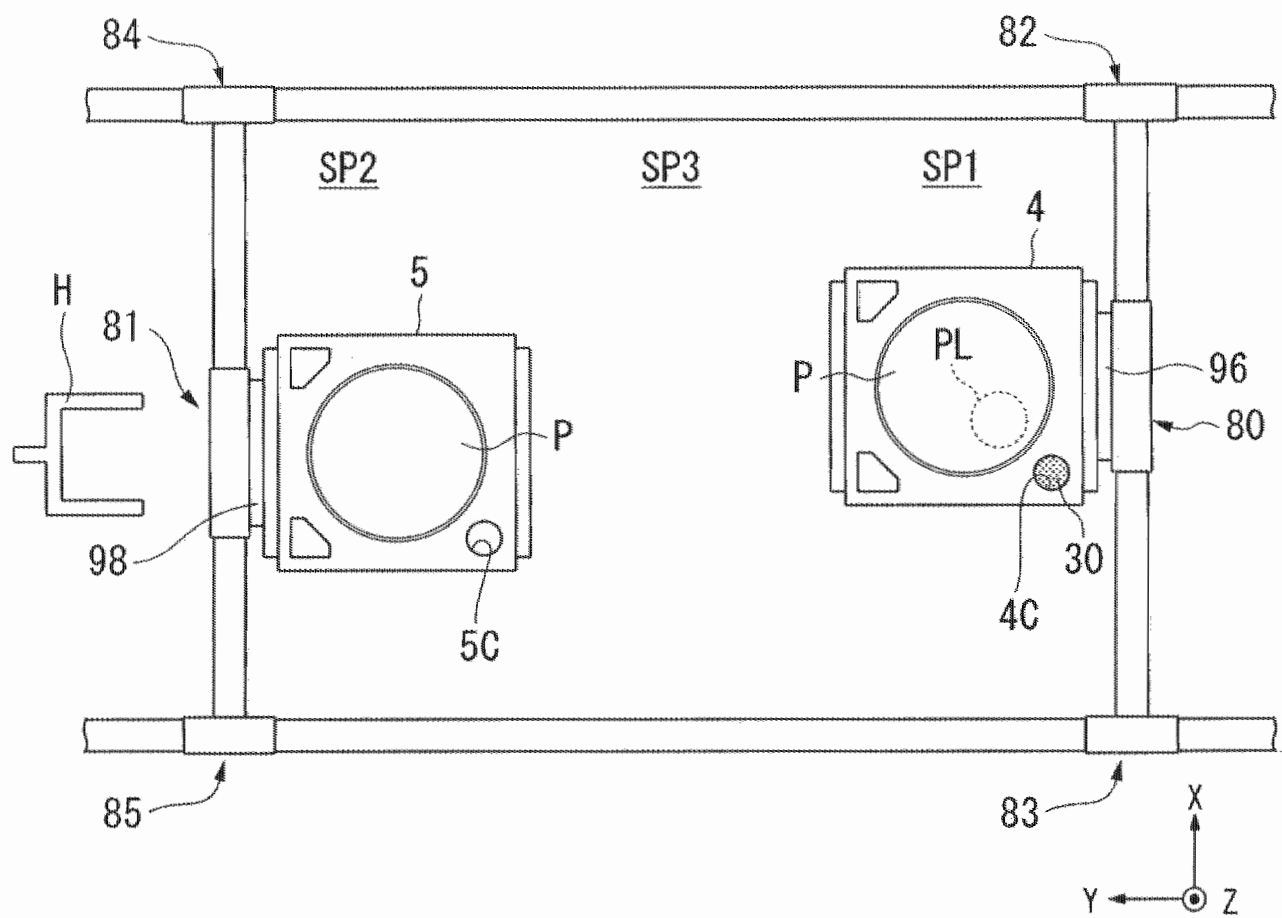


FIG. 58

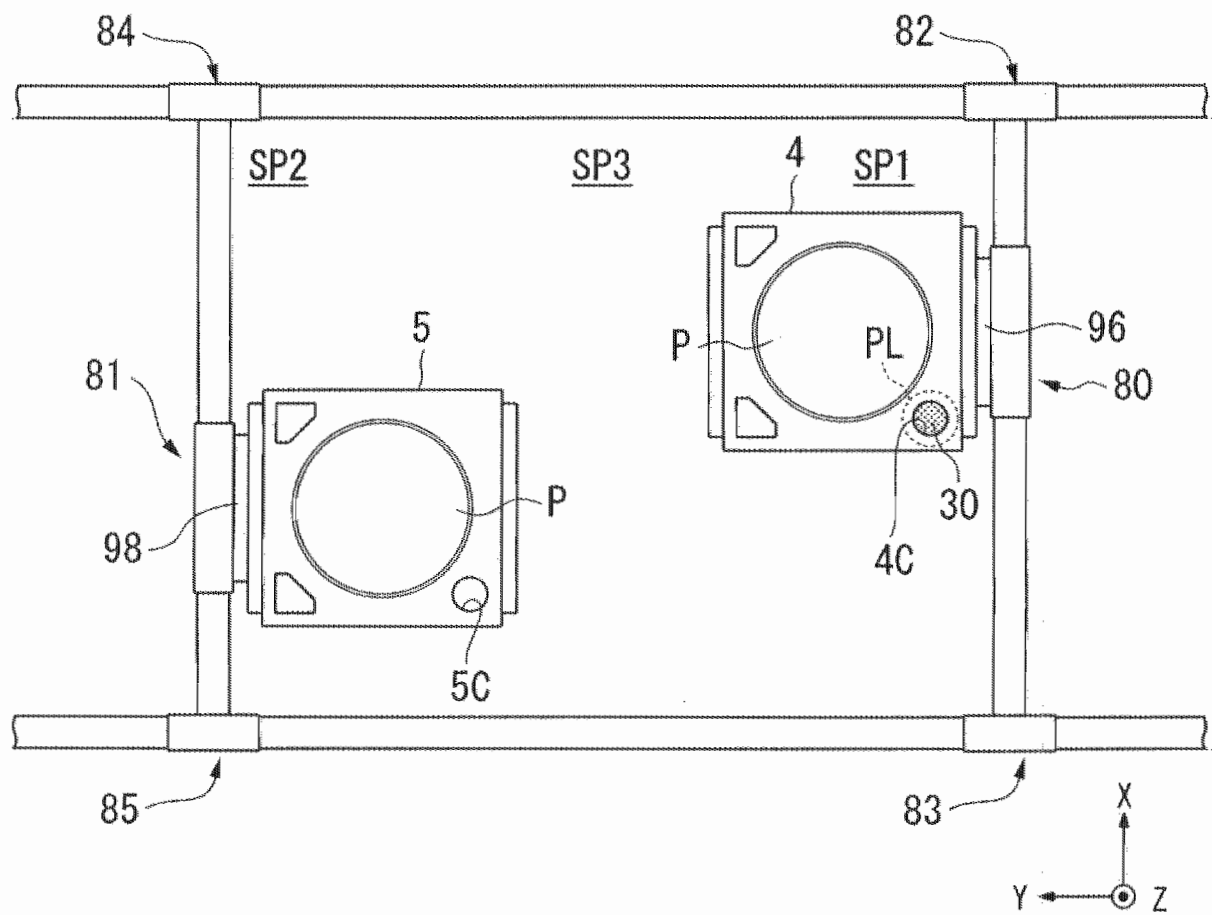


FIG. 59

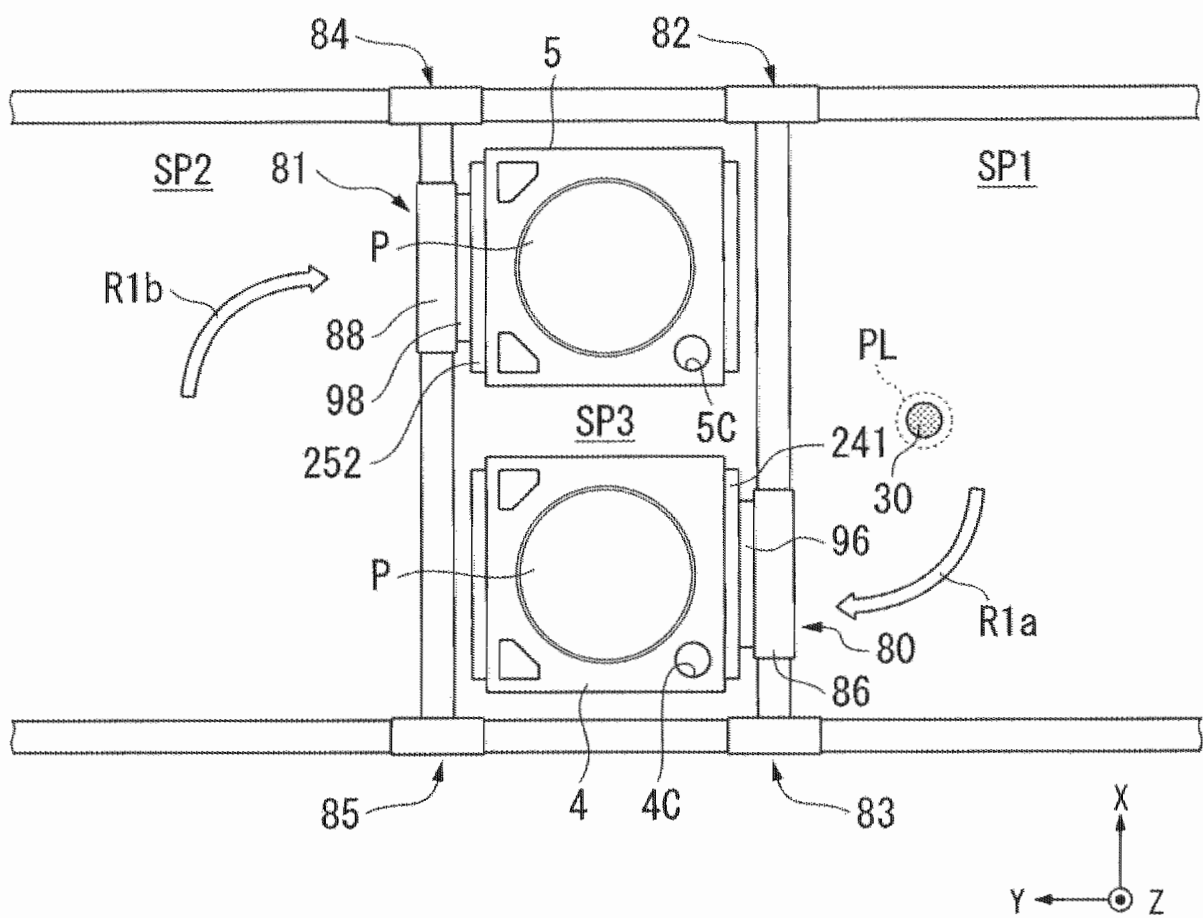


FIG. 60

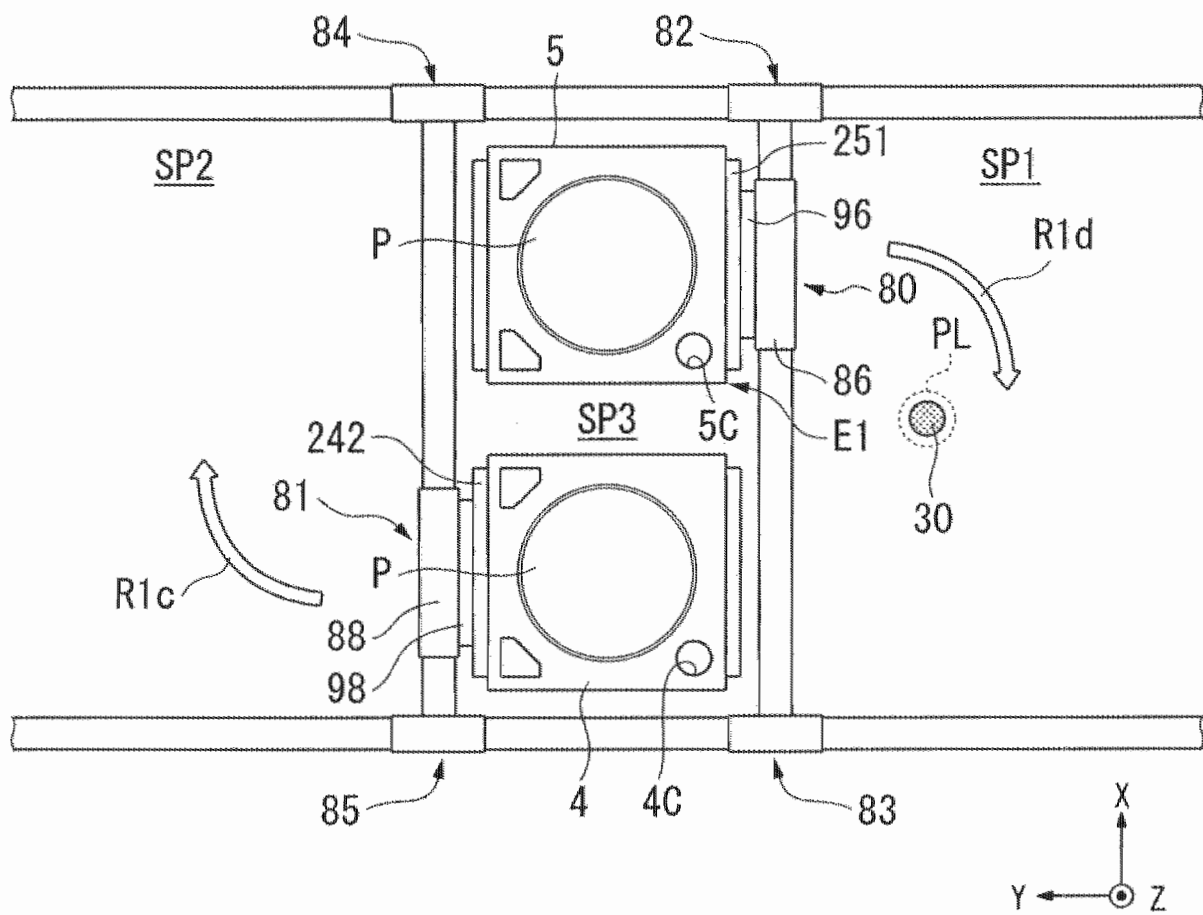


FIG. 61

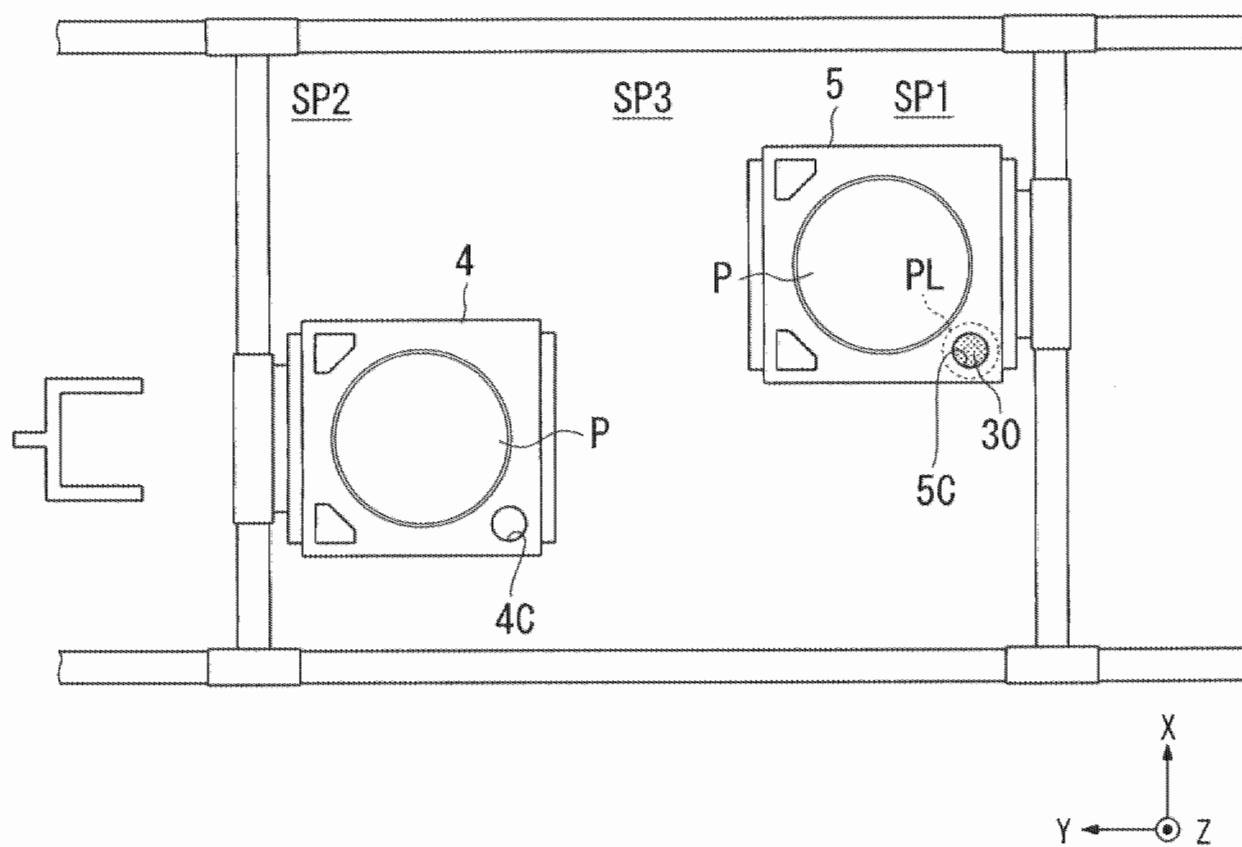


FIG. 62

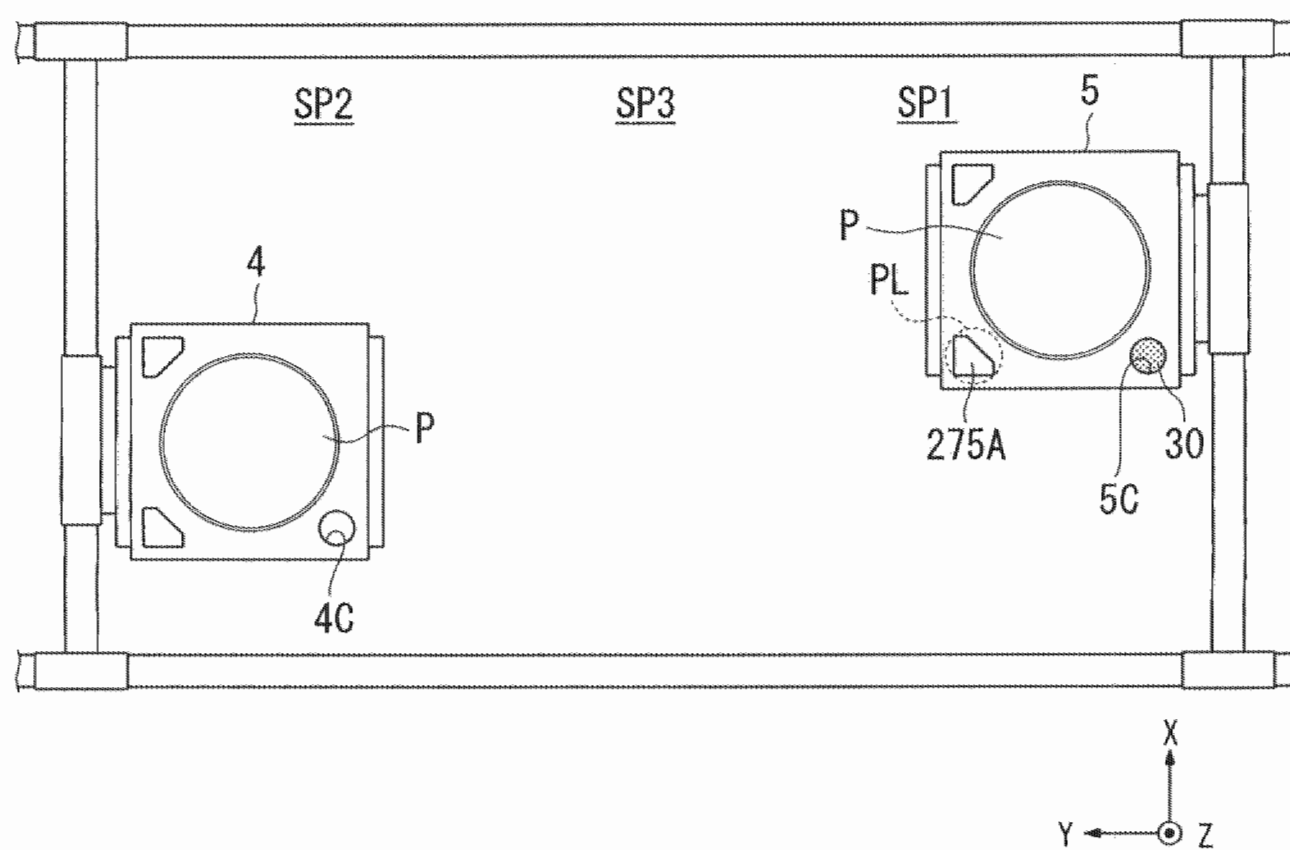


FIG. 63

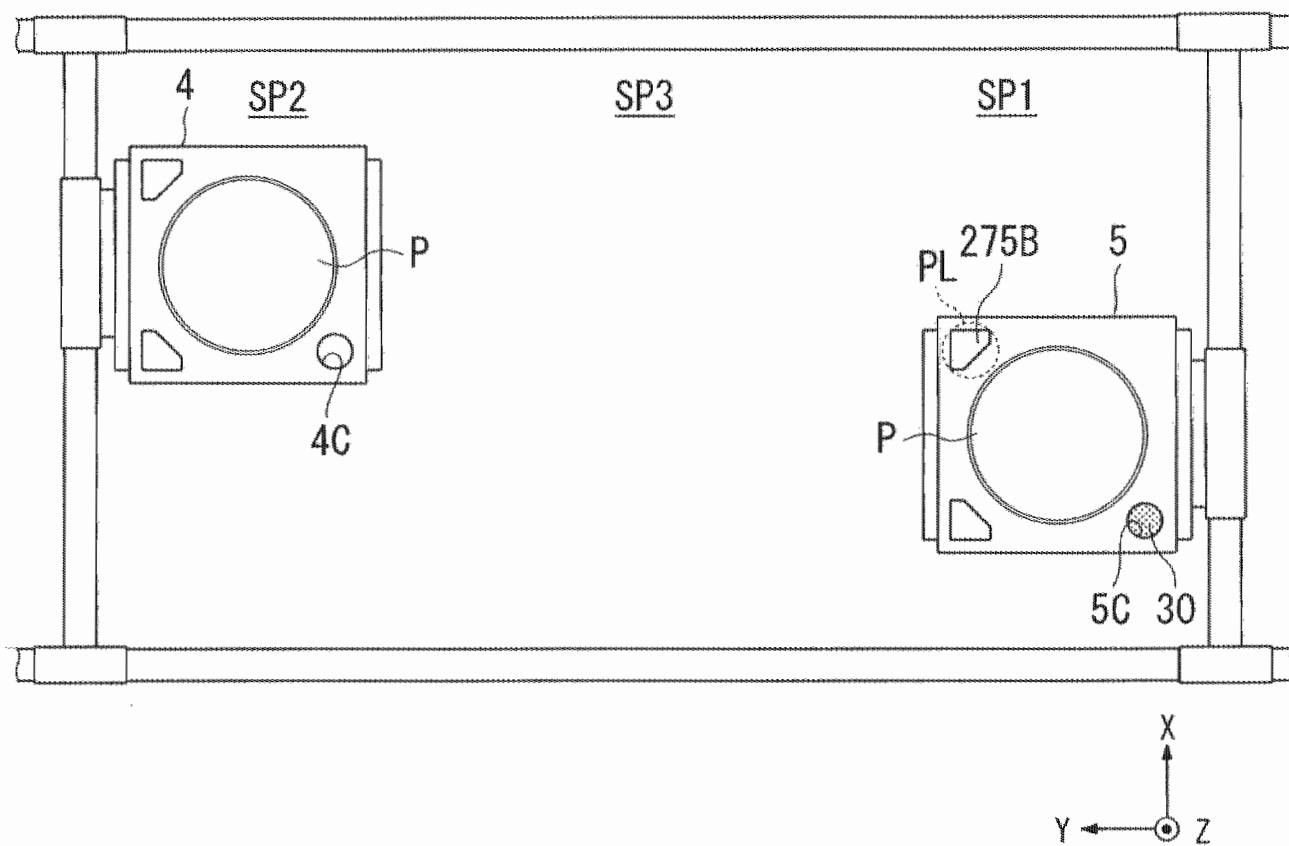


FIG. 64

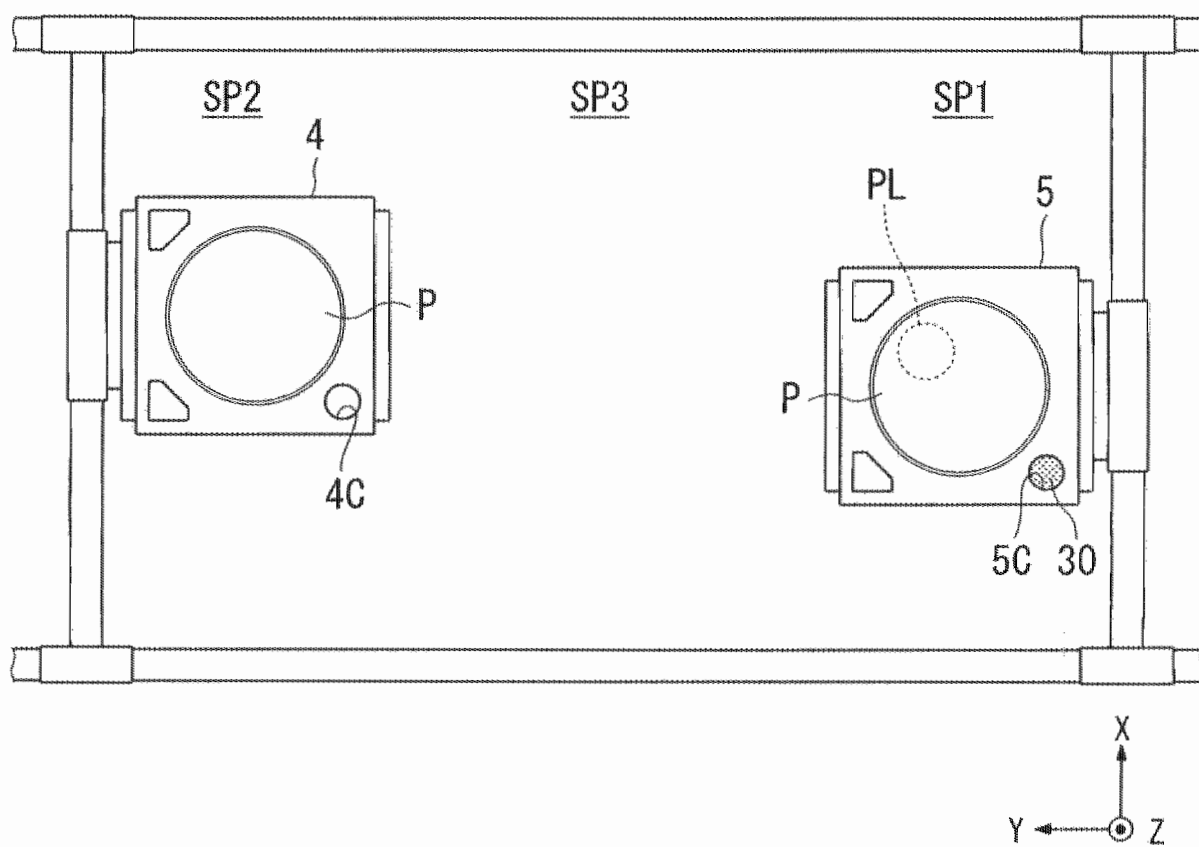


FIG. 65

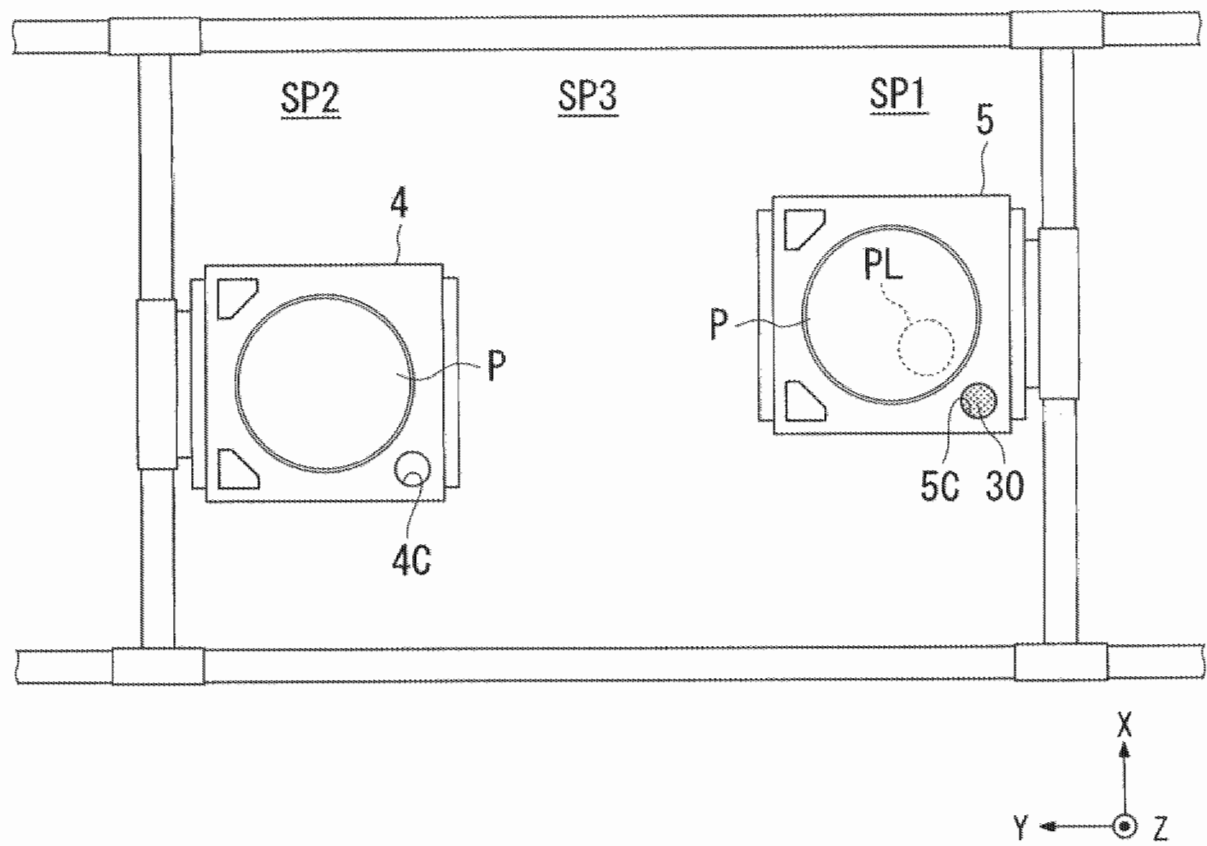


FIG. 66

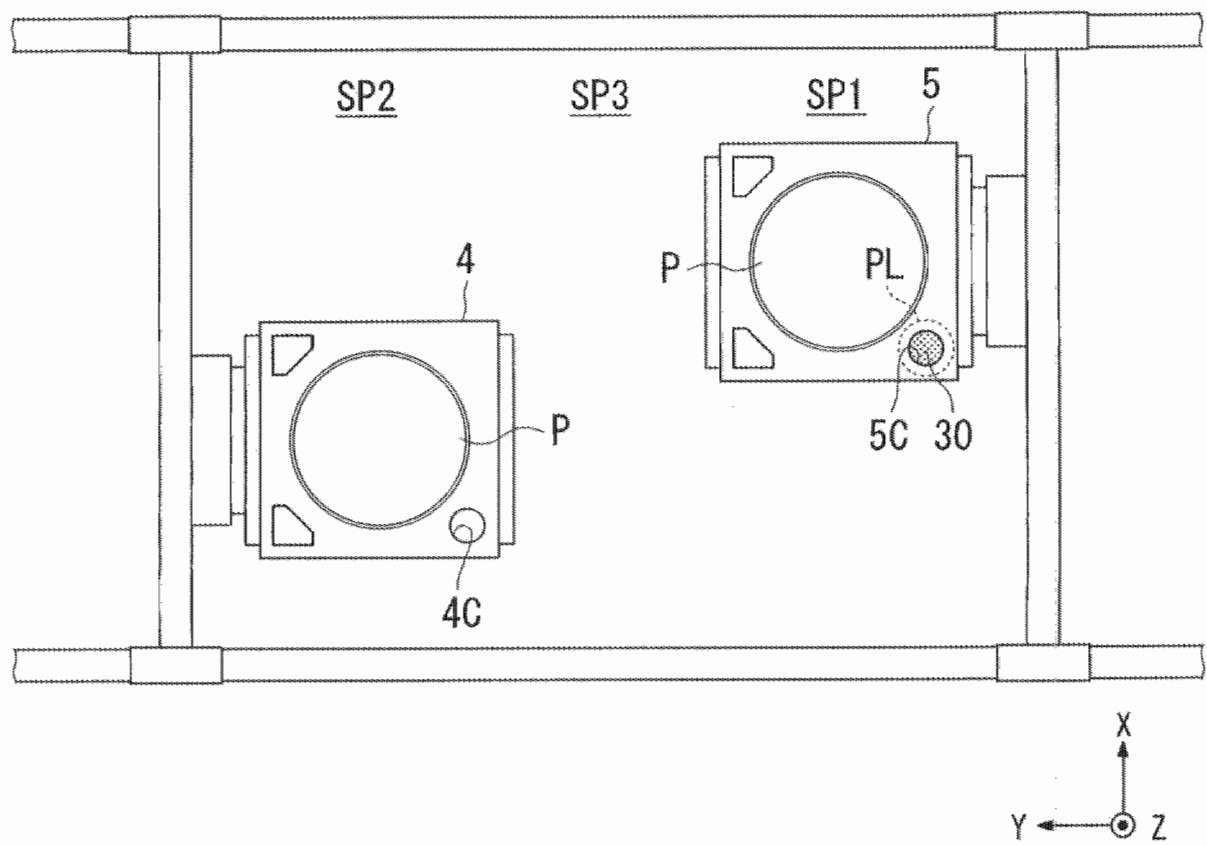


FIG. 67

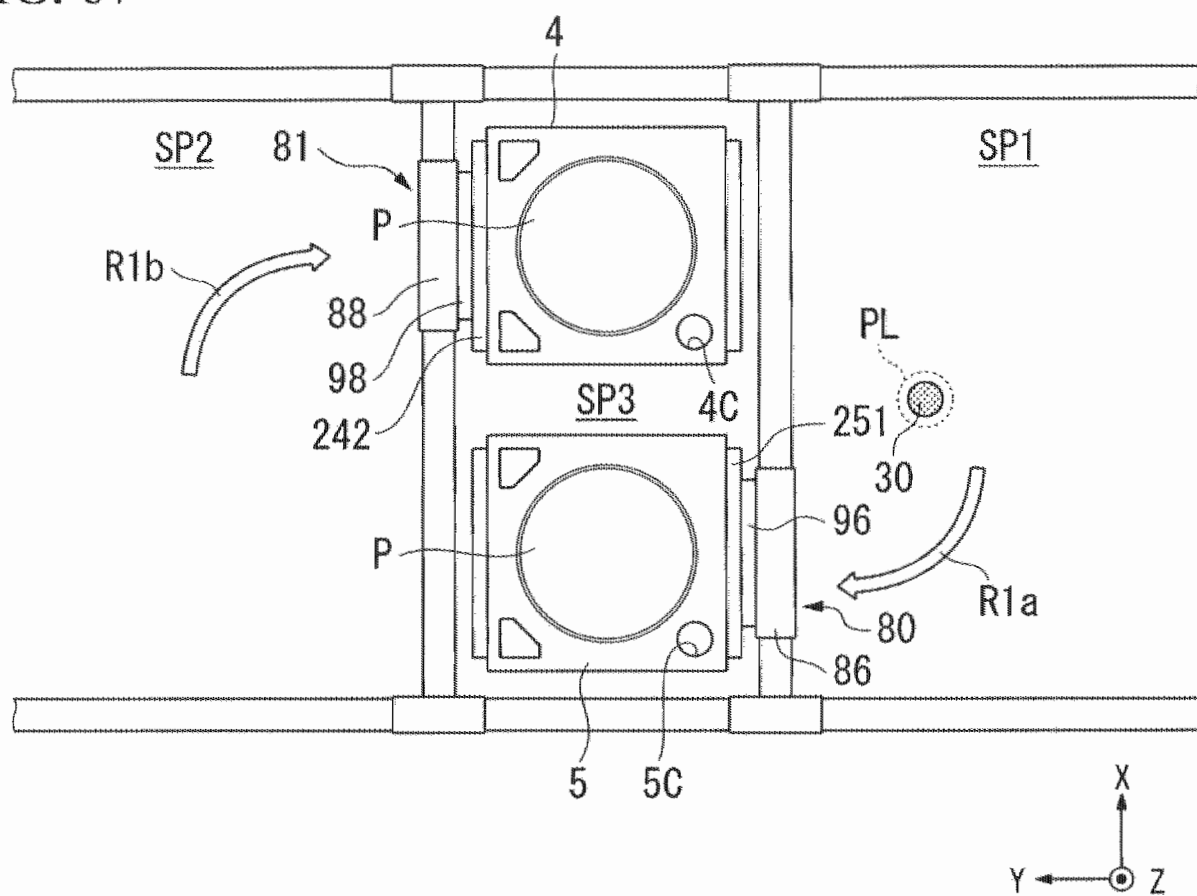


FIG. 68

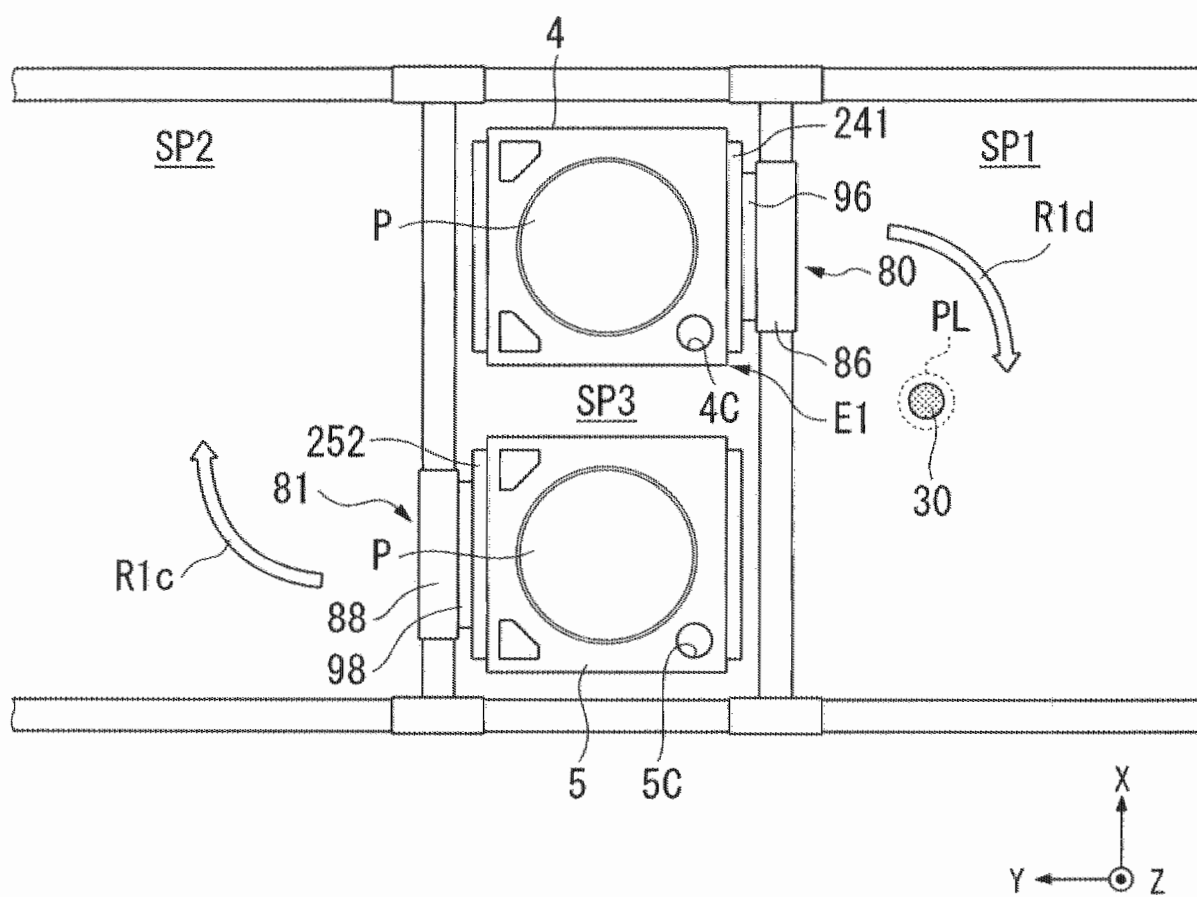


FIG. 69

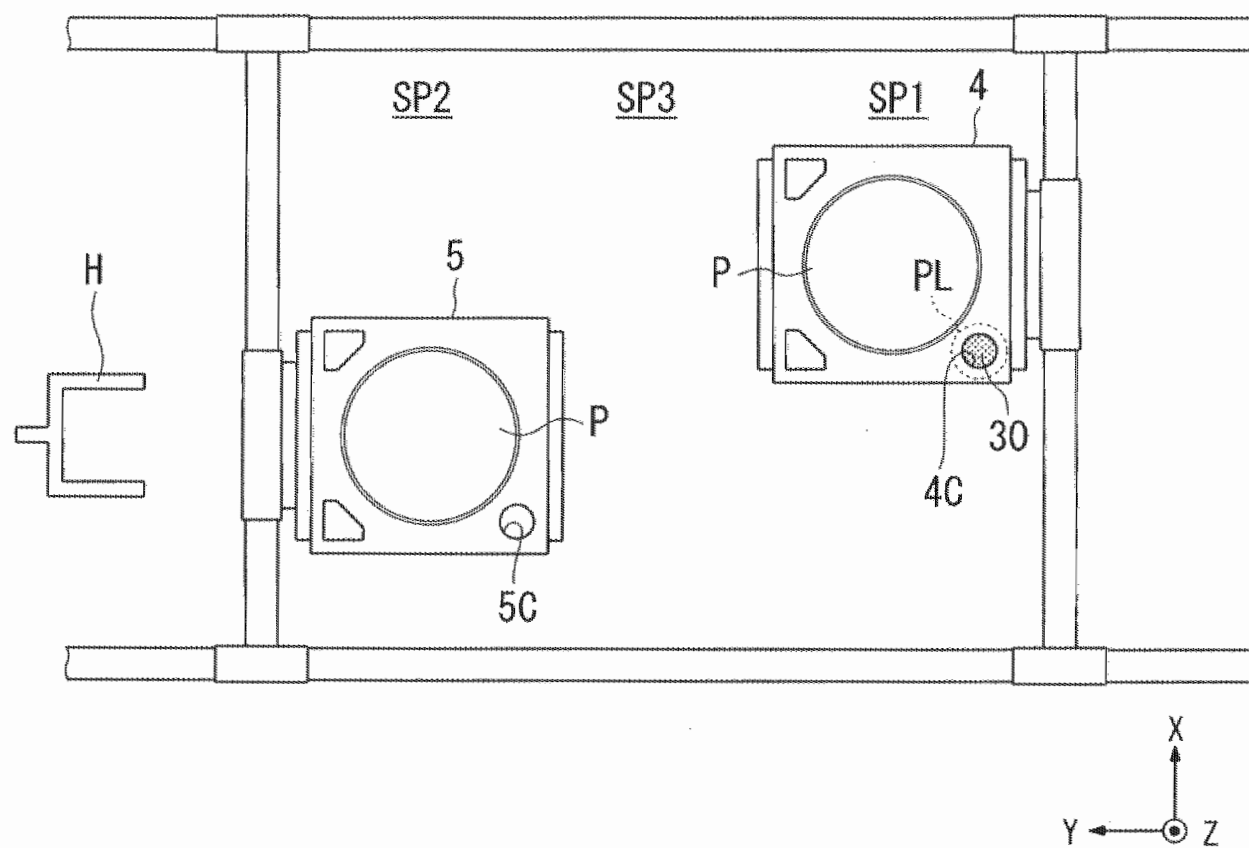


FIG. 70

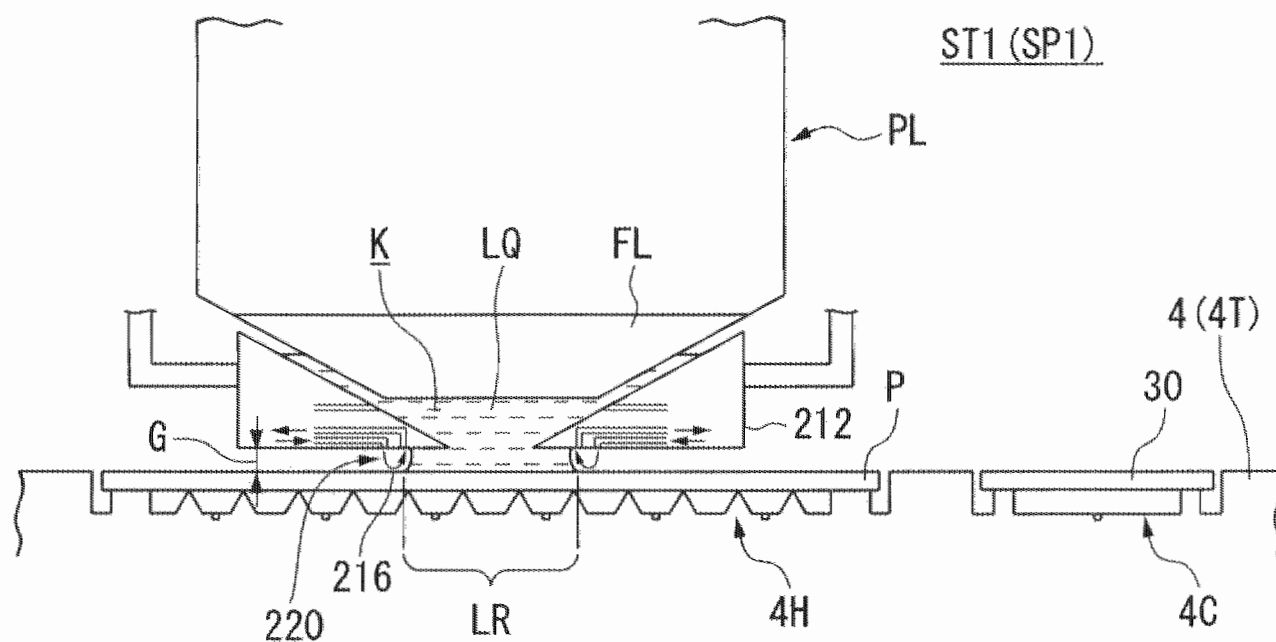


FIG. 71

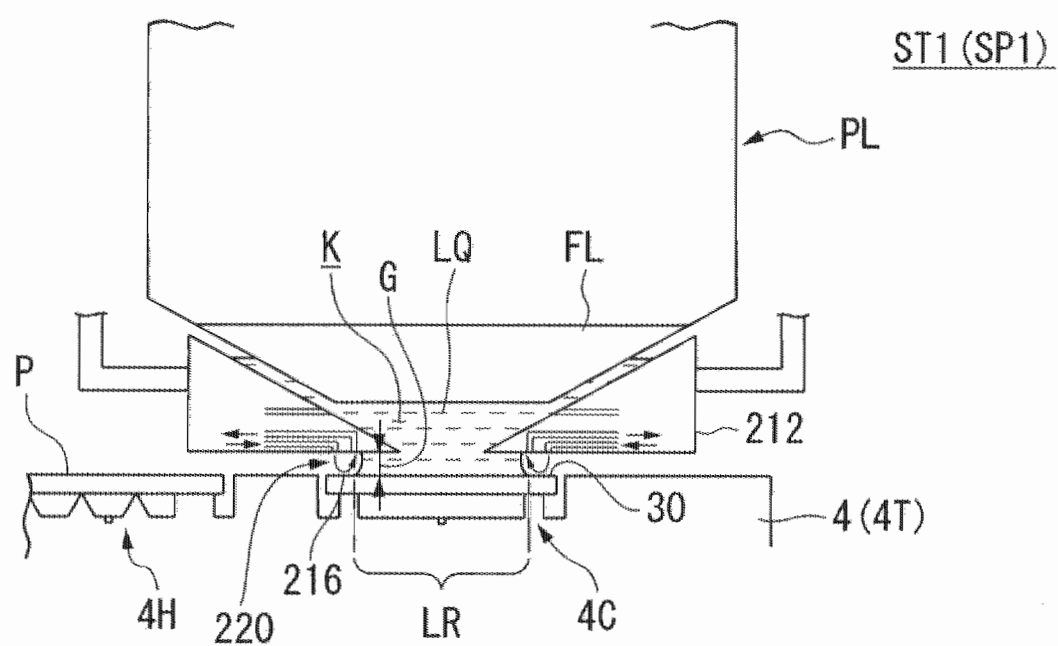


FIG. 72

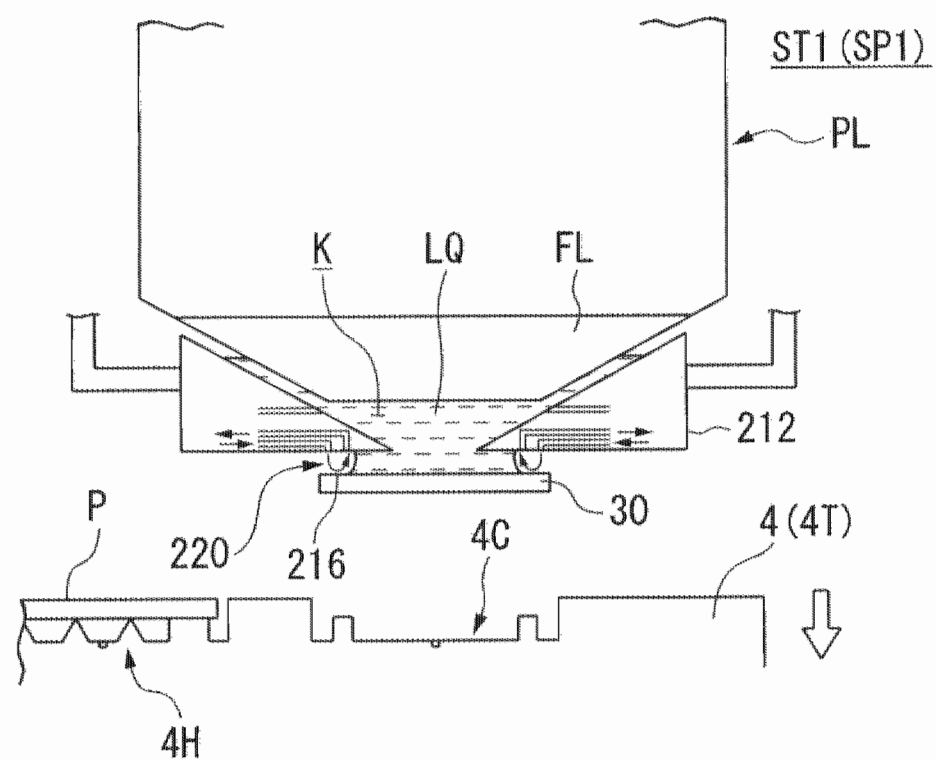


FIG. 73

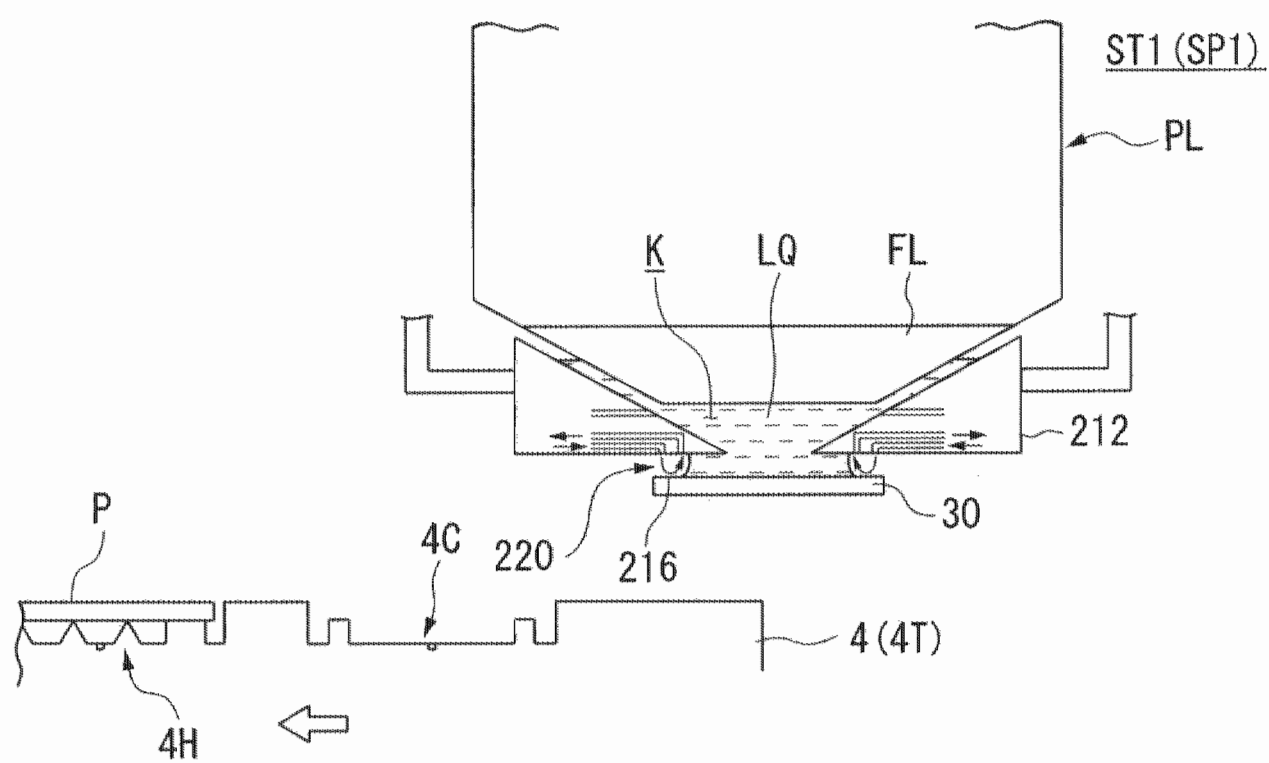


FIG. 74

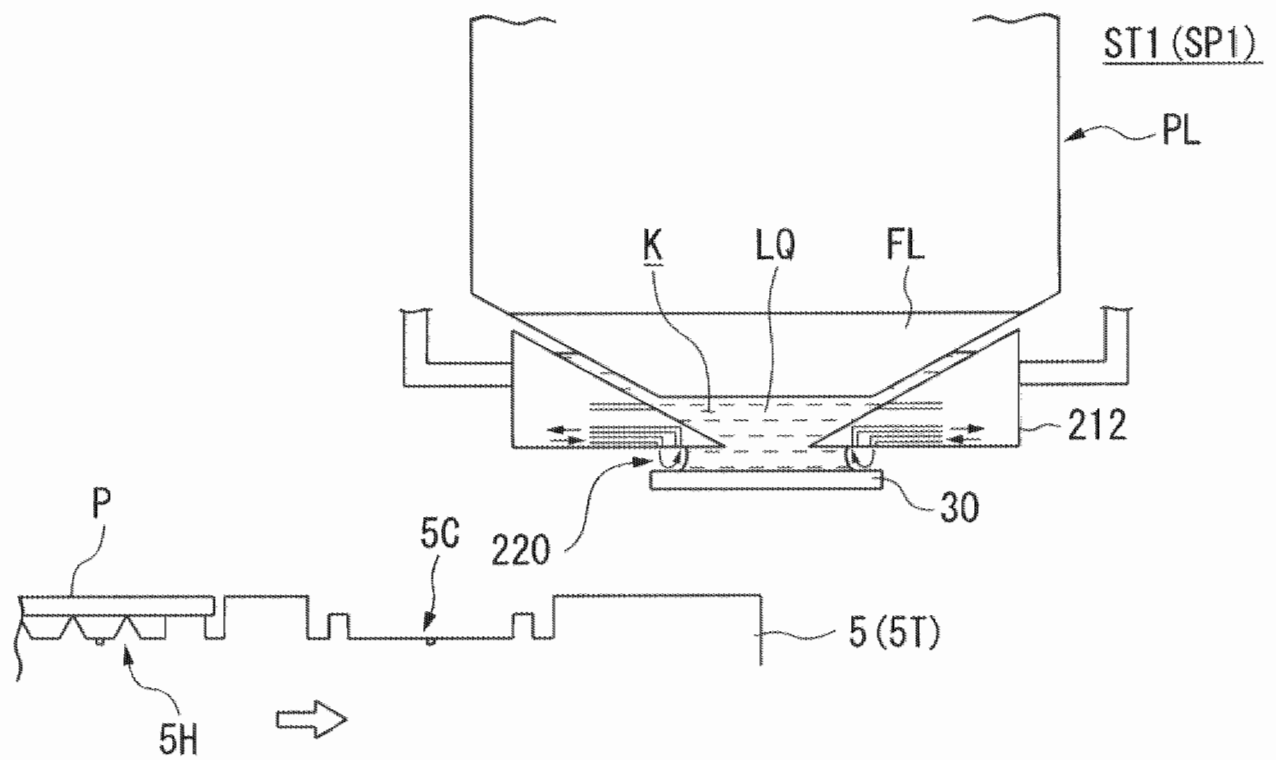


FIG. 75

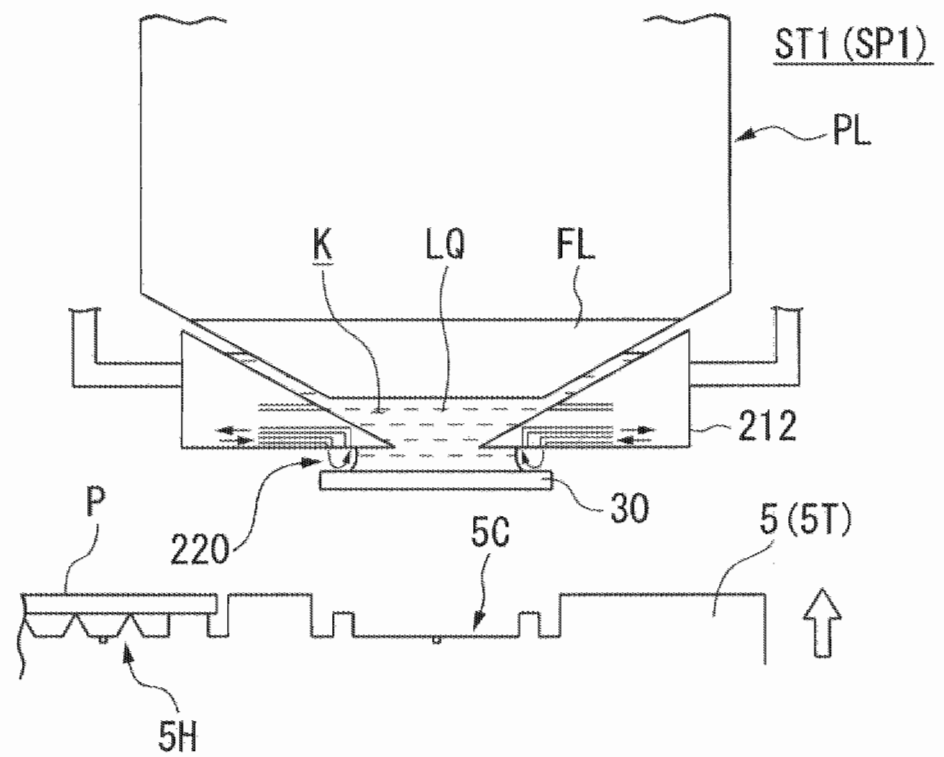


FIG. 76

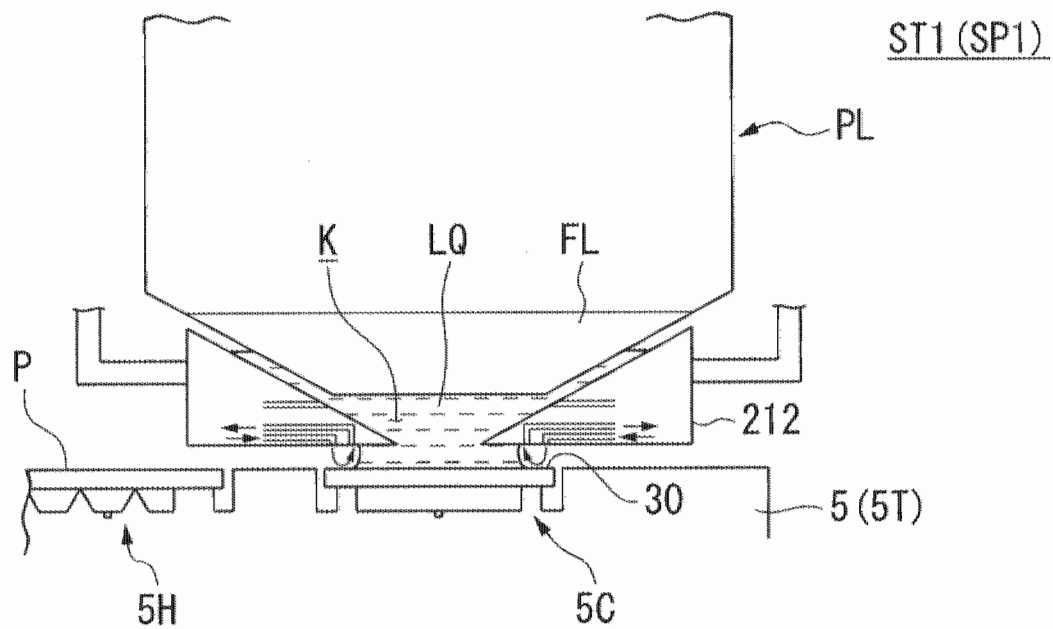


FIG. 77

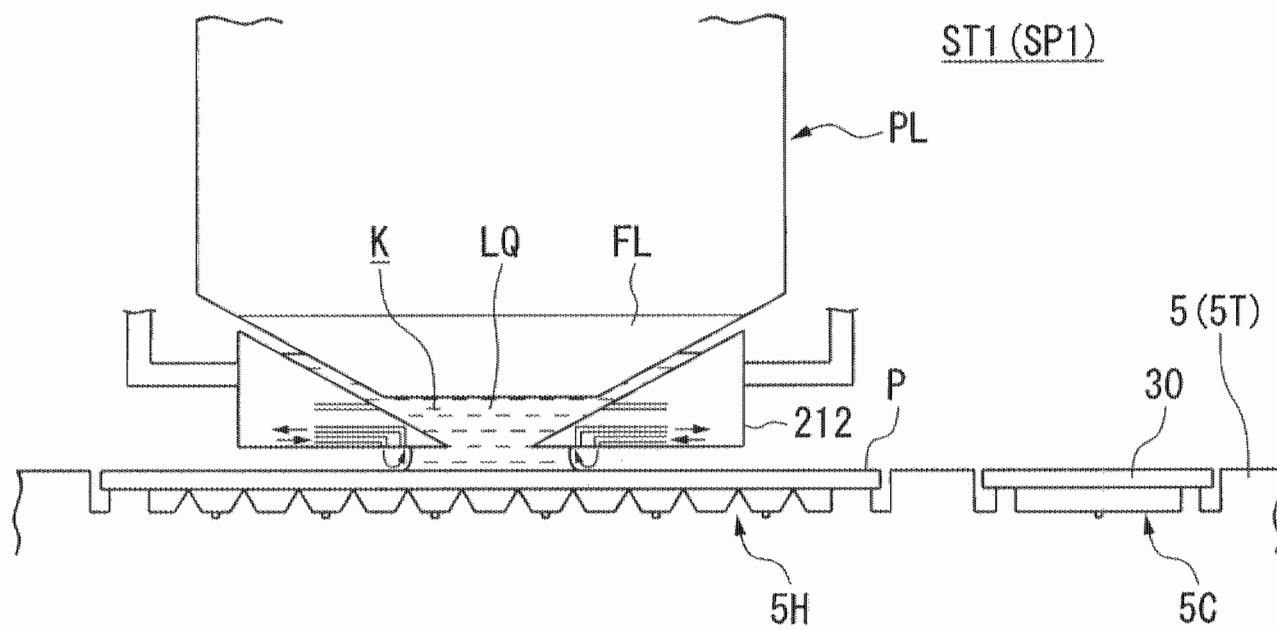


FIG. 78

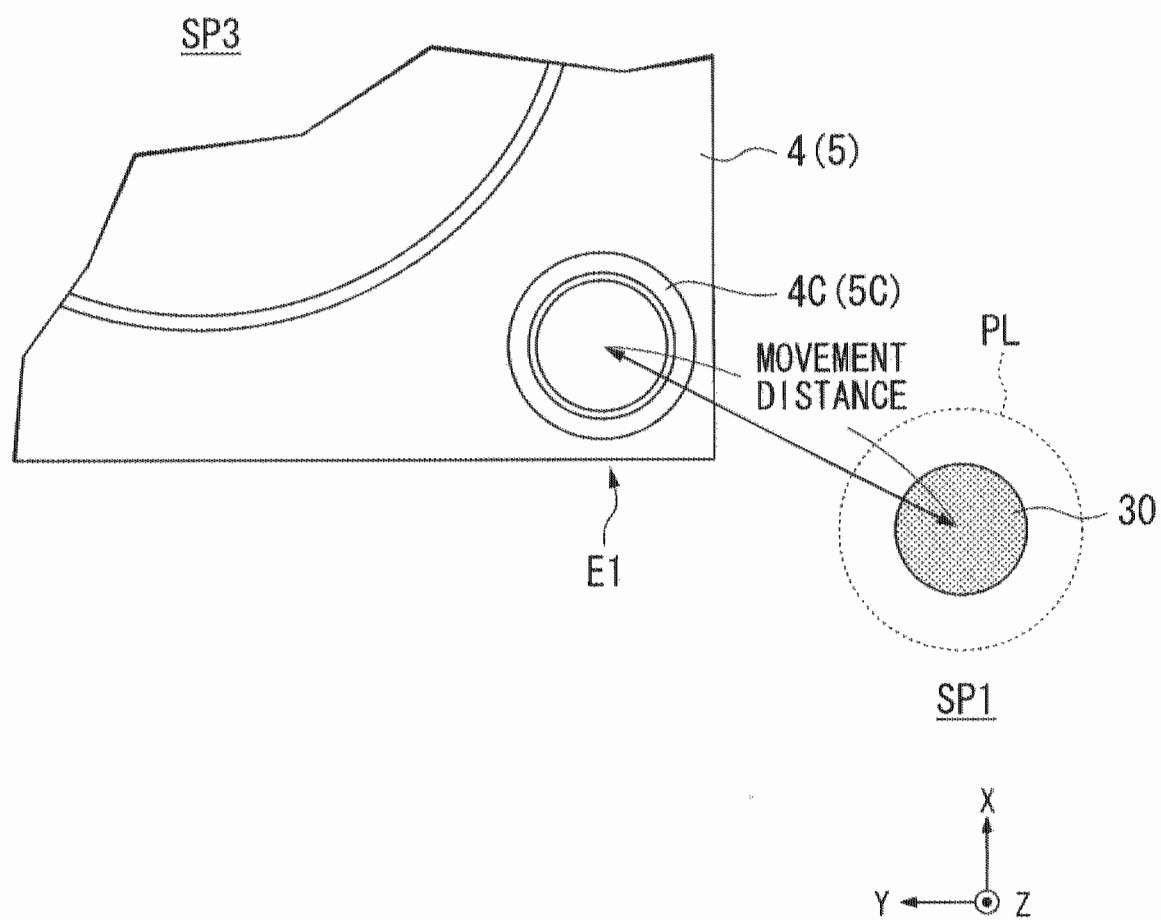


FIG. 79

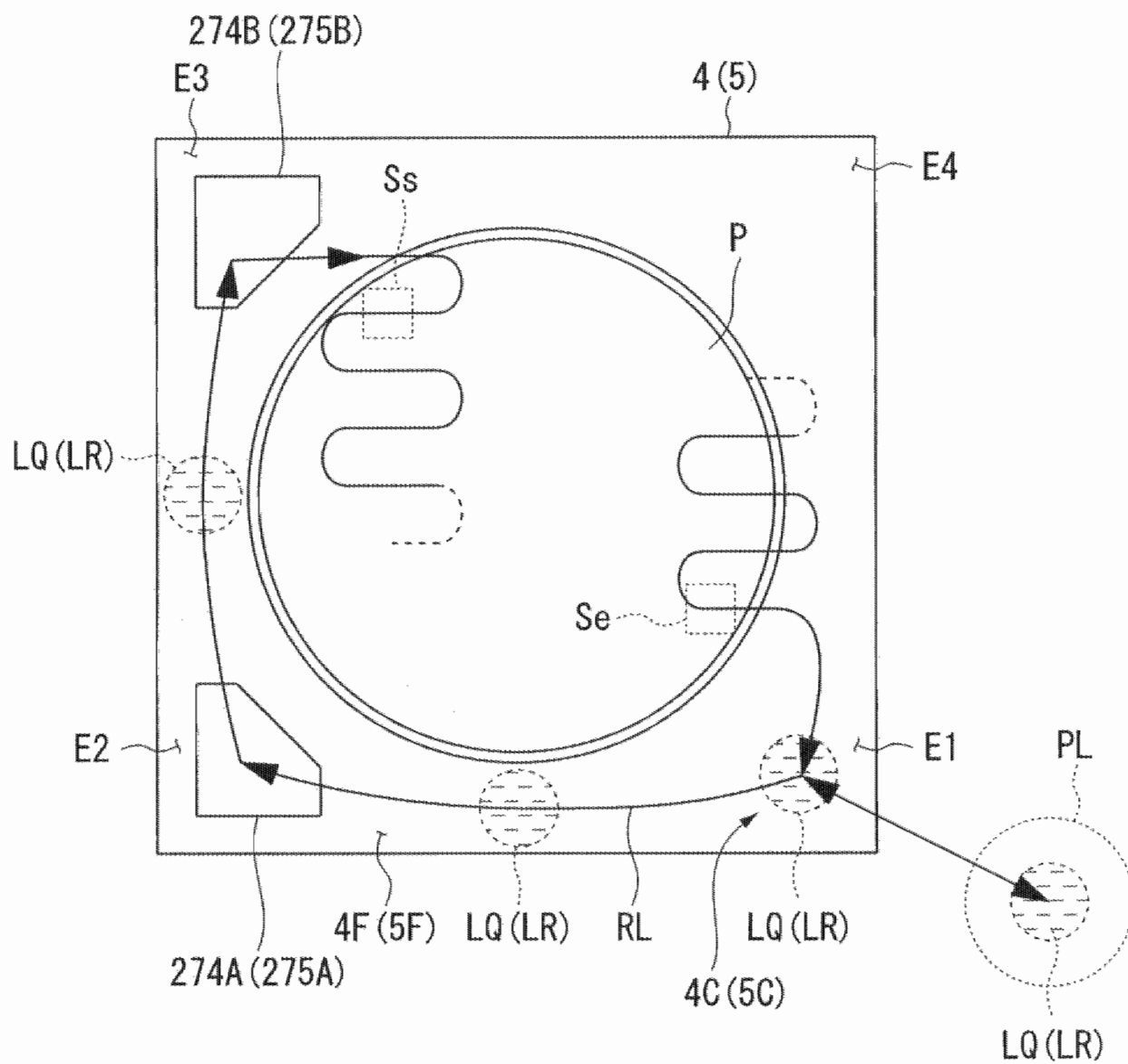


FIG. 80

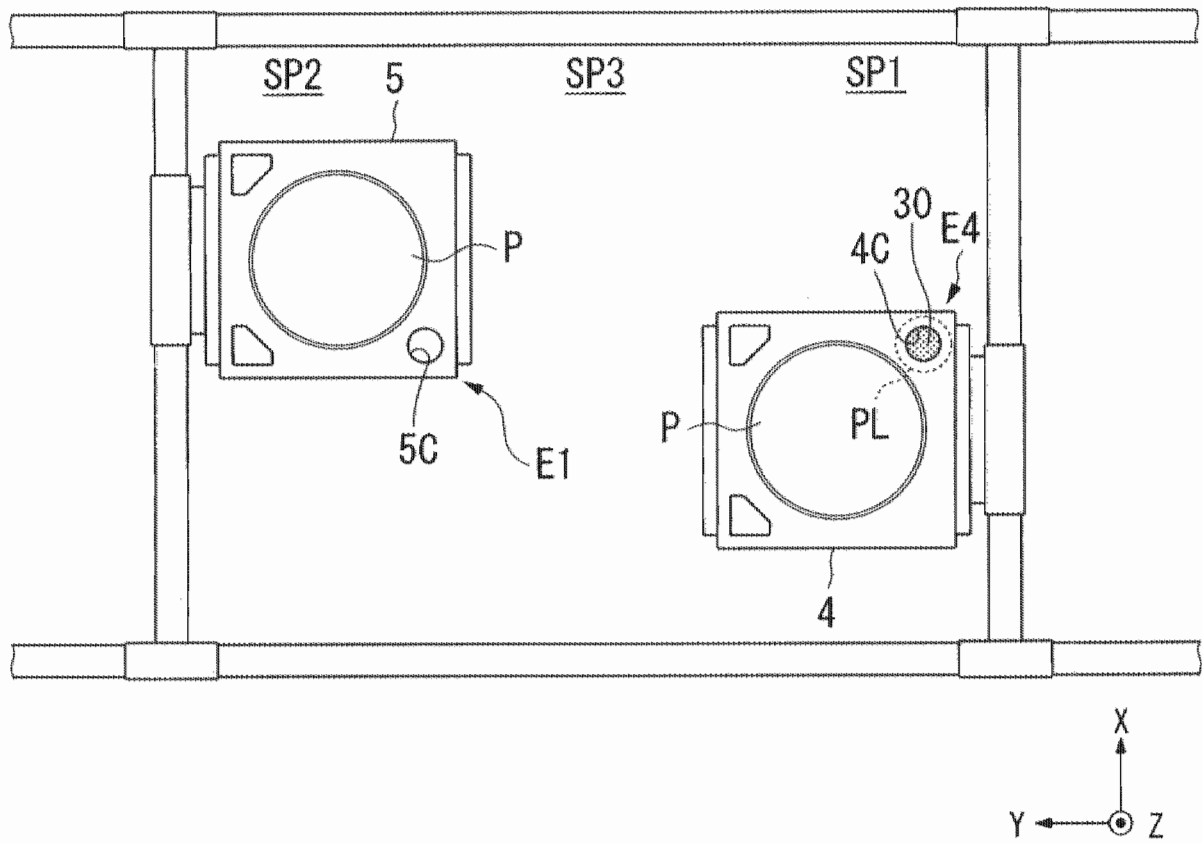


FIG. 81

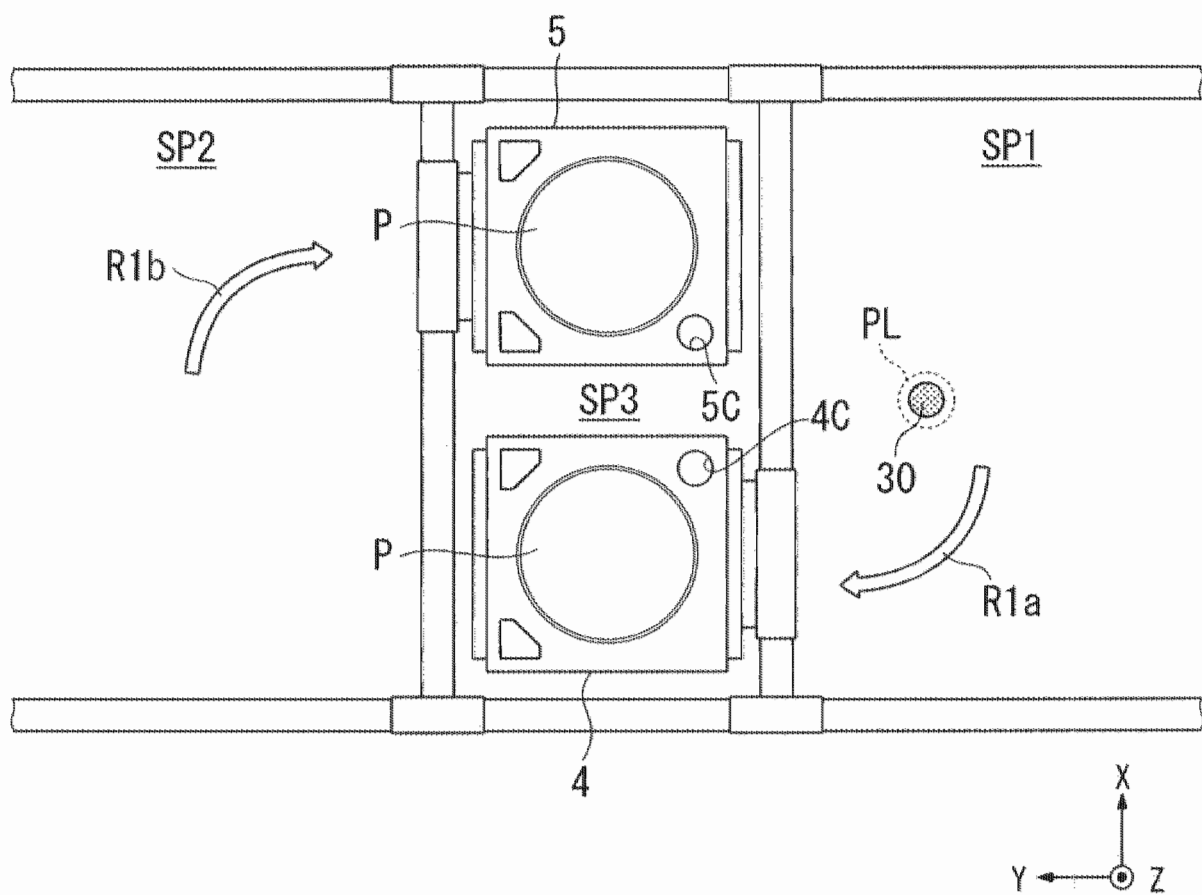


FIG. 82

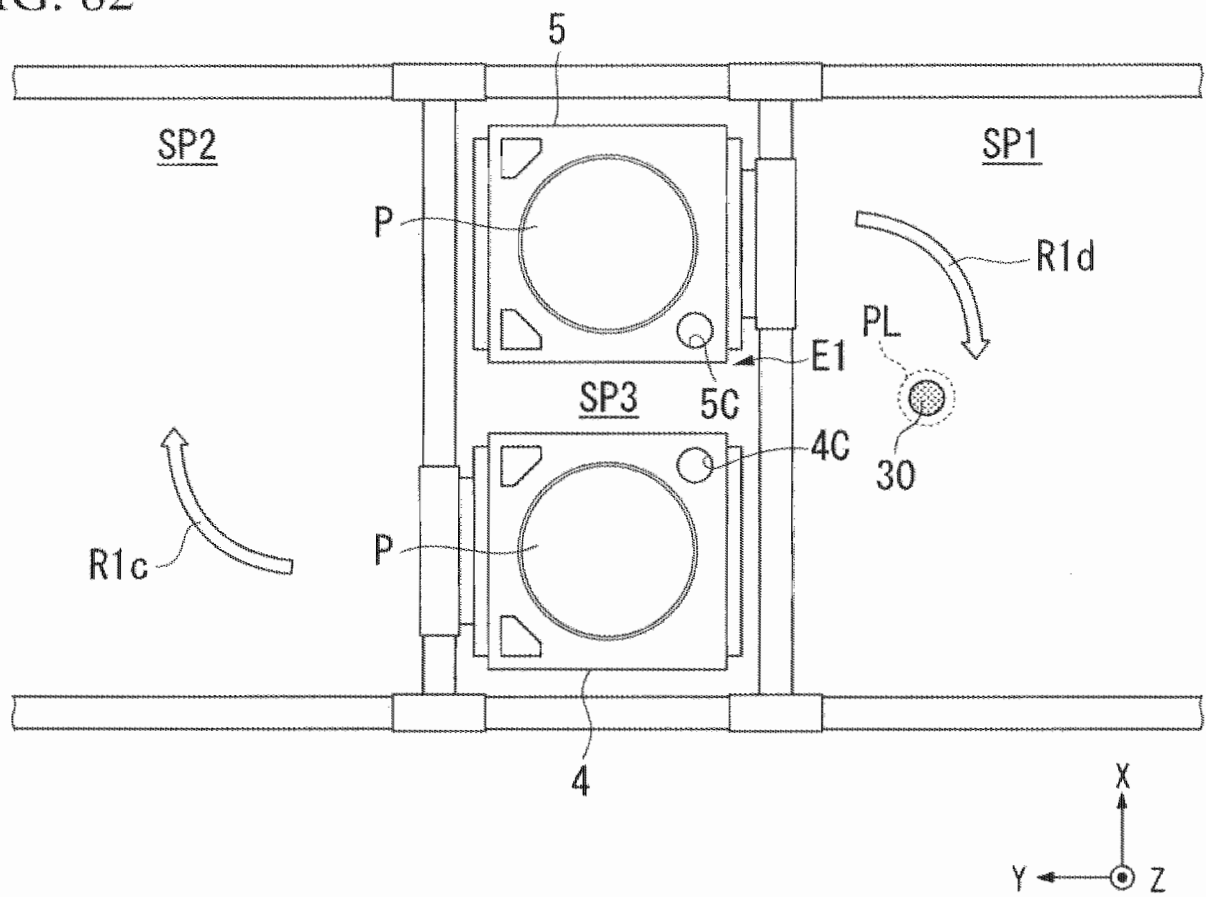


FIG. 83

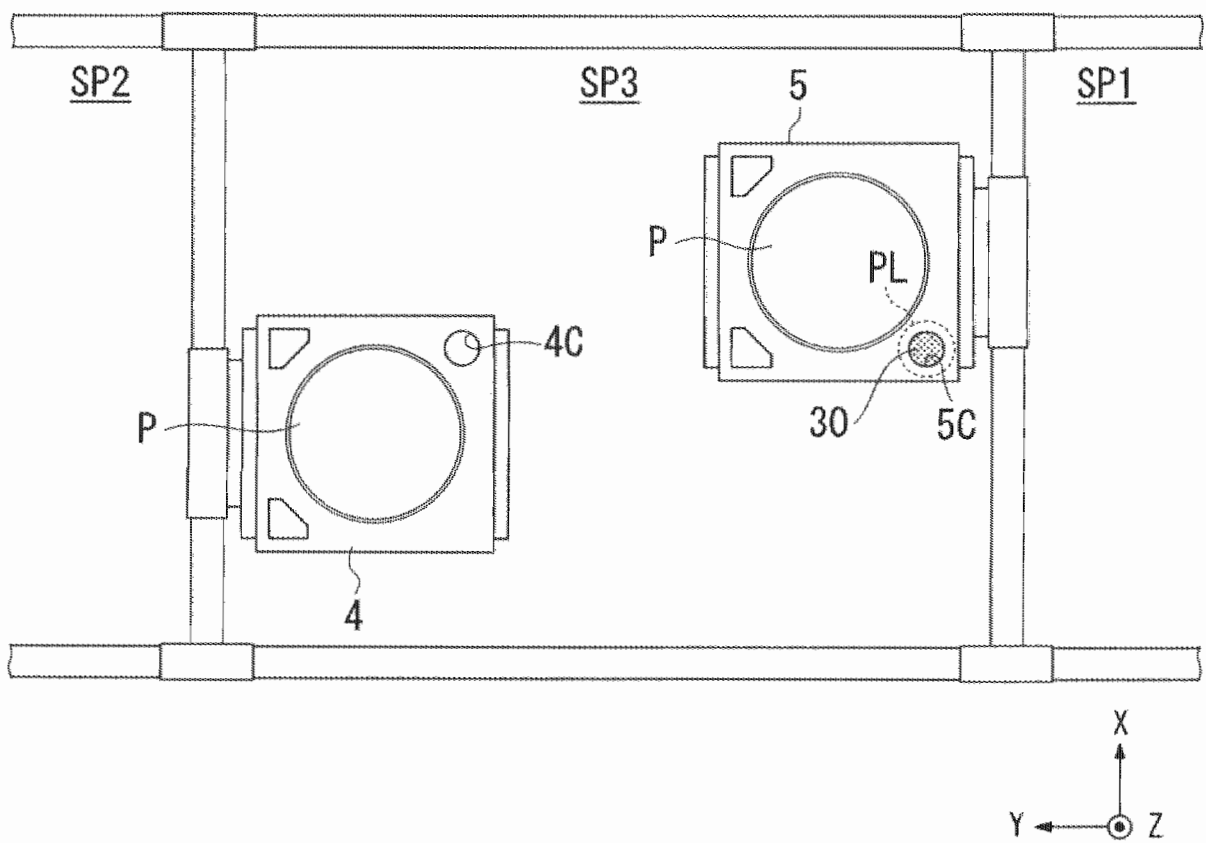


FIG. 84

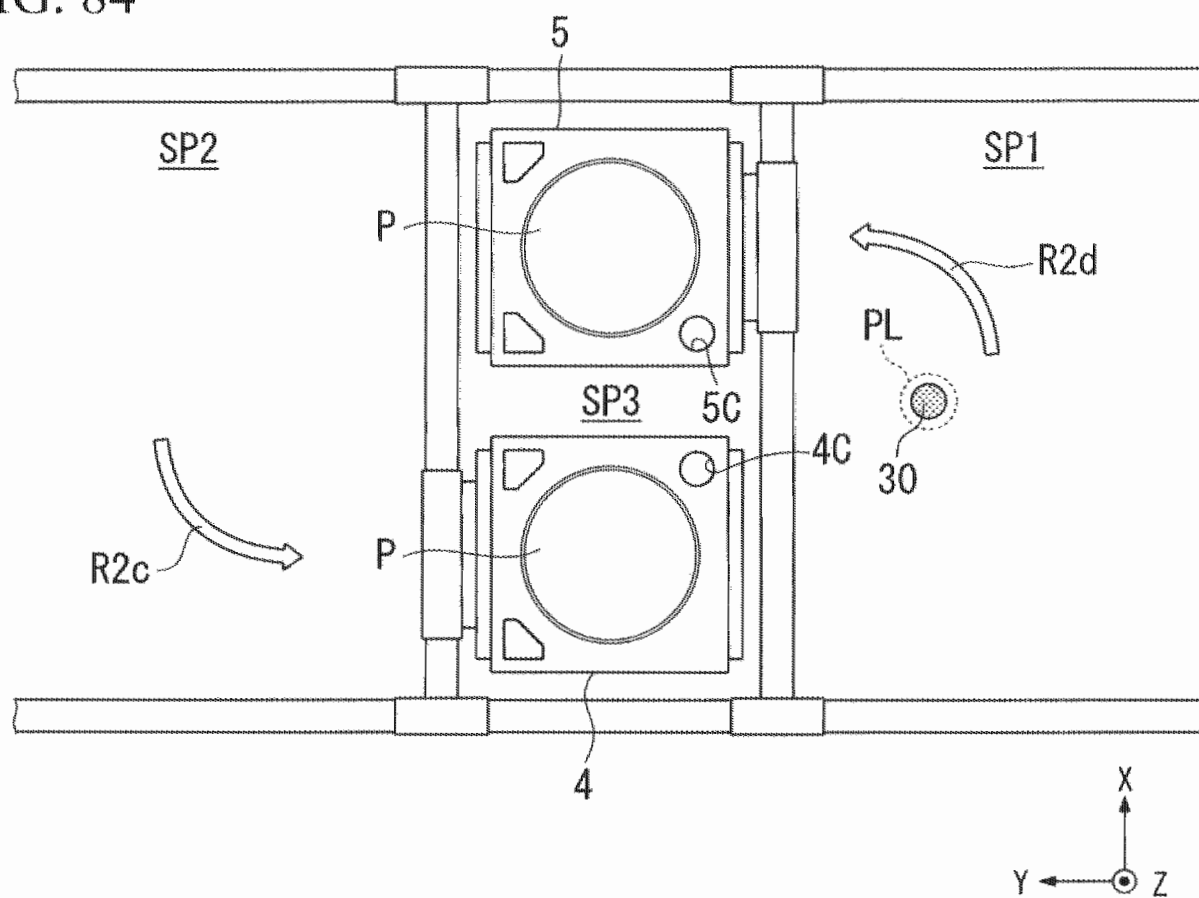


FIG. 85

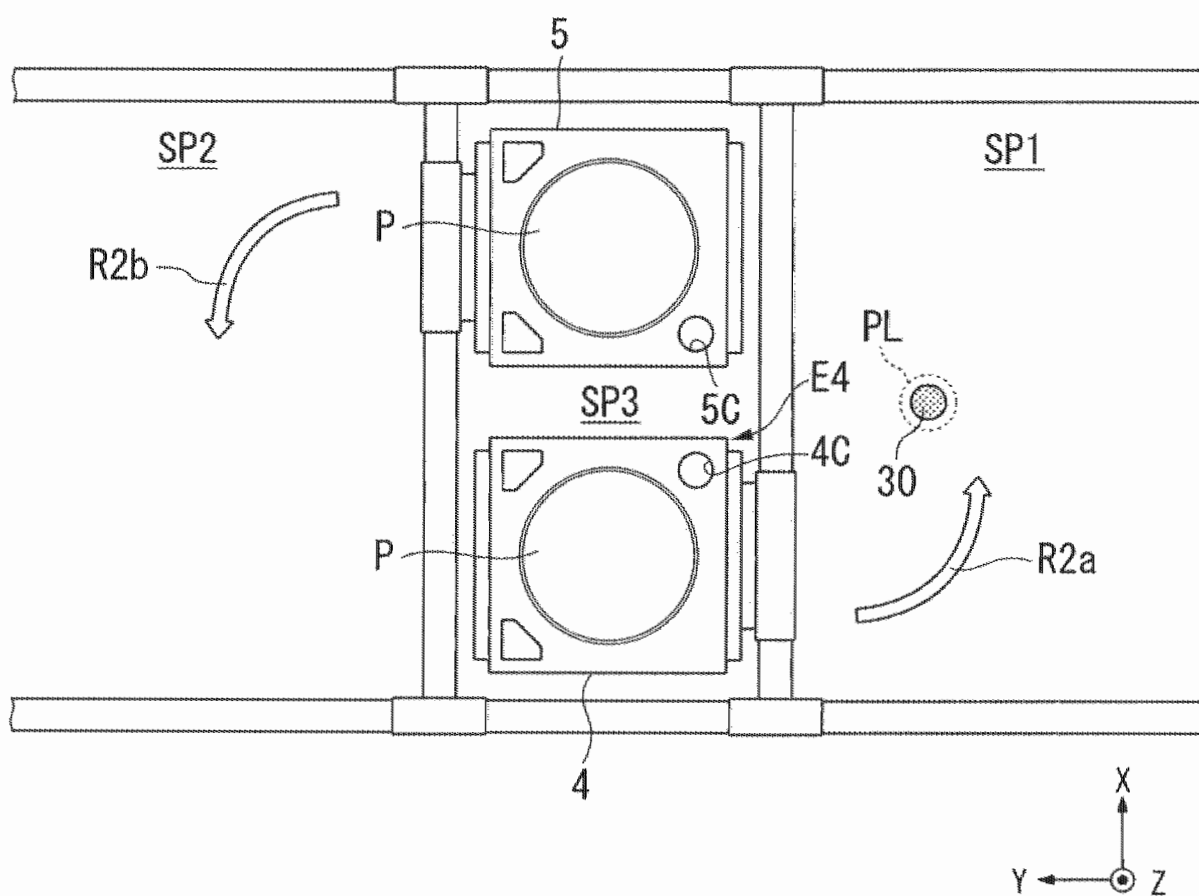


FIG. 86

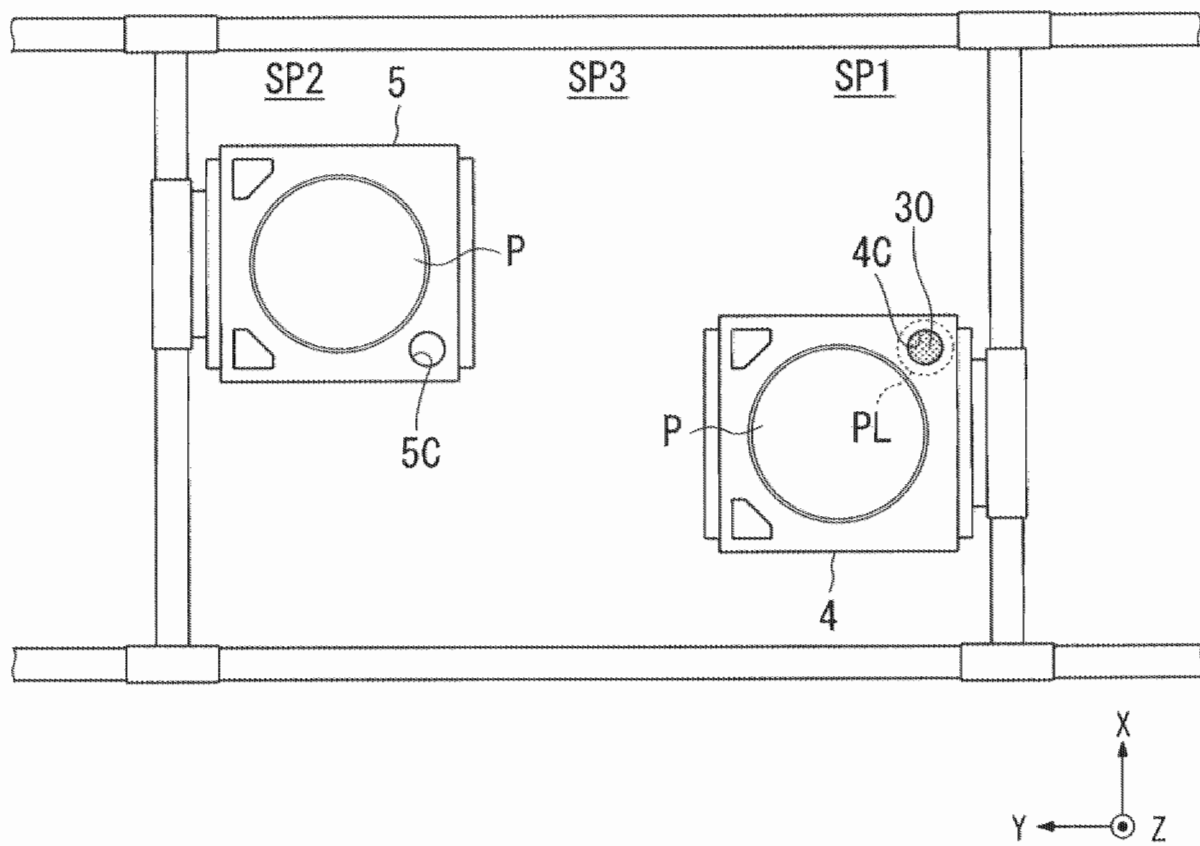
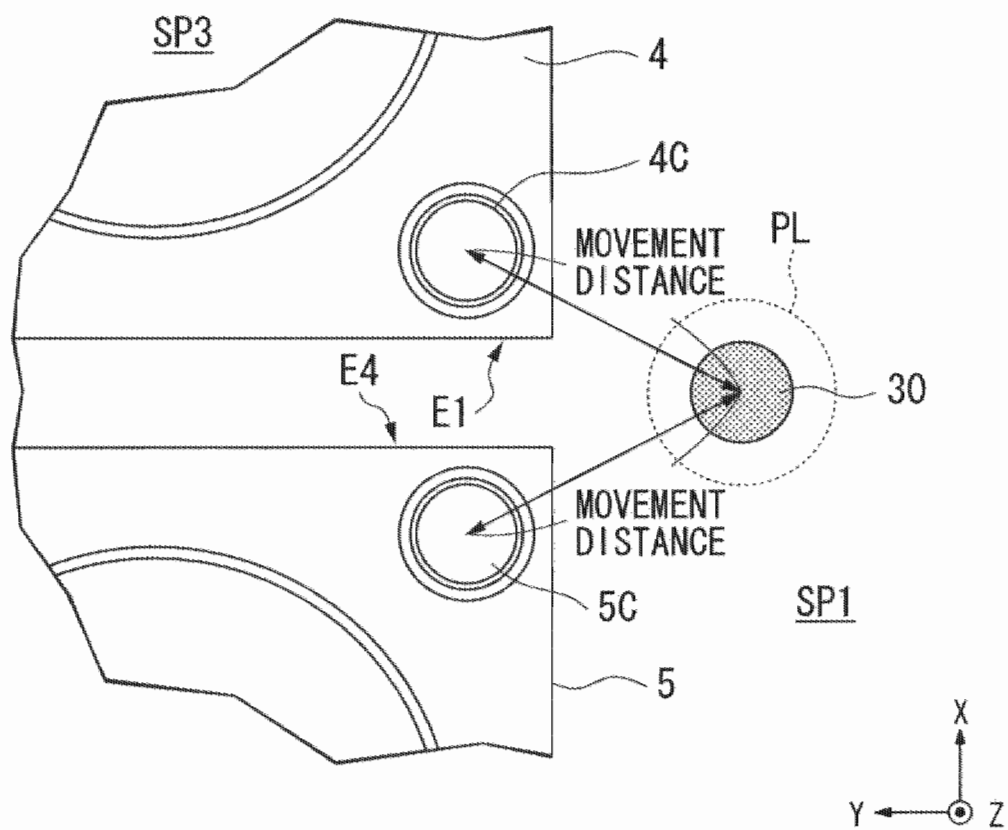


FIG. 87



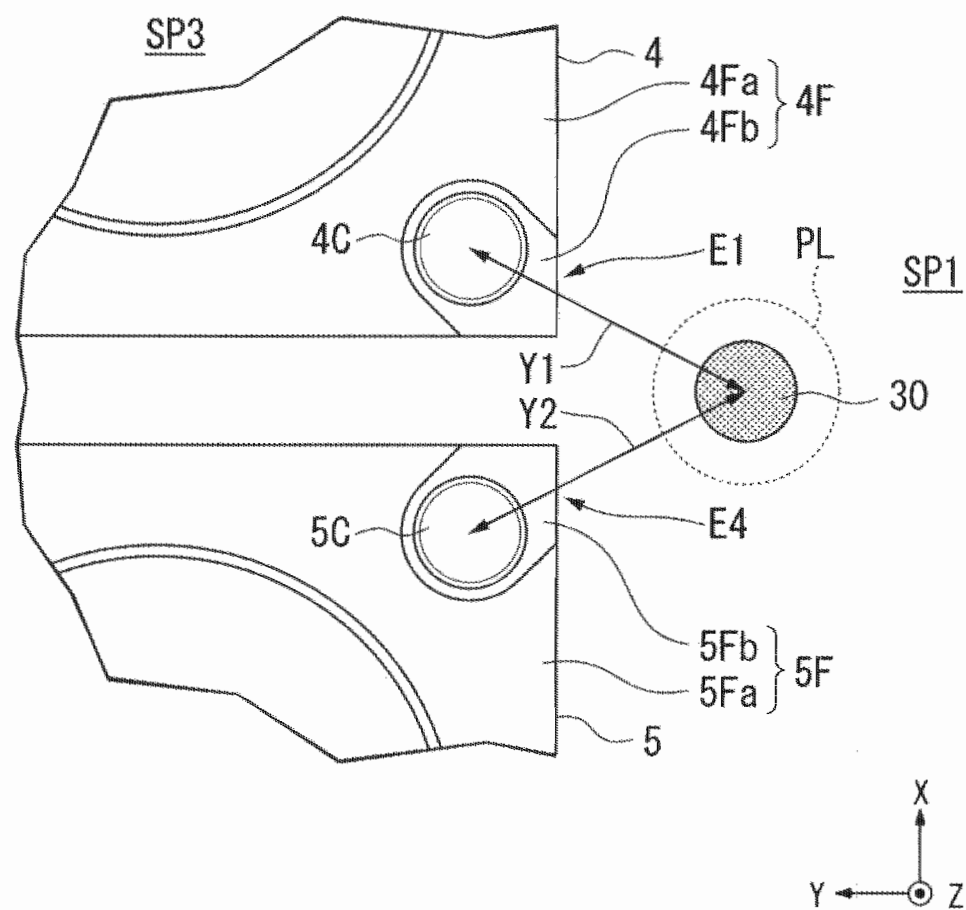


FIG. 90

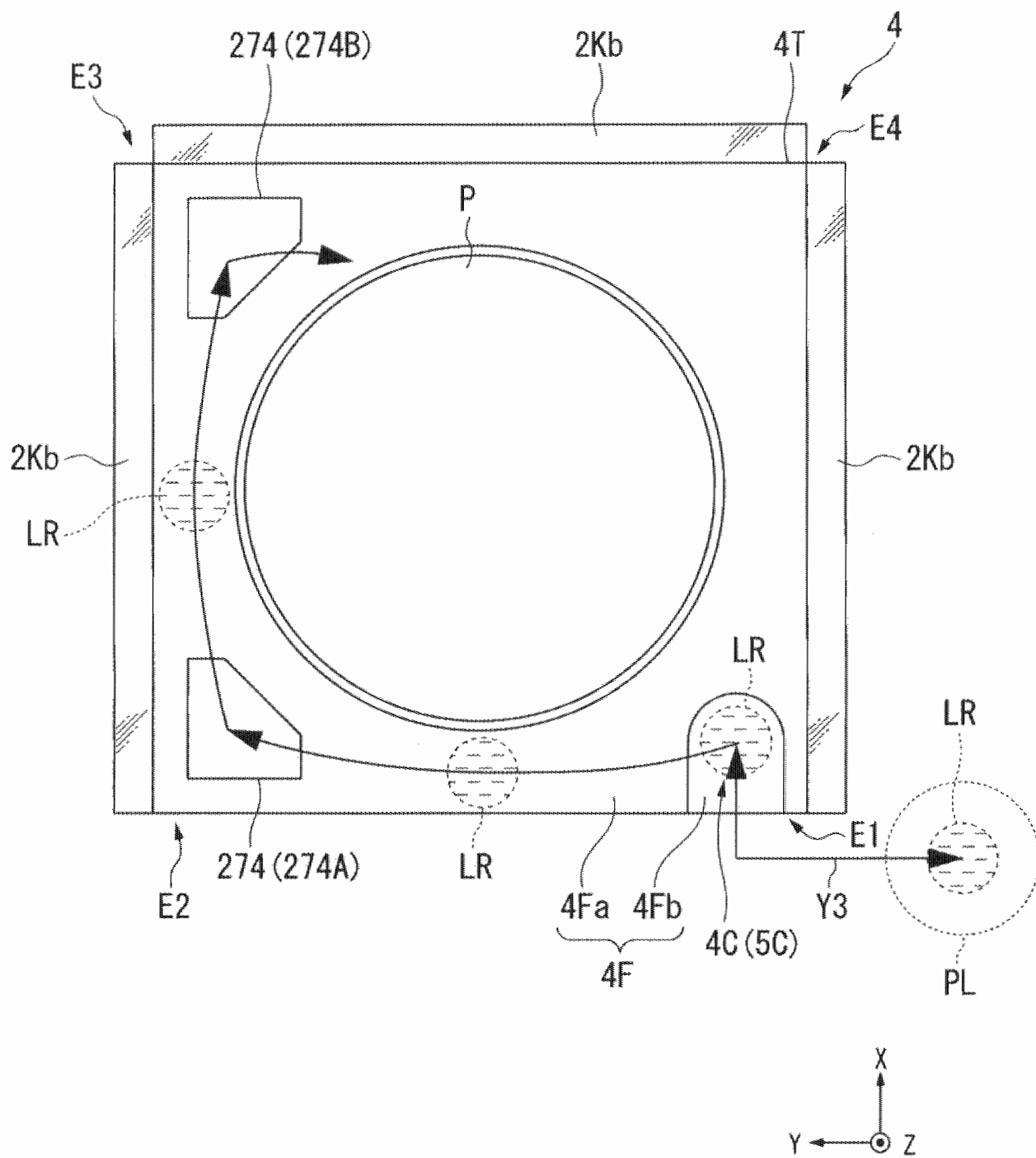


FIG. 91

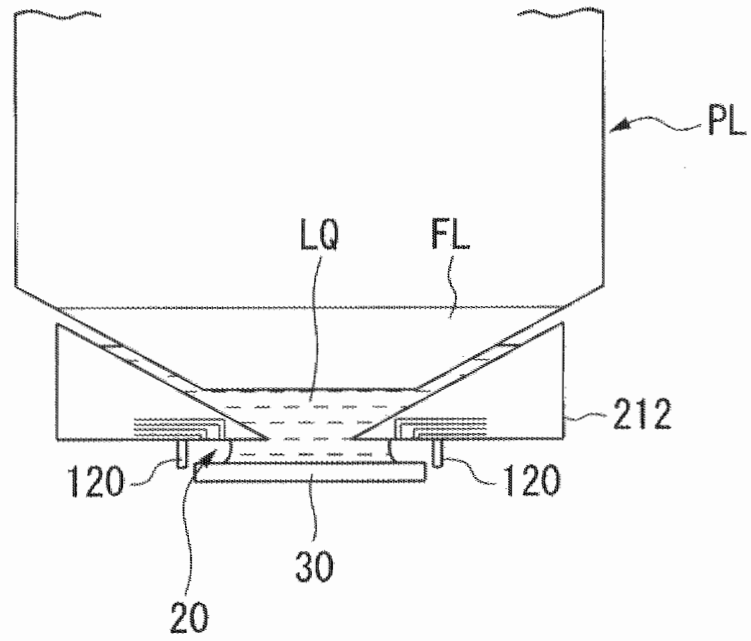


FIG. 92

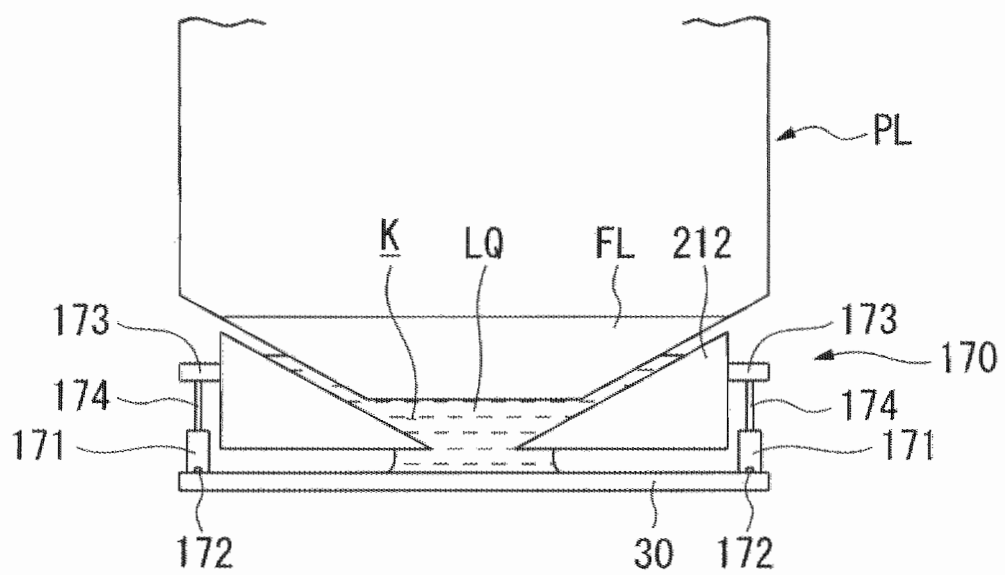


FIG. 93

