

SUPPORT FOR A SEMICONDUCTOR STRUCTURE

FIELD OF THE INVENTION

5 The present invention relates to a support for a semiconductor structure.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

10 Integrated devices are usually formed on substrates that mainly serve to hold them during their fabrication. However, the increase in the degree of integration and the expected performance of these devices has led to an increasingly tighter coupling of their performance and the
15 properties of the substrate on which they are formed. This is particularly the case for RF devices processing signals the frequency of which is comprised between about 3 kHz and 300 GHz, which are in particular employed in the telecommunications field (telephony, Wi-Fi, Bluetooth, etc.).

20 By way of example of device/substrate coupling, the electromagnetic fields generated by high-frequency signals propagating through the integrated devices penetrate into the bulk of the substrate and interact with any charge carriers
25 found there. This leads to coupling losses that consume some of the power of the signal and possibly to crosstalk between components.

 According to a second example of coupling, substrate
30 charge carriers may generate undesired harmonics, which may interfere with the signals propagating through the integrated devices and degrade device quality.

 These effects are especially observable when the
35 substrate employed comprises a buried insulating layer between a support and a useful layer on and in which the integrated devices are formed. Charges trapped in the insulating layer lead charges of complementary sign to accumulate under this

insulating layer, forming a conductive plane in the support. In this conductive plane, mobile charges are liable to interact strongly with the electromagnetic fields generated by the components of the useful layer.

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To prevent or limit this effect, it is known to insert, between the buried insulating layer and the support, directly under the insulating layer, a charge trapping layer, for example a layer of 1 to 5 microns of polycrystalline silicon. The boundaries of the grains forming the polycrystal then form charge traps, the trapped charge carriers possibly originating from the trapping layer itself or from the subjacent support. Thus, the formation of the conductive plane under the insulating layer is prevented. The fabrication of this type of substrate is for example described in documents FR2860341, FR2933233, FR2953640, US2015115480, US7268060 or US6544656.

In the presence of a trapping layer, the device/substrate coupling remains dependent on the strength of the interaction between the electromagnetic fields and the mobile charges in the support, and hence on the depth of penetration of these fields into this support. The density and/or mobility of these charges depends on the resistivity of the support.

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When the resistivity of the support is relatively high (and therefore charge density relatively low), higher than 1000 ohm.cm, a trapping layer of 1 to 5 microns in thickness may be suitable for limiting device/substrate coupling, even when the electromagnetic field penetrates deeply into the support. The integrity of the signals, and hence the radiofrequency (RF) performance of the devices integrated into the useful layer, is thus preserved.

In contrast, when the resistivity of the support is lower, lower than 1000 ohm.cm, or when the performance expected from the integrated device is high, it would be desirable to be able to form a very thick trapping layer, of greater than 5

microns, or even than 10 or 20 microns, in thickness, in order to shift the zone in which the charges are mobile deeper into the substrate and to limit the depth of penetration of the electromagnetic fields into this support. Interactions with
5 these electromagnetic fields could thus be prevented and the performance of devices integrated into the useful layer improved.

However, it has been observed that increasing the
10 thickness of a trapping layer beyond 5 microns does not always lead to the expected improvement in performance, in particular because this layer is liable to recrystallize during the heat treatments that it is liable to undergo. These heat treatments may correspond to those required to produce the substrate
15 itself or to those required to fabricate an RF integrated device in or on the useful layer of the substrate.

In order to prevent the recrystallization of this layer, document US9129800 envisages forming a silicon oxide layer
20 between the crystalline support and the charge trapping layer.

According to this document, this layer must necessarily have an initial thickness, before application of the heat treatments, that is relatively low, between 0.5 and 10 nm, in
25 order to have a final thickness, after application of the heat treatments, that is lower than 2 nm.

Stated otherwise, the initial thickness of this layer must be chosen according to the thermal budget to which the
30 substrate will be subjected so as not to negatively affect its RF performance.

When the insulating layer is absent for the entire duration of the heat treatment, the trapping layer is liable
35 to recrystallize, either partially or completely. Consequently, the lower grain boundary density or the large size of these grains decreases the trapping properties of the layer.

When the final thickness of the insulating oxide layer is higher than 2 nm, it is not transparent to the charges present in the support. These charges are therefore able to pass through the insulating layer only by tunnel effect, and are not able to diffuse into the polycrystalline layer and to be trapped therein. These charges thus accumulate in the support and a conductive plane forms under the insulating layer, which has a negative effect on the RF performance of the substrate.

Choosing a suitable initial thickness for this oxide is not straightforward. Specifically, the heat treatments to which a substrate may be subjected are not always known in advance of its fabrication, in particular those which are applied during the formation of an integrated device. However, these heat treatments may affect the quality or the thickness of this silicon dioxide insulating layer, for example by dissolution. In this regard, it has been observed that the heat treatments in device fabrication can have high thermal budgets, which may have a significant effect on the quality of the trapping layer in the event that the oxide layer has not been chosen with a suitable thickness. This may thus be a thermal processing operation at 1200°C for several minutes as is the case when it is for the purpose of introducing strain into zones of the useful layer using a buried oxide creep technique or during thermal processing operations for dopant activation.

The teaching of the cited prior art document is therefore not straightforward to implement without having knowledge of the total thermal budget that the trapping layer will receive over the course of all of the steps of fabricating the substrate and the integrated devices that are to be formed on this substrate.

The present invention aims to overcome all or some of the aforementioned drawbacks.

BRIEF DESCRIPTION OF THE INVENTION

With a view to achieving this aim, one subject of the invention provides, within its widest accepted form, a support for a semiconductor structure comprising:

- a base substrate;
- a first silicon dioxide insulating layer positioned on the base substrate and having a thickness greater than 20 nm;
- a charge trapping layer having a resistivity higher than 1000 ohm.cm and a thickness greater than 5 microns positioned on the first insulating layer.

The first insulating layer allows a thick trapping layer to be formed, this trapping layer exhibiting excellent charge trapping properties and having a low likelihood of recrystallizing. Unexpectedly, the inventors of the present application have observed that the decrease in RF performance that could be caused by this insulating layer was largely compensated for by the benefits brought by the thick trapping layer, the formation of which it made possible.

According to other advantageous and non-limiting features of the invention, which may be implemented alone or in any technically feasible combination:

- the trapping layer comprises polycrystalline silicon;
- the polycrystalline silicon is rich in carbon;
- the polycrystalline silicon consists of silicon grains having dimensions comprised between 10 nm and 900 nm;
- the trapping layer comprises amorphous or porous silicon;
- the trapping layer has a thickness greater than 10 microns;

- the trapping layer is formed from alternating layers of polycrystalline silicon and silicon dioxide;
- the base substrate has a resistivity lower than 1000 ohm.cm or than 500 ohm.cm or than 10 ohm.cm;
- the base substrate has a resistivity higher than 1000 ohm.cm or than 10k ohm.cm;
- the base substrate is made of silicon, of quartz, of glass or of sapphire;
- the support comprises a second insulating layer positioned on the trapping layer.

According to another aspect, the subject of the invention provides a semiconductor structure comprising:

- a support such as described above;
- an insulating layer on this support;
- a useful layer on the insulating layer.

The useful layer may comprise at least one integrated device.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following detailed description of the invention, which description is given with reference to the appended figures, in which:

- Figure 1 schematically shows a support for a semiconductor structure according to the invention;
- Figure 2 shows a semiconductor-on-insulator substrate including a support according to the invention;

- Figure 3 presents, in the form of a graph, experimental measurements made on a support according to the invention.

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DETAILED DESCRIPTION OF THE INVENTION

Figure 1 schematically shows a support 1 for a semiconductor structure according to the invention. The support 1 may take the form of a circular wafer of standardized size, for example of 200 mm or 300 mm or even 450 mm in diameter. However, the invention is in no way limited to these dimensions or to this shape.

Thus, in the case where the semiconductor structure is to be a finished or semi-finished integrated device, the support 1 will take the form of a block of material of rectangular or square longitudinal cross section the dimensions of which, from a few millimetres to a few centimetres, correspond to the dimensions of the integrated device.

The support 1 comprises a base substrate 3, which is typically a few hundred microns in thickness. Preferably, and especially when the support 1 is intended to receive a semiconductor structure for which the expected RF performance is high, the base substrate has a high resistivity, higher than 1000 ohm.centimetre, and even more preferably higher than 3000 ohm.centimetre. The density of charges, i.e. holes or electrons, that are liable to move in the base substrate is thus limited. However, the invention is not limited to a base substrate having such a resistivity, and it also provides advantages in terms of RF performance when the base substrate has a more usual resistivity, of about a few hundred ohm.centimetres, for example lower than 1000 ohm.cm, or than 500 ohm.cm or than 10 ohm.cm.

For reasons of availability and cost, the base substrate 3 is preferably made of monocrystalline silicon. It may for example be a CZ substrate containing a small amount of interstitial oxygen, this type of substrate, as is well known
5 per se, having a resistivity that may be higher than 1000 ohm.centimetre. The base substrate may alternatively be formed from another material: it may for example be made of sapphire, of glass, of quartz, of silicon carbide, etc.

10 The support 1 also includes, positioned on and making direct contact with the base substrate 3, a first silicon dioxide insulating layer 2a. The first insulating layer 2a has a thickness greater than 20 nm, for example comprised between 20 nm and 20 microns. It may be obtained by oxidation of the
15 base substrate 3 or by deposition on this substrate. In order to limit the time and cost required to form the first insulating layer, its thickness may be chosen so that it is comprised between 100 and 200 nm, such as for example 145 nm.

20 Above a thickness of 20 nm, the first insulating layer is stable with temperature, even for high thermal budgets. It may in particular be exposed to temperatures higher than or equal to 1200°C for a duration of several hours without breaking down, for example by dissolution.

25 The support 1 also includes, positioned on and making direct contact with the first insulating layer 2a, a trapping layer 2. The trapping layer 2 has a resistivity higher than 1000 ohm.cm, preferably higher than 10 kohm.cm. As was
30 mentioned above in detail in the introduction of the present application, the function of the trapping layer is to trap any charge carriers present in the support 1 and to limit their mobility. This is especially the case when the support 1 is provided with a semiconductor structure that emits an
35 electromagnetic field that penetrates into the support and that is therefore liable to interact with these charges and to make them mobile.

The trapping layer 2 may, in general, be formed from a non-crystalline semiconductor layer having structural defects such as dislocations, grain boundaries, amorphous zones, interstices, inclusions, pores, etc. The structural defects
5 form traps for any charges flowing through the material, for example at the site of incomplete or dangling chemical bonds. Conduction is thus prevented in the trapping layer, which consequently exhibits high resistivity. Since the trapping layer does not make direct contact with the support but with
10 the amorphous insulating layer, the trapping properties of this layer may be conserved even when the support undergoes a very high heat treatment. The structural defects are unlikely to undergo recrystallization.

15 For the same reasons of availability and cost which were mentioned above, the trapping layer 2 is preferably made of polycrystalline silicon. However, it may be formed from or comprise another polycrystalline semiconductor material. Alternatively, the trapping layer 2 may be formed from or
20 comprise amorphous or porous silicon.

It is also possible to envisage inserting at least one intermediate layer into the trapping layer 2, for example a carbon layer or a layer composed of a carbon-silicon alloy.
25 The intermediate layer may also comprise, or be formed from, silicon oxide or silicon nitride. In this case, the trapping layer 2 is then formed from alternating layers of polycrystalline silicon (or of another material, or of an amorphous or porous material) and intermediate layers of a
30 different nature (of silicon dioxide or nitride, of carbon, etc.).

In any case, the trapping layer 2 has a high resistivity higher than 1000 ohm.centimetre. To this end, the
35 trapping layer 2 is not intentionally doped, i.e. it has a charge carrier dopant concentration lower than 10^{14} atoms per cubic centimetre. It may be rich in nitrogen or in carbon in order to improve its resistivity characteristic.

The fabrication of the trapping layer 2 on the base substrate 3 provided with the first insulating layer 2a is particularly straightforward and achievable using industry-standard deposition equipment. It may thus involve RPCVD (remote plasma-enhanced chemical vapour deposition) or PECVD (plasma-enhanced chemical vapour deposition). It may also involve LPCVD (low-pressure chemical vapour deposition).

Unexpectedly, the inventors of the present application have observed that a trapping layer 2 based on polycrystalline silicon produced on the first insulating layer 2a and having a thickness greater than 20 nm was formed from grains the dimensions of which, typically comprised between 10 and 900 nm, were particularly suitable for effective charge trapping. Moreover, the dimensions of these grains are relatively constant throughout the thickness of the trapping layer 2, even when the thickness of the latter is substantial. These properties are also conserved after the trapping layer 2 has been exposed to a thermal budget, even to a high thermal budget.

It has been observed that grain size directly affects the RF performance of the support in two ways. Firstly, larger grains lead to a lower density of grain boundaries in the material. Since these boundaries form a prime zone of charge trapping, trap density is decreased.

Furthermore, the grains also form a confining space for the charge carriers that reside therein. In grains of substantial size, for example of the order of the size of an integrated device, the charges behave, as seen by the device, as in a defect-free material.

These two aspects combine to decrease the RF performance of the support, when the grains of the polycrystal of the trapping layer 2 are of substantial sizes.

Complementary studies have shown that the size of the grains must preferably be comprised between 100 nm (below which their thermal stability is no longer ensured and hence there is a risk that they will recrystallize with temperature) and 1000 nm (above which the RF performance of the support is affected).

A support 1 according to the invention may therefore have a thick trapping layer 2, having a thickness greater than 5 microns, and potentially reaching 10 microns or 20 microns, comprising a polycrystalline silicon material formed from grains the size of which is comprised between 10 and 900 nm. As mentioned above, provision may be made to insert one or a plurality of intermediate layers into the trapping layer in order to limit the size of the grains of each polycrystalline layer, this tending to increase with thickness. In order to promote the formation of small grains, it is thus possible to choose to limit the thickness of the polycrystalline layers positioned between two intermediate layers to 1 micron in thickness or less.

It should be noted that the cited prior art document recommends against placing a thick first insulating layer 2a between the trapping layer 2 and the base substrate 3, as recommended by the present invention. Specifically, and according to this document, the presence of charges in this insulator leads to the formation of a conductive plane consisting of charges of complementary sign in the base substrate 3, under the first insulating layer 2a. This conductive plane affects the radiofrequency performance of the support 1.

Surprisingly, the inventors of the present application have observed however that this loss of performance was in fact less than the gain obtained by forming a trapping layer 2 having a thickness greater than 5 microns, so that the total RF performance of the support 1 is overall improved thereby.

By forming a trapping layer having a thickness greater than 5 microns, only the electromagnetic fields penetrating most deeply into the bulk of the base substrate 3 are liable to affect the mobile charges present in the substrate. These fields constitute only a minor portion of the fields penetrating into the support, in particular when the signals from which they originate have a very high frequency, for example higher than a gigahertz.

The accumulation of charges under the first insulating layer 2a and the interaction of these charges with the electromagnetic fields penetrating sufficiently deeply into the support leads to a decrease in RF performance. However, unexpectedly, this decrease is largely compensated for by the increase in the RF performance related to the substantial thickness, greater than 5 microns, of the trapping layer 2.

The graph of Figure 3 presents the results of a series of experiments and simulations prepared by the applicant.

A plurality of supports having different characteristics and in accordance with the invention have been prepared. These supports comprise a base substrate consisting of a silicon wafer having a diameter of 300 mm and a resistivity of 17,6 k.ohms . The base substrates have each been provided with a silicon dioxide insulating layer having a thickness of 145 nm by thermal oxidation. A trapping layer made of polycrystalline silicon has been formed on this insulating layer by RPCVD, this layer having a thickness of 2 microns, 7 microns, and 16 microns.

A characterization measurement, referred to as a second harmonic distortion measurement, has then been performed on each of the supports prepared in this way. This measurement is made at 900 MHz. To this end, a silicon dioxide layer and coplanar metallic lines have been formed on each support.

This characterization measurement, a detailed description of which will be found in the document entitled "White paper - RF SOI wafer characterisation", January 2015, published by Soitec and in the document US2015/0168326, is particularly relevant since it is very representative of the performance of an RF integrated device that would be formed on the characterized support.

The axis of the abscissae of the graph of Figure 3 represents the thickness "e" of the trapping layer 2, in microns. The axis of the ordinates represents the second harmonic distortion measurement (denoted by HD2) in dBm.

The six measurements made have been represented by points on the graph of Figure 3. These measurement points have made it possible to calibrate a simulation of the second harmonic distortion measurement for a support having a base substrate of determined resistivity and having a polycrystalline silicon trapping layer of determined thickness. The simulation measurements are represented on the graph of Figure 3 by solid lines for various resistivity values of the base substrate.

It has been observed that the RF performance of all of the supports is improved when the thickness of the polycrystalline silicon layer increases. More specifically, performance is notably increased when the thickness of the trapping layer is greater than 5 microns. The presence of the insulating layer does not limit the level of performance that may be reached. These levels of performances are expected to be stable regardless of the temperature to which the support could be exposed, since the insulating layer prevents the recrystallization of the polycrystalline trapping layer.

Returning to the description of the support 1 shown in Figure 1, it is optionally possible to provide a second insulating layer 4 on the trapping layer 2 and in direct contact therewith, in order to facilitate the assembly of the

support 1 with a semiconductor structure. This second insulating layer 4 may be formed by deposition or by oxidation of the trapping layer 2. Provision may be made for a polishing step before and/or after the formation of the second
5 insulating layer 4, in order to improve the quality of this assembly.

As mentioned above, the support 1 is intended to receive a semiconductor structure on the side of the trapping
10 layer 2.

This structure may be formed in multiple ways on the support 1, but advantageously this formation comprises a step of transferring a useful layer 5 to the support.

15 As is well known per se, this transfer is usually achieved by bonding the face of a donor substrate to the support 1. The latter may or may not be provided with the insulating layer 4. In the same way, the donor substrate may have been provided beforehand with another insulating layer 6
20 of the same nature or of a different nature to the second insulating layer 4. It may for example be a silicon oxide or silicon nitride. The assembly may undergo a strengthening heat treatment, even one having a high thermal budget, since the trapping layer 2 of the support is not liable to recrystallize
25 by virtue of the presence of the insulating layer 2a. The strengthening heat treatment may correspond to thermal processing for several hours at 1200°C, which is generally required for fully strengthening a bond bringing two silicon oxide layers into contact.

30 After this bonding step, the thickness of the donor substrate is decreased to form the useful layer 5. This decreasing step may be a step of mechanical or chemical thinning. It may also be a fracture level with a fragile zone
35 introduced beforehand into the donor substrate, for example according to the principles of the Smart Cut™ technology.

A sequence of steps for finishing the useful layer 5, such as a polishing step, a heat treatment under a reducing or inert atmosphere, and a sacrificial oxidation may be carried out after the thickness-decreasing step.

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When the donor substrate is a simple semiconductor substrate, i.e. one that comprises no integrated devices, a semiconductor-on-insulator substrate is thus formed, in which, as is shown in Figure 3, the useful layer 5 is a virgin semiconductor layer comprising the support of the invention. The substrate may then be used to form integrated devices.

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When the donor substrate has been processed beforehand to form integrated devices on its surface, a useful layer 5 that comprises these devices is obtained at the end of this process.

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Of course, the invention is not limited to the described embodiment and variant embodiments may be rendered therefrom without departing from the scope of the invention such as defined by the claims.

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The expression "semiconductor structure" irrespectively refers to an integrated device whether the latter be formed from semiconductor materials or not. For example, it may be a surface or bulk acoustic wave type device, typically produced on and in a layer made of piezoelectric material, such as lithium tantalate.

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The expression "semiconductor structure" also refers to a layer (or a plurality of layers) of virgin device material, whether based on semiconductor materials or not, and in which integrated devices may be formed.

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CLAIMS

1. Support (1) for a semiconductor structure comprising:
 - a base substrate (3);
 - 5 - a first silicon dioxide insulating layer (2a) positioned on the base substrate (3) and having a thickness greater than 20 nm;
 - a charge trapping layer (2) having a resistivity higher than 1000 ohm.cm and a thickness greater than 5 microns
 - 10 positioned on the first insulating layer (2a).
2. Support (1) according to the preceding claim, in which the trapping layer (2) comprises polycrystalline silicon.
- 15 3. Support (1) according to the preceding claim, in which the polycrystalline silicon is rich in carbon.
4. Support (1) according to either of the preceding claims, in which the polycrystalline silicon consists of silicon grains
- 20 having dimensions comprised between 10 and 900 nm.
5. Support (1) according to Claim 1, in which the trapping layer (2) comprises amorphous or porous silicon.
- 25 6. Support (1) according to one of the preceding claims, in which the trapping layer (2) has a thickness greater than 10 microns.
7. Support (1) according to one of Claims 1 to 4, in which the
- 30 trapping layer (2) is formed from alternating layers of polycrystalline silicon and silicon dioxide.
8. Support (1) according to one of the preceding claims, in which the base substrate (3) has a resistivity lower than
- 35 1000 ohm.cm or than 500 ohm.cm or than 10 ohm.cm.

9. Support (1) according to one of Claims 1 to 7, in which the base substrate has a resistivity higher than 1000 ohm.cm or than 10k ohm.cm.
- 5 10. Support (1) according to one of the preceding claims, in which the base substrate (3) is made of silicon.
11. Support (1) according to one of Claims 1 to 9, in which the base substrate (3) is made of quartz, of glass or of
10 sapphire.
12. Support (1) according to one of the preceding claims, comprising a second insulating layer (4) positioned on the trapping layer (2).
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13. Semiconductor structure comprising:
- a support (1) according to one of Claims 1 to 11;
 - an insulating layer (4, 6) on the support (1);
 - a useful layer (5) on the insulating layer (4, 6).
- 20
14. Semiconductor structure according to the preceding claim, in which the useful layer (5) comprises at least one integrated device.