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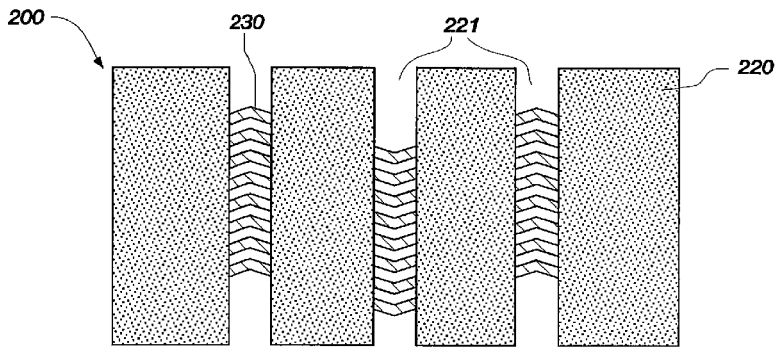


FIG. 9

(57) Abstract: Methods of pitch doubling of asymmetric features and semiconductor structures including the same are disclosed. In one embodiment, a single photolithography mask may be used to pitch double three features, for example, of a DRAM array. In one embodiment, two wordlines and a grounded gate over field may be pitch doubled. Semiconductor structures including such features are also disclosed.

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