CLAIMS

What is claimed is:

1. A semiconductor device package, comprising:

an interposer substrate comprising a dielectric member, a plurality of terminals proximate and extending along at least one peripheral edge thereof on one side thereof and an array of lands proximate and extending along a same at least one peripheral edge on an opposing side of the interposer substrate, terminals of the plurality being respectively electrically connected to lands of the land array through conductive via structures extending through the dielectric member, the interposer substrate further comprising a two-dimensional array of pads substantially centrally located on the opposing side of the interposer substrate, and wherein terminals of the plurality are respectively electrically connected to pads of the two-dimensional pad array;

at least one semiconductor die mounted by a back side thereof to the one side of the interposer substrate and having a plurality of bond pads on an active surface thereof proximate and extending along at least one peripheral edge thereof adjacent the at least one peripheral edge of the interposer substrate respectively electrically connected to the plurality of terminals; and

an encapsulant structure disposed over the at least one semiconductor die and the one side of the interposer substrate;

2. The semiconductor device package of claim 1, further comprising at least one electrical component mechanically and electrically connected to the interposer substrate through pads of the two-dimensional pad array.

3. The semiconductor device package of claim 2, wherein the at least one electrical component is selected from the group consisting of passive components and active components.

4. The semiconductor device package of claim 2, further comprising discrete conductive bumps disposed on at least some of the pads of the two-dimensional pad array, the at least one electrical component being connected to the pads through some of the discrete conductive elements.

5. The semiconductor device package of claim 2, further comprising discrete conductive bumps disposed on at least some of the pads of the two-dimensional pad array.

6. The semiconductor device package of claim 2, further comprising a lead frame comprising a plurality of lead fingers having inner ends respectively disposed over lands of the land array on the opposing side of the interposer substrate and mechanically and electrically connected thereto.

7. The semiconductor device package of claim 6, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and an inner end of at least one lead finger.

8. The semiconductor device package of claim 6, wherein at least the inner ends of the lead fingers and the opposing side of the interposer substrate are covered with a dielectric material.

9. The semiconductor device package of claim 6, wherein the at least one electrical component is covered with a dielectric material.

10. The semiconductor device package of claim 2, further comprising:

a carrier substrate to which the land grid array package is affixed by a side thereof opposite the interposer substrate, the carrier substrate including a plurality of conductive pads on a surface thereof to which the land grid array package is affixed; and

wire bonds extending between lands of the land array and conductive pads of the plurality of conductive pads.

11. The semiconductor device package of claim 10, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate.

12. The semiconductor device package of claim 11, wherein the wire bond bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate comprises two segments joined at an electrically isolated pad of the two-dimensional pad array.

13. The semiconductor device package of claim 10, wherein at least the lands of the land array, the wire bonds and the conductive pads are covered with a dielectric material.

14. The semiconductor device package of claim 10, wherein the at least one electrical component is covered with a dielectric material.

15. The semiconductor device package of claim 1, wherein the at least one peripheral edge of each of the interposer substrate and the at least one semiconductor die comprises two opposing peripheral edges.

16. The semiconductor device package of claim 1, wherein the plurality of bond pads are electrically connected to the plurality of terminals with wire bonds.

17. The semiconductor device package of claim 1, wherein the at least one semiconductor die comprises two semiconductor dice, one semiconductor die being mounted by a back side thereof on the interposer substrate, another semiconductor die being mounted by a back side thereof on the active surface of the one semiconductor die and sized to leave the bond pads of the first semiconductor die exposed.

18. The semiconductor device package of claim 17, wherein the bond pads of each of the one semiconductor die and the another semiconductor die are electrically connected to the plurality of terminals with wire bonds.

19. The semiconductor device package of claim 1, wherein the encapsulant structure extends to peripheral edges of the interposer substrate.

20. The semiconductor device package of claim 4, further comprising a dielectric underfill material disposed in an open volume between the at least one electrical component and the opposing side of the interposer substrate and about the discrete conductive elements by which the at least one electrical component is connected to the pads of the two-dimensional pad array.

21. The semiconductor device package of claim 2, wherein the at least one electrical component comprises a plurality of components including at least one passive component and at least one active component.

22. A method of fabricating a semiconductor device package, the method comprising:

providing an interposer substrate comprising a dielectric member, a plurality of terminals proximate and extending along at least one peripheral edge thereof on one side thereof and an array of lands proximate and extending along a same at least one peripheral edge on an opposing side of the interposer substrate, terminals of the plurality being respectively electrically connected to lands of the land array through conductive via structures extending through the dielectric member, the interposer substrate further comprising a two-dimensional array of pads substantially centrally located on the opposing side of the interposer substrate, and wherein terminals of the plurality are respectively electrically connected to pads of the two-dimensional pad array;

mounting at least one semiconductor die by a back side thereof to the one side of the interposer substrate with a plurality of bond pads on an active surface thereof proximate and extending along at least one peripheral edge thereof adjacent the at least one peripheral edge of the interposer substrate;

respectively electrically connecting the plurality of bond pads to the plurality of terminals; and

disposing an encapsulant structure over the at least one semiconductor die and the one side of the interposer substrate.

23. The method of claim 22, further comprising mechanically and electrically connecting at least one electrical component to the interposer substrate through pads of the two-dimensional pad array.

24. The method of claim 23, further comprising selecting the at least one electrical component from the group consisting of passive components and active components.

25 The method of claim 23, further comprising disposing discrete conductive bumps on at least some of the pads of the two-dimensional pad array and connecting the at least one electrical component to the pads through some of the discrete conductive elements.

26. The method of claim 23, further comprising disposing discrete conductive bumps on at least some of the pads of the two-dimensional pad array.

27. The method of claim 2, further comprising providing a lead frame including a plurality of lead fingers, disposing inner ends thereof respectively over lands of the land array on the opposing side of the interposer substrate and mechanically and electrically connecting the inner ends thereto.

28. The method of claim 27, further comprising extending a wire bond between at least one pad of the two-dimensional pad array and an inner end of at least one lead finger.

29. The method of claim 27, further comprising covering at least the inner ends of the lead fingers and the opposing side of the interposer substrate with a dielectric material.

30. The method of claim 27, further comprising covering the at least one electrical component with a dielectric material.

31. The method of claim 23, further comprising:

affixing a carrier substrate to the land grid array package by a side thereof opposite the interposer substrate, the carrier substrate including a plurality of conductive pads on a surface thereof to which the land grid array package is affixed; and

extending wire bonds between lands of the land array and conductive pads of the plurality of conductive pads.

32. The method of claim 31, further comprising extending a wire bond between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate.

33. The method of claim 32, wherein extending the wire bond bond between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate comprises extending the wire bond in two segments joined at an electrically isolated pad of the two-dimensional pad array.

34. The method of claim 31, further comprising covering at least the lands of the land array, the wire bonds and the conductive pads with a dielectric material.

35. The method of claim 22, further comprising selecting the at least one peripheral edge of each of the interposer substrate and the at least one semiconductor die to comprise two opposing peripheral edges.

36. The method of claim 22, further comprising electrically connecting the plurality of bond pads to the plurality of terminals with wire bonds.

37. The method of claim 22, further comprising:
selecting the at least one semiconductor die to comprise two semiconductor dice;
mounting one semiconductor die by a back side thereof on the interposer substrate;
mounting another semiconductor die by a back side thereof on the active surface of the one semiconductor die in a manner to leave the bond pads of the first semiconductor die exposed.

38. The method of claim 37, further comprising electrically connecting the bond pads of each of the one semiconductor die and the another semiconductor die to the plurality of terminals with wire bonds.

39. The method of claim 22, further comprising forming the encapsulant structure to extend to peripheral edges of the interposer substrate.

40. The method of claim 25, further comprising disposing a dielectric underfill material in an open volume between the at least one electrical component and the opposing side of the interposer substrate and about the discrete conductive elements by which the at least one electrical component is connected to the pads of the two-dimensional pad array.

41. The method of claim 23, further comprising selecting the at least one electrical component to comprise a plurality of components including at least one passive component and at least one active component.

42. The method of claim 22, further comprising testing the at least one semiconductor die after mounting to the interposer substrate and connection of the plurality of bond pads to the plurality of terminals and before assembly thereof with additional structures.

43. The method of claim 42, wherein testing comprises at least one of open/short testing and functional testing.

WHAT IS CLAIMED IS:

1. A semiconductor device package, comprising:

an interposer substrate comprising a dielectric member, a plurality of terminals proximate and extending along at least one peripheral edge thereof on one side thereof and an array of lands proximate and extending along a same at least one peripheral edge on an opposing side of the interposer substrate, terminals of the plurality of terminals being respectively electrically connected to lands of the land array through conductive via structures extending through the dielectric member, the interposer substrate further comprising a two-dimensional array of pads substantially centrally located on the opposing side of the interposer substrate, and wherein the terminals of the plurality of terminals that are respectively electrically connected to lands of the array of lands are respectively electrically connected to pads of the two-dimensional pad array;

at least one electrical component mechanically and electrically connected to the interposer substrate through pads of the two-dimensional pad array;

at least one semiconductor die mounted by a back side thereof to the one side of the interposer substrate, the at least one semiconductor die comprising a plurality of bond pads on an active surface opposite the back side thereof, the plurality of bond pads proximate and extending along at least one peripheral edge thereof adjacent the at least one peripheral edge of the interposer substrate, bond pads of the plurality of bond pads being respectively electrically connected to the plurality of terminals;

an encapsulant structure disposed over the at least one semiconductor die and the one side of the interposer substrate; and

a lead frame comprising a plurality of lead fingers having inner ends respectively disposed over lands of the land array on the opposing side of the interposer substrate and mechanically and electrically connected to respective lands of the land array thereunder.

2. The semiconductor device package of claim 1, further comprising discrete conductive elements disposed on at least some of the pads of the two-dimensional pad array, the at least one electrical component being connected to the pads through some of the discrete conductive elements.

3. The semiconductor device package of claim 1, further comprising discrete conductive bumps disposed on at least some of the pads of the two-dimensional pad array.

4. The semiconductor device package of claim 1, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and an inner end of at least one lead finger.

5. The semiconductor device package of claim 1, wherein at least the inner ends of the lead fingers and the opposing side of the interposer substrate are covered with a dielectric material.

6. The semiconductor device package of claim 1, wherein the at least one electrical component is covered with a dielectric material.

7. The semiconductor device package of claim 1, further comprising:
a carrier substrate to which the semiconductor device package is affixed by a side thereof opposite the interposer substrate, the carrier substrate including a plurality of conductive pads on a surface thereof to which the semiconductor device package is affixed.

8. The semiconductor device package of claim 7, further comprising a wire bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate.

9. The semiconductor device package of claim 8, wherein the wire bond extending between at least one pad of the two-dimensional pad array and a conductive pad of the carrier substrate comprises two segments joined at an electrically isolated pad of the two-dimensional pad array.

10. The semiconductor device package of claim 7, wherein at least the lands of the land array and the conductive pads are covered with a dielectric material.

11. The semiconductor device package of claim 7, wherein the at least one electrical component is covered with a dielectric material.

12. The semiconductor device package of claim 1, wherein the at least one peripheral edge of each of the interposer substrate and the at least one semiconductor die comprises two opposing peripheral edges.

13. The semiconductor device package of claim 1, wherein the plurality of bond pads are electrically connected to the plurality of terminals with wire bonds.

14. The semiconductor device package of claim 1, wherein the at least one semiconductor die comprises a first semiconductor die and a second semiconductor die, the first semiconductor die being mounted by a back side thereof on the interposer substrate, the second semiconductor die being mounted by a back side thereof on an active surface of the first semiconductor die and sized to leave the plurality of bond pads of the first semiconductor die exposed.

15. The semiconductor device package of claim 14, wherein the plurality of bond pads of each of the first semiconductor die and the second semiconductor die are electrically connected to the plurality of terminals with wire bonds.

16. The semiconductor device package of claim 1, wherein the encapsulant structure extends to peripheral edges of the interposer substrate.

17. The semiconductor device package of claim 2, further comprising a dielectric underfill material disposed in an open volume between the at least one electrical component and

the opposing side of the interposer substrate and about the discrete conductive elements by which the at least one electrical component is connected to the pads of the two-dimensional pad array.

18. The semiconductor device package of claim 1, wherein the at least one electrical component comprises a plurality of components including at least one passive component and at least one active component.

19. The semiconductor device package of claim 1, wherein each of the plurality of terminals is respectively electrically connected to a land of the array of lands.

20. The semiconductor device package of claim 1, wherein the at least one electrical component comprises at least one of at least one passive component and at least one active component.

21. The semiconductor device package of claim 1, wherein the at least one electrical component comprises at least one passive component and at least one active component.

22. The semiconductor device package of claim 14, wherein the plurality of lead fingers of the lead frame further comprise outer ends respectively disposed proximate to a side of the semiconductor device package opposite the interposer substrate.

23. The semiconductor device package of claim 22, wherein a portion of the plurality of lead fingers between the inner ends and the outer ends is disposed adjacent to an outside edge side of the interposer substrate.