A HIGH PERFORMANCE INTEGRATED VARACTOR ON SILICON

ABSTRACT

A new MOS varactor device is described. A bottom electrode comprises a plurality of diffusion junctions in a semiconductor substrate. The semiconductor substrate may be n-type or p-type. The diffusion junctions are arranged in a two-dimensional array. The diffusion junction may be either n-type or p-type. The diffusion junctions may be contained in a p-well or an n-well. A dielectric layer overlies the semiconductor substrate. A top electrode overlies the dielectric layer. The top electrode comprises a single polygon containing a two-dimensional array of openings therein that exposes the diffusion junctions. The top electrode preferably comprises polysilicon. An interlevel dielectric layer overlies the top electrode and the diffusion junction. The interlevel dielectric layer has a two-dimensional array of contact openings that expose the underlying diffusion junctions. A patterned metal layer overlies the interlevel dielectric layer and contacts the diffusion junctions through the contact openings.

Fig. 9