An object of the present invention is an integrated circuit protected from ultraviolet rays. It is applicable to integrated circuits produced using MOS technology and in particular to integrated circuits comprising memory cells comprising a floating gate.

It is current practice to use memory cells comprising a floating gate to customize an integrated circuit at the end of manufacture after the test sequences, among other things to fix the various access paths and to authorize, or not, reading of memory zones. These memory cells are then used like fuses. They are of course also used conventionally in memory zones of integrated circuits.

These memory cells comprising a floating gate are sensitive to ultraviolet rays which cause the release of charges stored on the floating gate. However, any user may expose a circuit to ultraviolet rays. It is therefore important, in certain applications, to protect the circuit from ultraviolet rays as, for example, in applications requiring high security with regard to the retention of data in a memory. Thus it is necessary to guarantee to certain users total protection from ultraviolet rays over a period of several years.

In that case a metal mask, made of aluminium for example, is placed in a known manner over the integrated circuit. In this way, for example, cells called UUPROM cells (Ultraviolet Unerasable PRogrammable Memory) are produced from EPROM cells. Experience shows that these cells provide a protection from ultraviolet rays only for a limited time.

In practice, in a first examplary embodiment, this protection is only for a few weeks. This is not sufficient for some applications.

In this example a metal mask which isolates the element of the cell to be protected, namely the floating gate, from ultraviolet rays is positioned over the cell in a horizontal plane. Because, however, there is no protection between the plane of the substrate and that of the metal mask, ultraviolet rays can reach the floating gate indirectly, by

reflection between the substrate and the metal plane, thus discharging the charges which are accumulated there: the protection from ultraviolet rays does not exceed a few weeks.

To overcome this lack of effectiveness, in a second embodiment, metal projections projecting vertically downwards from the plane of the metal have been provided. These downward projections are fixed to the substrate around the cell to be protected. In practice these downward metal projections are fixed to diffusions of the same type as the substrate but more highly doped with impurities than the substrate. They are diffusions forming contact terminals, for example P^+ formed in a P type substrate.

A memory cell comprising a floating gate must, however, have its source, its drain and its control gate connected to conductive lines carrying the control signals making it possible to read, to program or to erase the cell. If this cell is insulated by downward metal projections fixed to a P^+ diffusion forming a contact terminal, it is necessary to be able to make the said connections to the conductive lines. It is possible to do this for the source or the drain, which in the chosen example of a P type substrate, are formed by N^+ diffusions. It suffices to make an N type island inside which the P^+ diffusion, forming a contact terminal for fixing the downward metal projections Rm, will be formed. Bridging over the substrate and the island, two N^+ diffusions are formed, one of which will, for example, be the source of the cell and the other of which will make possible the metallic contact with a conductive line. The formation of such an N type island is in fact necessary because it is not technologically possible to form a P^+ diffusion directly in an N^+ diffusion because of their respective concentrations of impurities.

It is the connection of the control gate, which is formed by a polysilicon region, which poses problems. In practice the polysilicon region which constitutes the control gate is above the plane of the substrate but below the metal plate. It prevents the formation in its

vicinity of a vertical downward metal projection such as is described hereinabove. In practice it is not possible to cut off the polysilicon gate nor to allow contact between the control gate and the metal plate which is connected to a voltage: the control gate would be short-circuited. In practice there are no downward metal projections near the connection between the control gate and the outside. The cell is not completely insulated.

Thus, in the above example the possible entrances for ultraviolet rays have certainly been reduced, but the rays can still pass via the polysilicon control gate. Moreover these rays, by reflection between the metal plane and the substrate, can reach the floating gate. The period of protection is thus increased to a few months. For applications which require a minimum of 4 to 5 years protection, the result is unsatisfactory.

In a third embodiment, the shape of the polysilicon control gate has therefore been altered so as to decrease the amount of reflection of ultraviolet rays. An example of such an embodiment is shown in Figure 1. In this view of the circuit from above, two lines of metal can be seen which represent the contact on the substrate of the vertical downward metal projections. These lines are shown in Figure 1 by a region defined by thick lines.

A line of polysilicon, shown hatched in the Figure, can also be seen which passes between the two lines of metal without touching them. Inside the protected region the polysilicon line makes a plurality of 90° bends along a guiding axis. The two lines of metal follow, on either side, the twisting path of the polysilicon line. By means of these complicated zigzags of metal and polysilicon, the reflections of the ultraviolet rays are greatly attenuated and consequently several years of protection from ultraviolet rays are obtained.

However, this is obtained at the expense of an increased surface area occupied by the cell. In practice these zigzags along a guiding axis

require a lot of space, and they require more of it the longer the desired period of protection. Thus, in the current state of the art, a protection lasting 4 years is obtained with a length along the guiding axis of the zigzags of about 200 µm. Knowing that for the same state of the art the EPROM cell usually occupies a surface area of about 180 μm^2, it can be seen that this increased surface area is a major disadvantage in practice, because one always seeks to decrease surface areas in order to obtain an increasingly high density of integration. Moreover, the additional material incurs an additional manufacturing cost.

An aim of the invention is to overcome these disadvantages by proposing a different cell structure which makes it possible, on the one hand, to form a ring comprising downward metal projections which are continuous around the cell and, on the other hand, to decrease considerably the surface dimensions of the UUPROM cell thus obtained.

Consequently an object of the present invention is an integrated circuit produced using MOS technology from a semi-conductor having a first doping type, including at least one memory cell having a floating gate, a source, a drain and a control gate, and being protected from ultraviolet rays by a metal mask which covers its upper surface, this mask having fixing locations on the semiconductor substrate formed by downward metal projections from the metal mask, as known from the documents US-A-4519050 and EP-A-0227549, characterized in that the control gate is formed by a diffusion of a second type of doping, and in that the fixing locations form a continuous ring of metal fixed to a ring consisting of a diffusion of the same type as the substrate but more highly doped than the substrate and wider than the metal ring, this metal ring completely isolating the floating gate memory cell from ultraviolet rays in a region inside the metal ring, the drain, the source and the control gate being connected to the outside of the metal ring by buried connections.

The characteristics and advantages of a circuit in accordance with the invention are described in the following description. This

description is given by way of non-limiting illustration with reference to the attached Figures in which:

- Figure 1 is a view from above of a line of polycrystalline silicon interleaved between two lines of metal made in the state of the art for protection from ultraviolet rays, already described above,
- Figure 2 is a view from above of part of a circuit protected from ultraviolet rays in accordance with the invention,
- Figure 3 is the electronic equivalent circuit to the circuit function shown in a view from above in Figure 2,
- Figure 4a is a view in cross-section along the line AA' in Figure 2,
- Figure 4b is a view in cross-section along the line BB' in Figure 2,
- Figure 4c is a view in cross-section along the line CC' in Figure 2,
- Figure 4d is a view in cross-section along the line DD' in Figure 2.

Figure 2 is a plan view from above of a region of an integrated circuit protected from ultraviolet rays in accordance with one embodiment of the invention.

In this embodiment, two floating gate memory cells C_1 and C_2, having symmetrical structures in relation to an axis M, are protected from ultraviolet rays in a common interior region 1. This interior region 1 is defined in the plane of Figure 2 by a continuous metal ring Am shown in thick lines in Figure 2. In the plane of this Figure, the metal ring Am is shown by the line of contact of vertical downward metal projections of a metal mask. This metal ring is limited in width by two parallel end edges and in height by the plane of the substrate and the plane of the metal mask. Its geometrical shape in the plane of Figure 2 is defined as follows:

- two equal, facing parallel sides vertically enclosing the interior region 1;
- a horizontal side H connecting the left and right two vertical sides at their lower ends;

- from the upper end of the vertical left hand side, a side extends perpendicularly towards the right over a length l_1, then makes a 90° downward turn to reach an end X of a section XX' at right angles to it and extending to the right from the end X;

- from the upper end of the vertical right hand side, a side extends perpendicularly towards the left over a length l_1, then makes a 90° downward turn to reach an end X' of a section XX';

- the axis of symmetry M is the line perpendicular to the middle of the section XX'.

In the plane of Figure 2, the surface area of the metal ring Am is completely enclosed within the surface area of a diffusion ring Ad. The two end edges which delimit the width of the diffusion ring Ad are parallel to the end edges of the ring Am which they contain. The ring Ad has the same shape as the ring Am which it contains. In addition, the ring Ad is bordered by a limiting edge B1 on its outermost edge, its internal end edge delimiting the interior region 1.

In what follows the assembly comprising the rings Am and Ad and the edge B1 will be called the boundary F. Moreover, a P type substrate will be taken as an example.

Beneath the boundary, near the section XX', an N type island Cal is delimited by a parallelogram. The boundary F passes over it, parallel to two sides of the parallelogram seen from above.

In a preferred example the parallelogram of the island Cal is a rectangle, the 2 sides having the greatest length being parallel to the boundary which passses over the island Cal. The median line perpendicular to the sides of the island Cal parallel to the boundary coincides with the median line M perpendicular to the section XX', which once again is the axis of symmetry M of the circuit in this embodiment of the invention. In Figure 2 the island Cal is defined by fringe lines.

Bridging over the substrate and a part of the island Cal outside the boundary, a zone Z1 of N^+ diffusion is defined by a parallelogram. A metal contact AG is formed on all or part of the end of the diffused zone Z1 outside the boundary F. AG is the controlled ground of a memory array, not shown, containing the memory cells C_1 and C_2.

In this example the parallelogram is rectangular. The two longest sides of the diffusion Z1 are parallel to the two longest sides of the island Cal but they are not as long as the latter. Their median perpendicular line is coincident with the axis of symmetry M.

Bridging over the island Cal and over the substrate inside the internal region 1, a part 10 of an N^+ diffused zone Z2 has the same shape, having an equal and parallel greatest length as the facing diffused zone Z1. The diffused zone Z2 is symmetrical relative to the axis M. The part 10 is extended by an section 20, symmetrical relative to the axis M and narrowing obliquely towards another parallelogram 30, symmetrical relative to the axis M. This last part 30 of the diffused zone Z2 is continued by an N^+ diffused zone which extends, from its greatest length, perpendicularly to the axis M and symmetrically on either side of the latter. To the left of the axis M it forms the source S_1 of the cell C_1; to the right it forms the source S_2 of the cell C_2.

In practice this arrangement makes it possible to connect the source S_1 and the source S_2 to the controlled ground AG by a single conductive link formed by the zone Z2, the island Cal, the zone Z1 and lastly the metal contact by which the signal of the controlled ground AG (standing for Array Ground in English publications) is transmitted. However the conductive link thus formed is in fact the combination of two conductive links, each of the links being sufficiently wide for the current surge on each of the sources S_1 and S_2.

In the following description only the half-plane on the left relative to the axis M, which contains the cell C_1, will be considered. The description applies in a symmetrical manner (symmetry M) to the half-plane on the right which contains the cell C_2.

The memory cell C_1 comprises a source zone S_1 and a drain zone D_1, which are N^+ diffusions, a floating gate GF_1, made in the form of a polysilicon region, and a control gate GC_1 which in the invention is an N^+ diffusion.

Moving towards the left, starting from the N^+ diffused zone of the source S_1, the latter is cut at right angles to its greatest length, in other words vertically, by a rectangular branch 100 of the floating gate GF_1. The longest axis of the branch 100 is vertical. Aligned with the longest horizontal axis of the zone S_1, to the left of the branch 100, there is an N^+ diffused drain zone D_1 of the cell C_1. To the left of this zone D_1, another branch 200 of the floating gate GF_1 passes above the zone D_1 perpendicularly to its greatest length (in other words vertically in the description). The branch 200 has the same shape in the plane of Figure 2 as the branch 100 but it is narrower. At the upper end of the branch 200 the diffusion zone D_1 is continued in another N^+ diffusion zone Z3, which extends vertically upwards, then extends steeply obliquely towards the top of the interior region 1. This zone Z3 ends in a parallelogram 11, which is preferably rectangular. The diffusion Z3 in this part 11 is formed bridging the substrate in the interior region and an island Ca2.

The island Ca2 is preferably rectangular; its two longest sides are parallel to and longer than those of the parallelogram 11 of the facing zone Z3. The island Ca2 is crossed by the left vertical side of the boundary, which crosses it parallel to its two longest sides.

Outside the boundary, bridging the substrate and the island Ca2, an N^+ diffusion Z4 is formed having the same shape and an equal greatest length as the part 11 of the diffusion Z3 which faces it. This diffusion Z4 comprises a narrower left hand part which also forms a parallelogram and which constitutes the source St_1 of a selection transistor TS_1. This diffused part St_1 is cut perpendicularly at the left by a polysilicon region which forms the control gate Gt_1 of the selection transistor and which transmits a word line LM_1 signal.

This polysilicon region cuts off perpendicularly at the left the diffusion zone of the drain Dt_1 of the transistor TS_1, this zone Dt_1 being located facing that of the source St_1. A metal contact is formed on this diffusion zone Dt_1. This metal contact transmits a signal of a bit line LB1 to the drain Dt_1 of the selection transistor TS_1.

The diffusion zone Z3, indirectly through the intermediary of the island Ca2 and the diffusion zone Z4, forms a contact between the drain D_1 of the cell C_1 and the source St_1 of the selection transistor TS_1 (Figure 3).

The zone D_1 is in fact extended by the diffusion zone Z3, as has been seen.

The branch 200 of the floating gate GF_1 also comes closer to a region of the substrate thus decreasing the thickness of oxide at this location, in particular near the drain D_1. This thinner region of oxide (for example 9 nm (90 Angstroms)) is called a tunnel oxide region O (Figures 4d and 4a). It promotes the transfer of charges between the drain D_1 and the floating gate GF_1.

The two branches 100 and 200 rejoin at their lower end a parallelogram 300 positioned lower down than the zones aligned with the source S_1 and the drain D_1 of the cell C_1. This part 300 of the floating gate GF_1 covers an N^+ diffusion Z5 which forms, underneath the said floating gate, the control gate GC_1. The diffusion Z5 extends towards the left, towards the boundary where it terminates bridging the substrate in the interior region 1 and an N type island Ca4 formed on either side of the boundary like the islands Ca1 and Ca4 already described. The boundary passes across the island Ca4 parallel to one of its sides. The island Ca4 is preferably a parallelogram. In this case it is the shortest sides which are parallel to the boundary. A metal contact is formed over a portion of the island outside the boundary. It transmits a signal CG_1 for controlling the control gate GC_1 of the cell C_1.

The signals AG, LB1, LM1 and CG1 are the 4 control signals associated with the selection transistor TS_1 and with the memory cell C_1. By their state they control reading, programming or erasure of the cell C_1. An example of states corresponding to reading, programming or erasure are shown in the following Table:

	CG1	LM1	LB1	AG
Programming	Vss	20v	20v	floating
Erasure	20v	20v	floating	Vss
Reading	2v	5v	to the read circuit	Vss

Vss is the electrical ground potential of the circuit to which the metal mask, and consequently also the diffusion ring Ad, is connected.

It has been seen that the diffusion ring Ad forming a contact terminal is advantageously wider than the ring Am which it completely contains. In practice the supports for the vertical projections are obtained, for example, by hollowing out the circuit as far as the substrate using well known technological processes. Holes are then formed, the bottoms of which are constituted by the surface of the substrate. It is not necessary that the surface of the substrate thus laid bare should be wider than the diffusion forming the contact terminal on the surface of the substrate because, otherwise, there is a risk that the metal will make contact not only on this diffusion, but also on either side of the said diffusion, with the risks of short-circuiting which this entails.

Outside the diffusion ring Ad forming the contact terminal, relative to the interior region 1, the limiting edge B1 represents the projection of the contours of the metal mask in the plane of Figure 2. In the example described, and as can be seen in Figures 4a to 4d, the metal mask Mm projects beyond the vertical downward metal projections Rm. This makes it possible to ensure reliably that the metal layer, when it is applied, will correctly fill all the holes right down to the bottom, that is to say up to the surface of the substrate. Because the metal layer is spread out it is preferable to have a flat surface on either side of the hole.

The memory cell C_1 comprises a floating gate GF_1 and a control gate GC_1. Its essential feature made use of in the invention is that the control gate is a diffusion and not a polysilicon gate as in the UUPROM cells of prior art. In practice a cell having its control gate made by a diffusion and its floating gate made of polysilicon is substantially wider than a cell having two polysilicon levels (floating gate and control gate). It has been shown in fact that the diffused control gate GC_1 is displaced in the plane relative to the source S_1 and drain D_1 regions, the floating gate then covering the source and drain regions on the one hand and the control gate on the other hand. In a cell comprising two polysilicon levels, the control gate covers the floating gate which itself covers the source and drain regions. Such a structure is therefore more dense than the spread out structure of the cell comprising only one polysilicon layer. This greater surface area consumption is the major disadvantage of this technology called single layer polysilicon technology. However, it will be shown hereinafter that for the formation of an UUPROM cell, this major disadvantage becomes a definite advantage. Moreover the reduction to only one level of polysilicon eliminates one masking level. This technology is less costly in terms of masks.

In the example, it was decided to show an EEPROM type cell and a possible method of producing such a cell. However, it is of course understood that the invention is not limited to this embodiment nor to this type of cell. It would, for example, have been equally

possible to show an EPROM cell. The only limitation is that the cell must comprise a floating gate, an element which can be discharged by ultraviolet rays.

An EEPROM cell is of necessity controlled by a selection transistor because it is desired to have available at least two of the three commands, namely reading, programming and erasure of the cell. The equivalent circuit corresponding to Figure 2 is shown in Figure 3. The selection transistor TS_1 and the memory cell C_1 have the same type of channel opposite to the doping type of the substrate.

The description which is given for a P type substrate is easily transposable to an N type substrate by reversing the type of impurities and the polarization mentioned in the description.

The EEPROM cell is, in the example, not symmetrical: the drain D_1 and the source S_1 are not interchangeable. The drain D_1 is in fact characterized by a thin region of oxide O, beneath the branch 200 of the floating gate GF_1, and this facilitates the transfer of charges by the tunnel effect. This is what is shown in the cross-section DD' in Figure 4d, with the tunnel oxide zone O beneath the branch 200 of the floating gate GF_1.

The N^+ diffusion of the control gate GC_1 is formed before the polysilicon region 300 above it. The N^+ diffusion is then correctly located beneath the floating gate, as can be seen in the cross-sections AA' and CC' in Figures 4a and 4c respectively.

The two preceding paragraphs describe a possible embodiment of an EEPROM cell C_1 comprising a single layer of polysilicon, in an internal region 1. This cell structure makes possible the passage of all the signals between the internal region 1 and the exterior of the boundary defined by the rings Am and Ad, all of them being conducted through the intermediary of an island beneath this boundary. They are buried connections, that is to say they occur in the substrate beneath this

boundary. Thus, for each of the signals listed hereinafter, it is this type of connection which is used:

- the control gate GC_1, to connect to the command for the gate GC_1: island Ca4;
- the source S_1 of the cell C_1, to connect to the array ground AG: island Ca1;
- the diffusion Z3, connected to the drain D_1 of the cell C_1, to connect to the source St_1 of the transistor TS_1: island Ca2.

Take the N type island Ca2 for example. After the island Ca2 has been formed (N type diffusion in the P type substrate), the P^+ diffusion of the contact terminal ring Ad (Figures 2 and 4b) is then made inside the island Ca2. This P^+ diffusion thus occupies all the greatest length of the island seen from above (Figure 2). An N^+ diffusion is then made on each side of the P^+ diffusion bridging the island Ca2 and the substrate P: in the example these are Z4, which is continued by the source St_1, and Z3. Conduction then occurs between the two N^+ diffusion zones, Z3 and Z4, via the island Ca2 underneath the contact terminal ring Ad and consequently also beneath the metal ring Am. A first diffusion zone is therefore inside the interior region 1, Z3 in the example. A second is outside it, Z4 in the example.

In certain cases this second diffusion may not be formed and a metal contact is formed directly on the N diffusion of the island, outside the boundary. In the example shown in Figure 2 the metal contact associated with the command for the control gate CG_1 is formed in this manner. This second possible type of embodiment is shown in cross-section in Figure 4c. It all depends on the topology of the circuitry which produces CG_1, for example. Thus, if the signal CG_1 is generated far from the UUPROM cell it will be brought to the cell by a metal line: the metal contact will then be made directly on the island Ca4 in the example. On the other hand, if the signal CG_1 is supplied by a transistor very close to the UUPROM cell it will arrive in an N^+ diffusion and an N^+ contact will be required on the island: this is the case in the example for the island Ca2 for the signal St_1. These metal contacts are formed outside the boundary. If they were in fact formed inside the boundary,

the metallic conductor which carries a control signal would have to be made to pass through either the metal mask or the downward metal projections Rm of this mask which are put at the ground potential Vss : a short-circuit would be caused.

The formation of the N type island and the P^+ diffusion add two additional operations in the production of the cell. On the other hand, the corresponding masks exist and only their design has to be modified, as does the design of the mask for the N^+ diffusions to be formed.

It is because it is necessary to prevent the conduction of the various PN diodes constituted by the junctions:

- P^+ type diffusion in an N type island, and
- P type substrate in an N type island,

that the metal mask is connected to the plane of the circuit at ground potential Vss. Thus the various diodes are always reverse polarised and blocked.

Furthermore, the ratio of the width l separating the two N^+ diffusions on each side of an island at the boundary to the greatest length L of these N^+ diffusions parallel to the boundary is made as small as possible, whilst respecting restrictions of design, so as to reduce as much as possible the resistance R induced by the N type island. In practice the resistivity p of the N type island is greater than that of an N^+ diffusion, because the resistivity of a diffusion is inversely proportional to the doping concentration. However, a direct effect on the control signals of the induced resistance R is to increase the access time of the cell, whereas one always seeks to decrease this access time. It will be recalled that the value of this induced resistance R is given by the following equation:

$$R = (l/L)xp$$

According to the invention, preferably a ratio of l/L is chosen which is optimal for a minimum induced resistance. In particular, it is

with this in mind that the diffusions are formed in the example for the buried connection associated with the signal AG and the source St_1 of the selection transistor.

It has been seen above how the diffusion of the contact terminal P^+ of the ring Ad is formed in an N type island. Outside the islands made to provide the conduction of the command signals, the P^+ diffusion is formed directly in the P type substrate, as can be seen for example in the cross-section AA' shown in Figure 4a and in the cross-section DD' shown in Figure 4d.

It is in this manner that it is possible to fix the downward metal projections continuously on a P^+ diffusion, this diffusion being partially formed in the P type substrate and partially formed in an N type island to provide the conduction of the command signals to the region inside the boundary.

It is thus possible to protect from ultraviolet rays any cell or any assembly of cells for which, within a defined perimeter, all the control signals are provided through diffusions. The contact terminal ring Ad and the vertical downward metal projections fixed on the ring Ad are made on this perimeter.

In the case of an EEPROM cell which is controlled by a selection transistor TS_1, this selection transistor TS_1 is preferably located outside the said perimeter because its control gate is made of polysilicon. This is not otherwise inconvenient, since it does not have to be protected from ultraviolet rays.

In practice it would be technologically possible to form a metal contact from a metal line above the control gate, between the said control gate made of polysilicon and an N^+ diffusion, to provide the conduction between these two parts. It would also be possible to use a "buried contact" technology which makes it possible to connect the polysilicon directly to a diffusion or to the substrate. However, the latter technology is expensive and difficult to perform. By using such

techniques, however, it would be possible to include the selection transistor in the interior region 1, by forming a connection between this N^+ diffusion and the region outside the boundary.

This solution has, however, many disadvantages. First of all it increases the number of islands necessary for the connections between the interior region 1 and the outside. In practice, if the selection transistor TS_1 is located outside, only its source St_1 has to be connected in the interior region 1. If it is located inside the boundary not only the diffusion connected to the control gate but also that connected to the drain D_1 have to be connected to the outside. In this case therefore there is an additional island and consequently the final surface area occupied by the protected cell is larger. Furthermore, the selection transistor TS_1 has then the two control line signals LB_1 and LM_1, which are transmitted through the intermediary of an island beneath the boundary, and this increases the access time to the transistor and thus to the cell. Lastly, the metal contact between the control gate and an N^+ diffusion would have to be made by a metal line situated in a plane above the control gate, this metal line having at its two ends two downward projections, one on the gate and one on the diffusion. Since the metal line could not be in the plane of the metal mask, there would then be a second plane of metal between the first plane of the metal mask and the control gate. There would then be two levels of metal and an increase in the number of layers in the circuit. Moreover, in practice, one would only want one layer of metal in an integrated circuit, in particular in an integrated memory circuit. Lastly, the multiplicity of contacts and conduction modes tend to increase the access time (conduction through the intermediary of an island, metal contact between an N^+ diffusion and a polysilicon region).

It should however be noted that using this technique it would be possible to obtain total protection in accordance with the invention of a floating gate cell having its control gate made of polysilicon and making a metal contact with an N^+ diffusion. However, the disadvantages of such a metal contact technique have been seen and the technique of the first

embodiment described is preferred to it. With this technique it is particularly advantageous to choose an EEPROM cell the control gate of which is made in the form of a region of N^+ diffusion situated under the floating gate, and of a selection transistor located outside the boundary. In this case the metal lines mentioned hereinabove become unnecessary.

Lastly, it will be noted that in the invention it is not important that the downward metal projections should be vertical: this is a characteristic which arises solely from the example of the process for obtaining the downward projections described. It is only necessary that the downward projections connect the metal mask to the substrate and that they should be fixed continuously to a diffusion in the substrate so as to completely isolate the interior region from ultraviolet rays.

In the example shown in Figure 2, there are two memory cells C_1 and C_2 in the interior region 1. There is thus a "double" UUPROM cell.

The use of a cell comprising a diffused control gate has made it possible, on the one hand, to protect a floating gate memory cell completely from ultraviolet rays, and this in a simple manner both in principle and above all in its practical realisation, because it does not increase the number of masks necessary. On the other hand it has made it possible, and this is a considerable advantage from the point of view of integration density, to reduce substantially the surface area occupied by such an UUPROM cell. In the example of the double cell a surface area of 242 μm^2 could be expected for example. Moreover, the technology associated with cells comprising a diffused control gate is simpler and more reliable than that associated with cells comprising two levels of polysilicon because of the absence of inter-poly between the floating gate and the control gate. These advantages are therefore reflected in the reliability of such UUPROM cells in accordance with the invention.

The cells C_1 and C_2 have, in the example, their source S_1 and S_2 at the same array ground signal AG. This signal is in fact common to all of the memory array and the cells C_1 and C_2 are independent. Other

configurations are possible, depending on the logic function to be obtained. In the example the surface area occupied by memory cells protected from ultraviolet rays in accordance with the invention has been reduced by twice the surface area of a line of the ring Ad along the axis M, relative to the surface area occupied by two memory cells each independently protected from ultraviolet rays in accordance with the invention. It would also be possible to obtain such a structure comprising three or four cells by utilizing a symmetry relative to the bottom horizontal side H.

Finally, the invention also applies to a single cell on its own.

CLAIMS

1. An integrated circuit produced using MOS technology from a semiconductor having a first type of doping (P), comprising at least one memory cell (C_1) having a floating gate (GF_1), a source (S_1), a drain (D_1) and a control gate (CG_1) and being protected from ultraviolet rays by a metal mask (Mm) which covers its upper surface, this mask having fixing locations on the semiconductor substrate formed by downward metal projections (Rm) from the metal mask (Mm), characterized in that the control gate (CG_1) is formed by a diffusion of a second type of doping (N^+), and in that the fixing locations form a continuous ring of metal (Am) fixed to a ring (Ad) consisting of a diffusion of the same type but more highly doped (P^+) than the substrate (P) and wider than the metal ring (Am), this metal ring completely isolating the floating gate memory cell (C_1) from ultraviolet rays in a region (1) inside the metal ring (Am), the drain (D_1) the source (S_1) and the control gate (CG_1) being connected to the outside of the metal ring (Am) by buried connections.

2. An integrated circuit as claimed in claim 1, characterized in that the downward metal projections (Rm) from the metal mask (Mm) are not formed at the edge of the metal mask (Mm).

3. An integrated circuit as claimed in claim 1 or claim 2, characterized in that a circuit (TS_1) for selection of the UUPROM cell is located outside the metal ring (Am).

4. A circuit as claimed in either one of claims 2 or 3, characterized in that two floating gate memory cells (C_1, C_2) are inside the same metal ring each having their own selection transistor (TS_1, TS_2) and having only their sources (S_1, S_2) connected together in common, the latter being connected to a common array ground signal (AG) thus forming a double UUPROM cell.

* C L M S *

5. A circuit as claimed in claim 4, characterized in that the double UUPROM cell comprises an axis of symmetry (M) which separates it into two symmetrical structural layouts each comprising one cell (C_1, C_2).

6. A circuit as claimed in any one of the preceding claims which has a buried connection comprising an island and, bridging this island and the substrate, two facing diffusions, characterized in that the length (L) of the two facing diffusions is greater than the distance (l) which separates them, the length in question being that of the sides of the two parallel, facing diffusions of identical length.