

Description

Title of the invention: Device for testing a plurality of integrated circuits on a semiconductor wafer

Technical field

5 The present invention relates to a device and a method for testing a plurality of integrated circuits on a semiconductor wafer.

Technical background

10 In the microelectronics industry, chips, integrated circuits and dies are generally fabricated in series and in large quantities on a single semiconductor wafer, notably on a silicon wafer. Integrated circuits may include various elements, such as a memory circuit, a microprocessor, a fuse circuit, communication busses, flip-flop, latch or buffer logic circuits, and other input/output (I/O) interface circuits.

15 Before being cut and packaged, each integrated circuit undergoes a performance or failure test in order to verify whether its electrical characteristics conform to the specifications for which it was designed. For example, a performance test may be conducted in which signals in the form of a data frame are sent to the input of the integrated circuit and the response signals at the output of the circuit are monitored and analyzed. When the response signals do not conform, the integrated circuit is declared to be defective and is discarded. A static failure test may also be
20 conducted in which high voltages and/or currents are applied to integrated circuits in order to eliminate those which are liable to be affected by premature failure.

25 It is common practice to conduct performance and failure tests using an automated test equipment (ATE) which is in the form of a programmable electronic system the main function of which is to implement a test program such as, for example, sending a set of data frames or values of voltages and/or currents to the input of integrated circuits, then collect and analyze the response signals of said circuits. For performing this function, the test equipment has input-outputs, called channels, the number of which generally conditions the number of integrated circuits which it is capable of testing simultaneously.

30 The automatic test equipment generally communicates with integrated circuits under test conditions by means of an interface card, itself connected to a probe card.

The probe card is configured to establish an electrical connection between the interface card and test pads which are specific to integrated circuits. The interface card relays and, optionally, preprocesses the signals between the probe card and the test equipment. When they are under conditions of testing by the automatic test equipment, integrated circuits are often called DUTs (devices under test). They are generally tested in rows directly on the semiconductor wafer.

The probe card is generally in the form of an electronic card provided with a plurality of pins or studs, the number and dimensions of which correspond to the density and to the size of the test pads which are specific to integrated circuits, and the arrangement of which makes it possible to redistribute the electrical signals exchanged between the test equipment and the integrated circuits via the interface card. In use, the probe card generally remains fixed while the wafer comprising the integrated circuits is placed under the probe card using a prober so as to establish electrical contact between the pads of the integrated circuits in a row of electrical circuits and the pins of the probe card.

In the semiconductor industry, and more generally, in the microelectronics industry, the cost of test equipments and the time required to conduct the procedures for testing the performance of integrated circuits are major concerns in the face of ever greater and faster demands for producing circuits.

A general trend is to increase the number of integrated circuits tested simultaneously, notably when the cycles of the test procedures are particularly long. This is the case, for example, with integrated circuits comprising non-volatile memories which require, in their test procedures, numerous write and erase operations. Nowadays, several tens or even hundreds of integrated circuits are tested simultaneously in parallel depending on the available channels of test equipments and probe cards. In addition to increasing the number of integrated circuits simultaneously, it is also common to optimize test procedures or to modify the design of circuits in order to reduce their test duration.

US 4956602 A, [AMBER ENGINEERING INC [US]], 11.09.1990 describes a semiconductor wafer the surface of which comprises a plurality of integrated circuits and a plurality of multiplexers which are composed of multiplexing lines located in the cutting areas of the wafer. The integrated circuits are connected to a reduced

number of test pads via the multiplexers. A larger number of integrated circuits may be tested in parallel with the same number of test pads.

US 6366112 B1 [MICRON TECHNOLOGY INC [US]] 09.10.2001 describes a probe card comprising a multiplexer circuit configured to selectively broadcast and transmit test signals from a test equipment to the integrated circuits of a semiconductor wafer. The multiplexer circuit makes it possible to distribute the channels of the test equipment over several integrated circuits tested in parallel. The probe card comprises a silicon-based substrate on which contactors are formed by chemical etching. The contactors are of suitable dimensions to be brought into contact with the pads of the integrated circuits to be tested. Each multiplexer circuit is formed by a plurality of field-effect transistors which make it possible to select the contactors using control signals. Each multiplexer circuit redistributes the channels of each test site of the test equipment in order to multiply the number of integrated circuits which may originally be tested by each test site.

US 6400173 B1 [HITACHI LTD [JP]] 04.06.2002 describes a system which makes it possible to reduce the time for testing the integrated circuits on a semiconductor wafer. The system comprises a probe card provided with a plurality of pins which are spatially arranged so as to be able to be connected to the pads of the integrated circuits. The pins are connected to a plurality of test circuits contained in the probe card. The test circuits are configured to exchange electrical signals with the integrated circuits and generate test results according to a given test program.

US 2003 074611 A1 [TOWER SEMICONDUCTOR LTD [US]] 17.04.2003 describes a system which makes it possible to increase the number of non-volatile memory integrated circuits which may be tested simultaneously in parallel. The system includes a test equipment, a probe card and an alignment plate. The probe card comprises a substrate provided with an auxiliary circuit, a first series of pads which are arranged on one of its surfaces and suitable for being electrically connected to the test equipment, and a second series of pads which are arranged on its other surface and suitable for being electrically connected to pads arranged on the wafer comprising the integrated circuits to be tested. The two series of pads are also connected to the auxiliary circuit by means of switches configured to optionally bypass it. The auxiliary circuit comprises a plurality of self-diagnostic circuits which may be respectively associated in parallel with the integrated circuits of a wafer. This

configuration makes it possible to reduce the time required to conduct read or erase operations in the non-volatile memory of the integrated circuits. Self-diagnostic circuits may also be directly integrated into the cutting lines of the wafer comprising the integrated circuits to be tested. They are configured to exploit only a limited
5 number of pads of the integrated circuits and share certain pads between several circuits, thus increasing the number of circuits which may be tested in parallel.

US 6903565 B2 [INFINEON TECHNOLOGIES AG [DE]] 07.06.2005

describes a system for testing, in parallel, a plurality of integrated circuits on a semiconductor wafer. The system comprises a probe card provided with pins and an
10 interface card. The system comprises an external power supply unit which makes it possible to deliver a supply voltage to a plurality of integrated circuits. The interface card comprises a voltage regulation unit controlled by a reference voltage source, and an electric current-limiting unit which makes it possible to measure the current consumed by the integrated circuits. The electric current-limiting unit is configured to
15 operate an electrical isolation device when the current consumed exceeds a certain threshold.

WO 2006 083856 A1 [FORMFACTOR INC [US]] 10.08.2006 and WO 2007 146583 A2 [FORMFACTOR INC [US]] 21.12.2007 describe a probe card comprising a circuit which makes it possible to share an electrical power supply channel of a test
20 equipment between four integrated circuits. With each integrated circuit, said circuit associates a voltage regulation module which makes it possible to isolate an integrated circuit in the event of a current overload. The probe card may comprise a multiplexer circuit for redirecting the output signals from the integrated circuits to the test equipment.

25 US 8378698 B2 [SAMSUNG ELECTRONICS CO LTD [KR]] 19.02.2013 describes a probe card provided with pins which are suitable for being in electrical contact with the pads of a plurality of integrated circuits on a semiconductor wafer. The probe card includes a plurality of test circuits, each test circuit itself comprising a plurality of signal transmitters corresponding to an integrated circuit to be tested on
30 the semiconductor wafer. The voltages and the control signals of a test equipment are relayed by the signal transmitters and sent to the integrated circuits. The signal transmitters are further configured to relay the response signals from the integrated circuits to the test equipment.

US 2016011232 A1 [INFINEON TECHNOLOGIES AG [DE]] 14.01.2016

describes a system for increasing the number of integrated circuits which may be tested simultaneously in parallel without having to increase the number of channels of the test equipment. The system comprises a test equipment, an interface card and
5 a probe card in the form of a circuit provided with a plurality of pads which are suitable for being connected to a plurality of integrated circuits. The circuit of the probe card is configured to exchange an identical instruction with all of the integrated circuits to which it is connected and exchange an instruction with the test equipment via the interface card.

10 US 2022 341991 A1 [WINBOND ELECTRONICS CORP [TW]] 27.10.2022

describes a system for the number of integrated circuits which may be tested simultaneously in parallel by sharing the available channels of a test equipment. The system comprises a test equipment and a test device which is composed of an interface circuit and an analysis circuit. The interface circuit is simultaneously
15 connected to four integrated circuits to be tested on a silicon wafer and makes it possible to transmit signals from the test equipment to the integrated circuits. The interface circuit comprises a buffer circuit coupled to the four integrated circuits to be tested and to the design circuit. The buffer circuit makes it possible to redistribute a power supply channel of the test equipment between the four circuits as well as the
20 control and input/output signals. The analysis circuit receives and serializes the output signals of the four integrated circuits using flip-flop circuits before communicating them to the test equipment.

Summary of the invention

25 Technical problem

A significant trend in the microelectronics industry is the development of low-power integrated circuits in order to reduce their energy consumption. Concretely, this trend results in a reduction in the operating voltages and currents of the integrated circuits. By way of example, in the field of smart cards, the development
30 effort is currently concentrated on class B and C integrated circuits within the meaning of ISO/IEC 7816-3:2006, that is to say integrated circuits with operating

voltages and currents which are less than 3.3 V and 50 mA for class B and less than 1.98 V and 30 mA for class C, respectively.

A direct consequence of this trend is the high-priority development of test equipments which are suitable for this type of integrated circuits and, because of the high costs and the technical constraints of installing such test equipments, their preferred deployment within semiconductor foundries, in particular within open foundries. In other words, "high power" test equipments of electronic circuits with high operating voltages such as, for example, class A integrated circuits in the field of smart cards, are becoming less and less available in foundries. Either they are, in current foundries, being gradually replaced by "low-power" test equipments or, in new foundries, they are no longer deployed.

Despite the general trend towards low-power electronics, there still remains a need to fabricate high-power integrated circuits – for example class A integrated circuits in the field of smart cards. However, the implementation of performance and failure tests, in particular static failure tests, on this type of integrated circuits requires the use of "high-power" test equipments, the availability of which is now becoming ever rarer. Also, for cost reasons, it is essential to test integrated circuits on the production site, that is to say in the foundry. A need therefore appears to be able to conduct performance and failure tests on "high power" circuits such as, notably, class A integrated circuits in the field of smart cards, using test equipments which are not suitable for implementing these tests on this type of integrated circuit.

Technical solution

In a first aspect of the invention, a probe card for testing a plurality of integrated circuits on a semiconductor wafer is provided, said probe card comprising:

- a plurality of pins which are suitable for providing a temporary electrical connection with pads of a plurality of integrated circuits to be tested on a semiconductor wafer;
- at least one buffer circuit arranged to share the same electrical power supply channel of a test equipment with electrical power supply inputs of a group of at least four integrated circuits among the plurality of integrated circuits to be tested;

- at least one group of at least four multiplexer circuits which are arranged so that the same high-voltage channel of the test equipment is shared with a first input of each of the four multiplexer circuits, a different data input/output electronic channel of the test equipment being in electrical communication with a second input of each of the four multiplexer circuits, and an output of each of the four multiplexer circuits being in electrical communication with a test input/output of an integrated circuit in said group of at least four integrated circuits among the plurality of integrated circuits to be tested.

In some particular embodiments, the probe card which conforms to the invention may furthermore comprise one or more of the following features, taken individually or in all possible technical combinations:

- each multiplexer circuit in a group of multiplexer circuits is configured to simultaneously connect the high-voltage channel of the test equipment with the test input/output of each integrated circuit in the group of at least four integrated circuits among the plurality of integrated circuits to be tested depending on a first value of a control signal.
- each multiplexer circuit in a group of multiplexer circuits is configured to sequentially connect the high-voltage channel of the test equipment with the test input/output of each integrated circuit in the group of at least four integrated circuits among the plurality of integrated circuits to be tested depending on a second value of a control signal.
- each multiplexer circuit in a group of multiplexer circuits is configured to simultaneously connect an electronic channel of the test equipment with the test input/output of each integrated circuit in the group of at least four integrated circuits among the plurality of integrated circuits to be tested depending on a third value of a control signal.
- the first value of the control signal corresponds to a static failure test of the integrated circuits to be tested by applying a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.
- the second value of the control signal corresponds to a measurement test of the integrated circuits to be tested with a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.

- the third value of the control signal corresponds to a current measurement of the integrated circuits to be tested with a voltage which is less than a threshold value, preferably less than a threshold value fixed at 4.5 V.
- the buffer circuits and/or the groups of multiplexer circuits are integrated into an interface card in electrical communication with said probe card.
- the probe card is further suitable for being in electrical communication with a test equipment of class B and/or C integrated circuits, and a plurality of class A integrated circuits to be tested according to ISO/IEC 7816-3:2006.
- the probe card is further suitable for being in electrical communication with a test equipment configured to test semiconductor mass storage and/or random-access memory architectures.

In a second aspect of the invention, a system for testing a plurality of integrated circuits on a semiconductor wafer comprising a test equipment and a probe card according to the first aspect of the invention is provided.

In a third aspect of the invention, alternative or additional methods for testing a plurality of integrated circuits on a semiconductor wafer are provided, notably:

- A method for testing a plurality of integrated circuits on a semiconductor wafer, said method comprising the following steps:
 - sharing an electrical power supply channel of a test equipment with electrical power supply inputs of a group of at least four integrated circuits among the plurality of integrated circuits to be tested;
 - connecting, in parallel, the same high-voltage channel of said test equipment with a test input/output of each integrated circuit in a group of at least four integrated circuits among the plurality of integrated circuits to be tested;
 - applying a voltage which is greater than a threshold value to a test input/output of each integrated circuit in said group of at least four integrated circuits;
 - verifying the operation of each of the integrated circuits by analyzing the response signals via their respective test input/output.

- A method for testing a plurality of integrated circuits on a semiconductor wafer, said method comprising the following steps:
 - sequentially connecting a high-voltage channel of said test equipment with a test input/output of each integrated circuit in a group of at least four integrated circuits among the plurality of integrated circuits to be tested;
 - sequentially applying a voltage which is greater than a threshold value to the test input/output of each integrated circuit in said group of at least four integrated circuits;
 - sequentially measuring a response of each of the integrated circuits by analyzing the response signals via their respective test input/output.
- A method for testing a plurality of integrated circuits on a semiconductor wafer, said method comprising the following steps:
 - connecting, in parallel, a data input/output electronic channel of a test equipment with a test input/output of each integrated circuit in a group of at least four integrated circuits among the plurality of integrated circuits to be tested;
 - sending, in parallel, a data frame to the test input/output of each integrated circuit in said group of at least four integrated circuits;
 - receiving, in parallel, a response data frame from each of the integrated circuits by analyzing the response signals via their respective test input/output.

In a fourth aspect of the invention, a computer program is provided comprising instructions which, when the program is executed by a computer, cause the latter to implement one of the methods according to the third aspect of the invention using a system according to the second aspect.

Brief description of the drawings

Figure 1 is a schematic depiction of a semiconductor wafer on which integrated circuits are formed.

Figure 2 is a schematic depiction of a group of four integrated circuits.

Figure 3 is a schematic depiction of a system for testing performance and failure of integrated circuits on a semiconductor wafer.

Figure 4 is a structural diagram of a probe card according to the first aspect of
5 the invention.

Figure 5 is a functional diagram of a probe card according to a first embodiment.

Figure 6 is a functional diagram of a probe card according to a second embodiment.

10 Figure 7 is a functional diagram of a probe card according to a third embodiment.

Detailed description of the embodiments

With reference to figure 1, the integrated circuits 1001, also called electronic
15 chips, are generally fabricated in series and in large quantities on a single semiconductor wafer 1000. Their arrangement is often according to a Hippodamian plan in which the circuits are arranged in columns 1002a-n and in rows 1003a-n so as to make it easier to locate them and make it possible to test several of them in parallel during performance and failure tests.

20 In the context of the present invention, what is meant by "integrated circuit" is an indivisible set of electronic components electrically interconnected and associated inseparably on a semiconductor substrate. The integrated circuit implements, by means of its components, logic operations for processing electromagnetic signals, notably electrical signals. It may be a programmable microcontroller or one or more
25 subelements such as a microprocessor, a random-access memory, a read-only memory, a fuse circuit, communication busses, flip-flop, latch or else buffer logic circuits, and other input/output (I/O) interface circuits.

With reference to figure 2, an integrated circuit 1001 comprises a certain number of inputs-outputs VCC, DQ, SPT. Certain of these inputs-outputs VCC, DQ
30 may be used during performance and failure test procedures and then subsequently during the implementation and the use of integrated circuits in electronic devices.

Other inputs-outputs SPT are dedicated only to performance and failure test procedures. The inputs-outputs have different functions. In the example of figure 2, the input/output VCC is an electrical power supply input, the input/output DQ is an input/output for exchanging data during the subsequent use of the circuit in electronic devices, and the input/output SPT is an input/output dedicated exclusively to procedures for testing performance and failure of the circuit 1001.

On the wafer 1000, the input-outputs of the circuits are connected to pads 2000 in order to make it possible to connect them to the pins of a probe card during the performance and failure test procedures. These pads may be dedicated only to the test procedures and not be intended to be used in the electronic device in which the circuit will subsequently be implemented. They may be arranged in the cutting areas of the wafer in order to be able to be eliminated during the packaging of the circuits, or simply be kept in the electronic device during packaging but remain unused.

With reference to figure 3, a system 3000 for testing performance and failure of integrated circuits 1001 on a semiconductor wafer 1000 comprises a holder or prober 3001 of a semiconductor wafer, a probe card 3002, an interface card 3003 and an automatic test equipment (ATE) 3004. The probe card 3002 has the shape of an electronic card provided with a plurality of pins or studs 3002a. The pins 3002a are brought into contact with the test pads (not depicted) which are specific to the integrated circuits 1001 and make it possible to redistribute the electrical signals exchanged between the test equipment 3004 and the integrated circuits 1001 via the interface card 3003. Their number and the dimensions correspond to the density and to the size of the test pads of the integrated circuits 1001.

During the operation of the system, the probe card 3002 generally remains fixed while the wafer 1000 comprising the integrated circuits 1001 is placed under the probe card by the holder or prober 3001 so as to establish electrical contact between the pads 2000 of the integrated circuits 1001 in a row of electrical circuits and the pins 3002a of the probe card 3002. Each test pad of an integrated circuit 1001 is thus placed in electrical communication with a channel 3004a of the test equipment 3004. By way of example, with reference to figure 2, the input/output VCC may be brought into electrical communication with an electrical power supply channel of the test equipment, and the input/output SPT be brought into electrical

communication with a high-voltage channel or an electronic channel of the test equipment. The number of channels of the test equipment generally conditions the number of integrated circuits which it is capable of testing simultaneously.

5 In the context of the present invention, what is meant by "channels" of a test equipment is the inputs-outputs of the test equipment which make it possible to exchange a set of data frames with electronic circuits, and/or to apply values of voltages and/or electric currents to the input of the integrated circuits.

10 In the context of the present invention, what is meant by "power supply channel" of a test equipment is a channel which makes it possible to deliver a voltage and/or an electric current which is sufficient to supply power to an integrated circuit and start it up. What is meant by "electronic channel" is a channel which makes it possible to exchange a data frame between said test equipment and a pad of an integrated circuit. What is meant by "high-voltage channel" of a test equipment is a channel which makes it possible to deliver a voltage which is higher than that of
15 one of its electronic channels. Notably, this type of channel may deliver voltages of several tens of volts, for example up to 30 volts.

As illustrated in figure 3, the probe card 3002 comprises a set of electrical circuits 3002b the function of which is to distribute the channels of the test equipment to the pads of the integrated circuits via the interface card.

20 In a first aspect of the invention, with reference to figures 3 & 4, a probe card 3002 for testing a plurality of integrated circuits 1001 on a semiconductor wafer 1000 is provided, said probe card 3002 comprising:

- a plurality of pins 3002a which are suitable for providing a temporary electrical connection with pads 2000 of a plurality of integrated circuits 1001 to be
25 tested on a semiconductor wafer 1000;
- at least one buffer circuit 4001a arranged to share the same electrical power supply channel SC1 of a test equipment 3004 with electrical power supply inputs VCC of a group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested;
- 30 - at least one group 4002 of at least four multiplexer circuits 4002a-d which are arranged so that the same high-voltage channel HVC1 of the test equipment

3004 is shared with a first input of each of the four multiplexer circuits 4002a-d, a different data input/output electronic channel DC1-4 of the test equipment 3004 being in electrical communication with a second input of each of the four multiplexer circuits 4002a-d, and an output of each of the four multiplexer circuits 4002a-d being in electrical communication with a test input/output SPT of an integrated circuit 1001a-d in said group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested.

For illustrative purposes, in figure 4, two buffer circuits 4001a, 4001b and two groups 4002, 4003 of multiplexer circuits are depicted. The number of buffer circuits and groups of multiplexer circuits depends on the number of high-voltage channels of the test equipment 3004. By way of example, for a test equipment such as the Magnum V EV marketed by Teradyne Inc.®, comprising 512 electronic channels, 128 high-voltage channels and 128 power supply channels, the number of buffer circuits and groups of multiplexer circuits may reach 512. The probe card 3002 according to the first aspect of the invention may be implemented with other types of test equipment, notably with test equipments comprising 1024 electronic channels, 256 high-voltage channels and 256 power supply channels. The number of integrated circuits which may be tested simultaneously using the probe card according to the first aspect of the invention may then reach 1024.

The number of integrated circuits per buffer circuit and per group of multiplexer circuits is at least four, with one multiplexer circuit per integrated circuit. Thus, in the configuration of the preceding example, a probe card 3002 according to the first aspect of the invention may make it possible to test 512 integrated circuits simultaneously by virtue of sharing the power supply channels and the high-voltage channels of the test equipment. The number of integrated circuits per buffer circuit and per group of multiplexer circuits may be higher. It may be equal to a power N of 2, where N is greater than 2.

A remarkable advantage of a probe card according to the first aspect of the invention is the possibility of carrying out static tests on integrated circuits, notably class A integrated circuits in the field of smart cards, using test equipments which are not suitable for implementing these tests on this type of integrated circuit. In the preceding example, the voltage delivered by the electronic channels of the Magnum V EV test equipment is suitable for class B and class C integrated circuits. The probe

card according to the first aspect of the invention makes it possible to use such a test equipment on a class A integrated circuit, in particular for a static performance or failure test on non-volatile, for example flash, memory elements of integrated circuits.

The multiplexer circuits 4002a-d, 4003a-d in each group 4002, 4003 are
5 configured to propagate one of their inputs to their output depending on the value of a control signal CS1, CS2. This operation may be executed differently according to the nature of the test implemented on the integrated circuits.

According to a first embodiment, with reference to figure 5, each multiplexer circuit in a group 4002 of multiplexer circuits 4002a-d is configured to simultaneously connect
10 the high-voltage channel HVC1 of the test equipment 3004 with the test input/output SPT of each integrated circuit in the group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested depending on a first value of a control signal CS1. Depending on a first value of a control signal CS1, the multiplexer circuits 4002a-d in the group 4002 propagate, simultaneously, and
15 therefore in parallel, the same high-voltage channel HVC1 at their output to the test input/output SPT of each integrated circuit 1001a-d.

This first embodiment is particularly suitable for implementing static failure tests on integrated circuits, notably on the memory elements of class A integrated circuits. Thus, according to a preferred variant, the first value of the control signal
20 CS1 corresponds to a static failure test of the integrated circuits to be tested by applying a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.

According to a second embodiment, which is an alternative or an addition to the first embodiment, with reference to figure 6, each multiplexer circuit in a group
25 4002 of multiplexer circuits 4002a-d is configured to sequentially connect the high-voltage channel HVC1 of the test equipment 3004 with the test input/output SPT of each integrated circuit in the group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested depending on a second value of a control signal CS1. Depending on a second value of the control signal CS1, the
30 multiplexer circuits 4002a-d in the group 4002 propagate the same high-voltage channel HVC1 at their output one after another, and therefore sequentially, to the

test input/output SPT of each integrated circuit 1001a-d. Integrated circuits are tested individually one after another.

This second embodiment is particularly suitable for implementing static performance tests on integrated circuits based on the measurement and the analysis of a response signal of an integrated circuit. Measuring the response signal may notably consist in measuring the voltage at the test input/output SPT of each integrated circuit 1001a-d. Thus, according to a preferred variant, which is notably applicable to class A integrated circuits, the second value of the control signal (CS1) corresponds to a measurement tests of the integrated circuits to be tested with a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.

According to a third embodiment, which is an alternative or an addition to the two other preceding embodiments, with reference to figure 7, each multiplexer circuit in a group 4002 of multiplexer circuits 4002a-d is configured to simultaneously connect an electronic channel DC1-4 of the test equipment 3004 with the test input/output SPT of each integrated circuit in the group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested depending on a third value of a control signal CS1. Depending on a third value of a control signal CS1, the multiplexer circuits 4002a-d propagate, simultaneously, and therefore in parallel, a data input/output electronic channel DC1-4 from the test equipment 3004 to the test input/output SPT of each integrated circuit in the group of at least four integrated circuits 1001a-d. A single data input/output electronic channel DC1-4 of the test equipment 3004 is used for each integrated circuit 1001a-d.

This third embodiment is particularly suitable for implementing current measurement tests on integrated circuits such as exchanging one or more data frames between the test equipment and the integrated circuits. The one or more data frames may consist of a succession of voltage values, the durations and values of which correspond to time constants and bit values, respectively. For example, the test equipment may communicate, via its electronic channels, instructions to integrated circuits to execute a succession of write and read operations in their memory element. In a preferred variant, the third value of the control signal CS1 corresponds to a current measurement of the integrated circuits to be tested with a

voltage which is less than a threshold value, preferably less than a fixed threshold value at 4.5 V.

In all of the embodiments and their variants described above, the buffer circuits 4001a, 4001b and the groups 4002, 4003 of multiplexer circuits form part of the probe card 3002. However, in certain systems 3000 for testing integrated circuits 1001, such as the one illustrated in figure 3, it may be common to resort to an interface card 3003 between the test equipment and the probe card 3002. Also, in certain alternative embodiments, the buffer circuits 4001a, 4001b and/or the groups 4002, 4003 of multiplexer circuits are integrated into an interface card 3003 in electrical communication with said probe card 3002.

A probe card 3002 according to the first aspect of the invention may operate with any type of suitable test equipment. Nevertheless, as mentioned above, an advantage of a probe card 3002 according to the first aspect of the invention is the possibility of carrying out static tests on class A integrated circuits 1001 in the field of smart cards, using test equipments which are not suitable for implementing these tests on this type of integrated circuit. Also, according to some preferred embodiments, which may be combined with all the embodiments described above, the probe card 3002 according to the first aspect of the invention is further suitable for being in electrical communication with a test equipment 3004 of class B and/or C integrated circuits 1001, and a plurality of class A integrated circuits to be tested according to ISO/IEC 7816-3:2006.

A probe card 3002 according to any one of the embodiments of the first aspect of the invention may be advantageously used to test any type of integrated circuit, in particular the non-volatile memory elements of integrated circuits.

According to some preferred embodiments, it may be further suitable for being in electrical communication with a test equipment 3004 configured to test semiconductor mass memory, for example flash memory, and/or random-access memory, architectures.

In a second aspect of the invention, a system 3000 for testing a plurality of integrated circuits 1001 on a semiconductor wafer 1000 is provided. The system comprises a probe card 3002 according to the first aspect of the invention and a test equipment 3004. The test equipment 3004 may be a test equipment for class A

integrated circuits 1001 or a test equipment for class B and/or C integrated circuits within the meaning of ISO/IEC 7816-3:2006.

In a third aspect of the invention, several alternative or additional methods for testing a plurality of integrated circuits on a semiconductor wafer are provided.

5 According to a first variant, a method for testing a plurality of integrated circuits 1001 on a semiconductor wafer 1000 is provided, said method comprising the following steps:

- sharing an electrical power supply channel SC1 of a test equipment 3004 with electrical power supply inputs VCC of a group of at least four integrated
10 circuits 1001a-d among the plurality of integrated circuits 1001 to be tested;
- connecting, in parallel, the same high-voltage channel HVC1 of said test equipment 3001 with a test input/output SPT of each integrated circuit in a group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested;
- 15 - applying a voltage which is greater than a threshold value to the test input/output SPT of each integrated circuit in said at least four integrated circuits 1001a-d;
- verifying the operation of each of the integrated circuits 1001a-d by analyzing the response signals via their respective test input/output SPT.

20 A method according to this first variant simultaneously subjects the integrated circuits to a static failure test by imposing on them a voltage which is greater than a threshold value via sharing of the same high-voltage channel of the test equipment. The method is notably suitable for implementing static failure tests on the non-volatile memory elements of class A integrated circuits. The threshold value of the
25 voltage may be advantageously fixed at 4.5 V.

According to a second variant, a method for testing a plurality of integrated circuits 1001 on a semiconductor wafer 1000 is provided, said method comprising the following steps:

- sequentially connecting a high-voltage channel HVC1 of a test equipment
30 3004 with a test input/output SPT of each integrated circuit in a group of at

least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested;

- sequentially applying a voltage which is greater than a threshold value to the test input/output SPT of each integrated circuit in said group of at least four integrated circuits 1001a-d;
- sequentially measuring the response of each of the integrated circuits 1001a-d by analyzing the response signals via their respective test input/output SPT.

A method according to this second variant successively subjects the integrated circuits to a performance test by imposing on them a voltage which is greater than a threshold value via sequential sharing of the same high-voltage channel of the test equipment. The method is particularly suitable for implementing static failure tests on the non-volatile memory elements of class A integrated circuits. The threshold value of the voltage may be advantageously fixed at 4.5 V.

According to a third variant, a method for testing a plurality of integrated circuits 1001a-d on a semiconductor wafer 1000 is provided, said method comprising the following steps:

- connecting, in parallel, a data input/output electronic channel DC1-4 of said test equipment 3004 with a test input/output SPT of each integrated circuit in a group of at least four integrated circuits 1001a-d among the plurality of integrated circuits 1001 to be tested;
- sending, in parallel, a data frame to the test input/output SPT of each integrated circuit in said group of at least four integrated circuits 1001a-d;
- receiving, in parallel, a response data frame from each of the integrated circuits 1001a-d by analyzing the response signals via their respective test input/output SPT.

A method according to this third variant simultaneously subjects the integrated circuits to a current measurement test by exchanging a data frame between the test equipment and the integrated circuits via the electronic channels of the test equipment. For example, the test equipment may communicate, via its electronic channels, instructions to integrated circuits, notably class A integrated circuits, to execute a succession of write and read operations in their memory element.

The methods according to the three preceding variants may alternatively or additionally be implemented by any means. Preferably, they are implemented using a system according to the second aspect of the invention. They may be implemented by the test equipment itself or by means of a data processing device configured to control the test equipment so that it executes their steps.

An example of a data processing device is a device which may be tasked with automatically executing sequences of arithmetic or logic operations in order to perform tasks or actions. This device, also called a computer, may comprise one or more central processing units (CPUs) and/or one or more graphics processors (GPUs) as well as at least one control device which is suitable for executing these operations. It may also comprise other electronic components such as input/output interfaces, non-volatile or volatile storage devices, and communication busses for transferring data between the internal components of the device or with external components. One of the input/output devices may be a user interface for human-machine interaction, for example a graphical user interface for displaying information which is understandable to humans. For implementing one or more of the methods according to the third aspect of the invention, the device may comprise an input/output interface in electronic communication with a test equipment, and optionally a probe card according to the first aspect of the invention.

In a fourth aspect of the invention, a computer program is provided comprising instructions which, when the program is executed by a computer, cause the latter, by means of a system according to the second aspect of the invention, to implement one or more of the methods according to the third aspect of the invention. The program may be stored in the memory of a data processing device as described above and be executed by the latter. Alternatively, it may be executed by the test equipment itself after it has been loaded into memory.

Any type of compiled or interpreted programming language may be used to implement the steps of the method according to the third aspect of the invention in a computer program. The computer program may form part of a software solution, that is to say a collection of executable instructions, codes, scripts or the like and/or databases.

The computer program may be stored on a recording medium which may be read by the computer or the test equipment. The recording medium is preferably a non-volatile memory, for example a hard disk or a semiconductor reader. It may be a removable storage medium or a non-removable storage medium forming part of the computer. It may also be a volatile memory inside a removable medium or form part of a computer used as a server from which executable instructions may be downloaded and, when they are executed by a computer, ensure that the computer executes a method according to the third aspect of the invention.

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Claims

1. A probe card (3002) for testing a plurality of integrated circuits (1001) on a semiconductor wafer (1000), said probe card (3002) comprising:
 - a plurality of pins (3002a) which are suitable for providing a temporary electrical connection with pads (2000) of a plurality of integrated circuits (1001) to be tested on a semiconductor wafer (1000);
 - at least one buffer circuit (4001a) arranged to share the same electrical power supply channel (SC1) of a test equipment (3004) with electrical power supply inputs (VCC) of a group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested;
 - at least one group (4002) of at least four multiplexer circuits (4002a-d) arranged so that the same high-voltage channel (HVC1) of the test equipment (3004) is shared with a first input of each of the four multiplexer circuits (4002a-d), a different data input/output electronic channel (DC1-4) of the test equipment (3004) being in electrical communication with a second input of each of the four multiplexer circuits (4002a-d), and an output of each of the four multiplexer circuits (4002a-d) being in electrical communication with a test input/output (SPT) of an integrated circuit (1001a-d) in said group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested.
2. The probe card (3002) as claimed in claim 1, such that each multiplexer circuit in a group (4002) of multiplexer circuits (4002a-d) is configured to simultaneously connect the high-voltage channel (HVC1) of the test equipment (3004) with the test input/output (SPT) of each integrated circuit in the group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested depending on a first value of a control signal (CS1).
3. The probe card as claimed in either one of claims 1 and 2, such that each multiplexer circuit in a group (4002) of multiplexer circuits (4002a-d) is configured to sequentially connect the high-voltage channel (HVC1) of the test equipment (3004) with the test input/output (SPT) of each integrated circuit in the group of at least four integrated circuits (1001a-d) among the plurality of

integrated circuits (1001) to be tested depending on a second value of a control signal (CS1).

4. The probe card (3002) as claimed in any one of claims 1 to 3, such that each multiplexer circuit in a group (4002) of multiplexer circuits (4002a-d) is configured to simultaneously connect an electronic channel (DC1-4) of the test equipment (3004) with the test input/output (SPT) of each integrated circuit in the group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested depending on a third value of a control signal (CS1).
5. The probe card (3002) as claimed in claim 2, such that the first value of the control signal (CS1) corresponds to a static failure test of the integrated circuits to be tested by applying a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.
6. The probe card (3002) as claimed in claim 3, such that the second value of the control signal (CS1) corresponds to a measurement test of the integrated circuits to be tested with a voltage which is greater than a threshold value, preferably greater than a threshold value fixed at 4.5 V.
7. The probe card (3002) as claimed in claim 4, such that the third value of the control signal (CS1) corresponds to a current measurement of the integrated circuits to be tested with a voltage which is less than a threshold value, preferably less than a threshold value fixed at 4.5 V.
8. The probe card (3002) as claimed in any one of claims 1 to 7, such that the buffer circuits (4001a, 4001b) and/or the groups (4002, 4003) of multiplexer circuits are integrated into an interface card (3003) in electrical communication with said probe card (3002).
9. The probe card (3002) as claimed in any one of claims 1 to 8, such that it is further suitable for being in electrical communication with a test equipment (3004) of class B and/or C integrated circuits (1001), and a plurality of class A integrated circuits to be tested according to ISO/IEC 7816-3:2006.
10. The probe card (3002) as claimed in any one of claims 1 to 9, such that it is further suitable for being in electrical communication with a test equipment

(3004) configured to test semiconductor mass storage and/or random-access memory architectures.

11. A system (3000) for testing a plurality of integrated circuits (1001) on a semiconductor wafer (1000) comprising a test equipment (3004) and a probe card (3002) as claimed in any one of claims 1 to 10.
12. A method for testing a plurality of integrated circuits (1001) on a semiconductor wafer (1000), said method comprising the following steps:
 - sharing an electrical power supply channel (SC1) of a test equipment (3004) with electrical power supply inputs (VCC) of a group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested;
 - connecting, in parallel, the same high-voltage channel (HVC1) of said test equipment (3004) with a test input/output (SPT) of each integrated circuit in a group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested;
 - applying a voltage which is greater than a threshold value at a test input/output (SPT) of each integrated circuit in said group of at least four integrated circuits (1001a-d);
 - verifying the operation of each of the integrated circuits (1001a-d) by analyzing the response signals via their respective test input/output (SPT).
13. A method for testing a plurality of integrated circuits (1001) on a semiconductor wafer (1000), said method comprising the following steps:
 - sequentially connecting a high-voltage channel (HVC1) of said test equipment (3004) with a test input/output (SPT) of each integrated circuit in a group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested;
 - sequentially applying a voltage which is greater than a threshold value at the test input/output (SPT) of each integrated circuit in said group of at least four integrated circuits (1001a-d);
 - sequentially measuring a response of each of the integrated circuits (1001a-d) by analyzing the response signals via their respective test input/output (SPT).

14. A method for testing a plurality of integrated circuits (1001a-d) on a semiconductor wafer (1000), said method comprising the following steps:
- connecting, in parallel, a data input/output electronic channel (DC1-4) of a test equipment (3004) with a test input/output (SPT) of each integrated circuit in a group of at least four integrated circuits (1001a-d) among the plurality of integrated circuits (1001) to be tested;
 - sending, in parallel, a data frame to the test input/output (SPT) of each integrated circuit in said group of at least four integrated circuits (1001a-d);
 - receiving, in parallel, a response data frame from each of the integrated circuits (1001a-d) by analyzing the response signals via their respective test input/output (SPT).
15. A computer program comprising instructions which, when the program is executed by a computer, cause the latter to implement the method as claimed in any one of claims 12 to 14 using a system as claimed in claim 11.