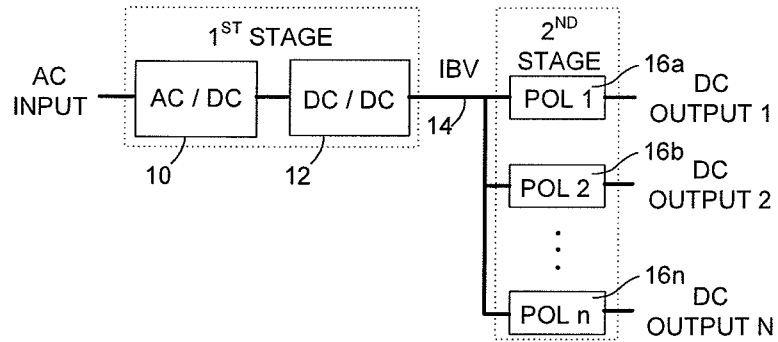
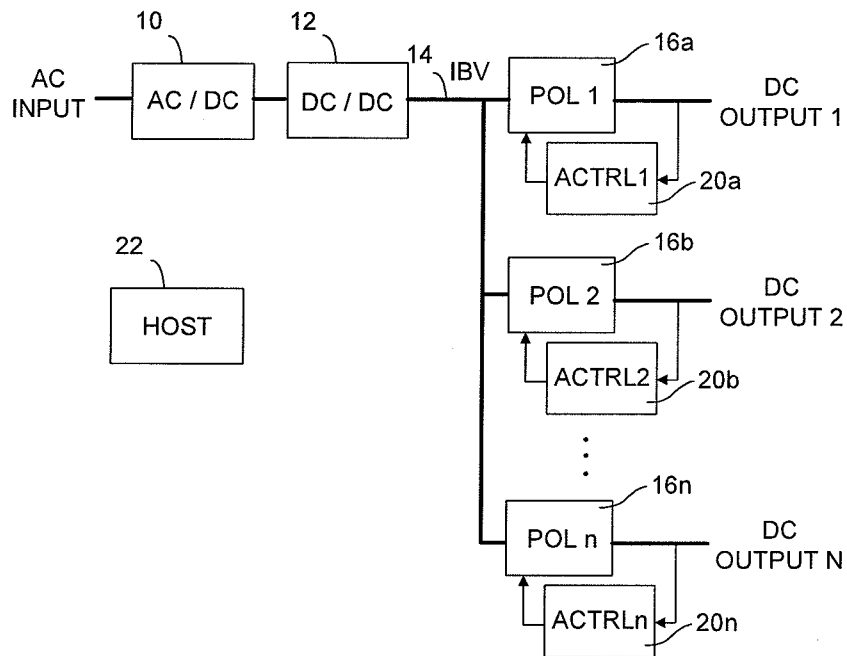


**Fig. 1****Fig. 2**

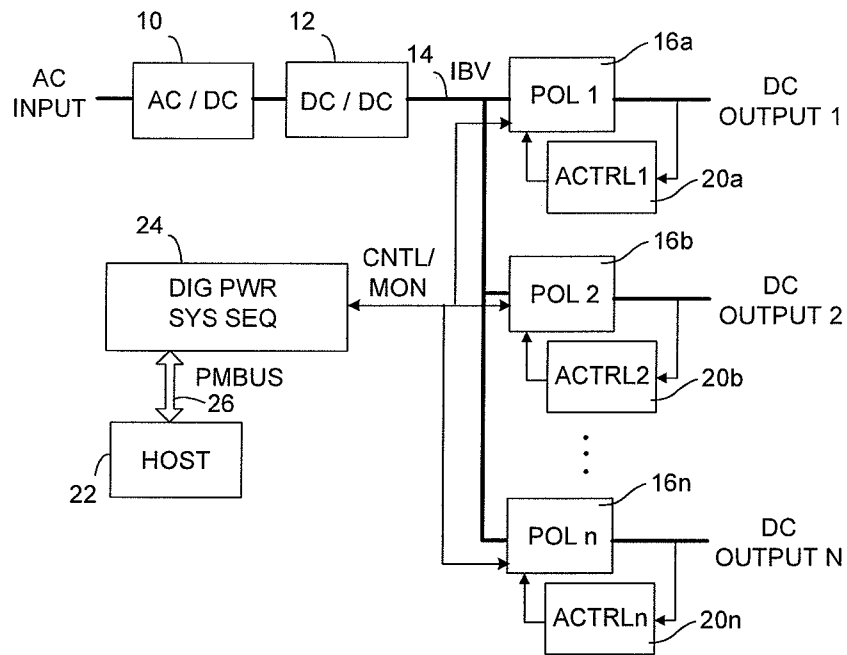


Fig. 3

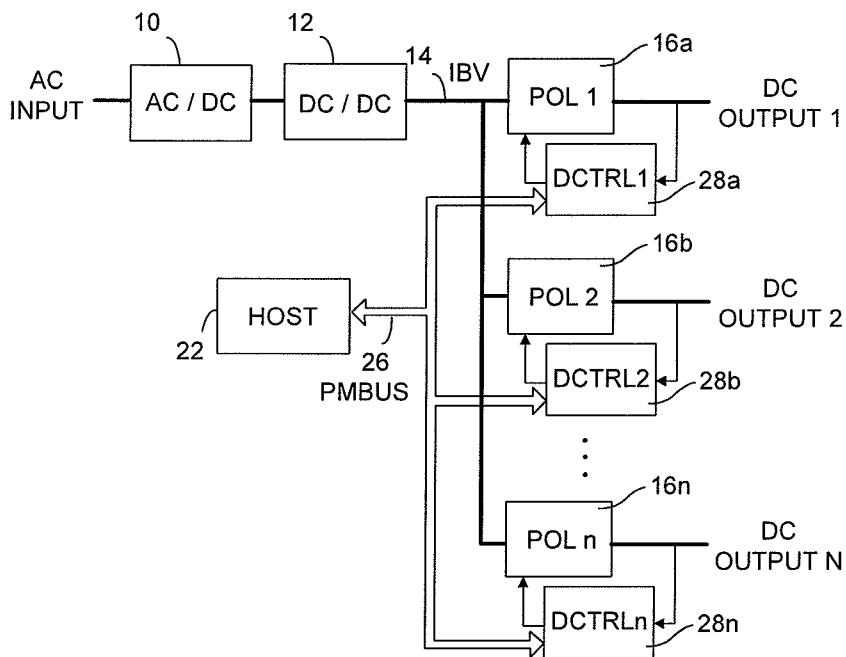


Fig. 4

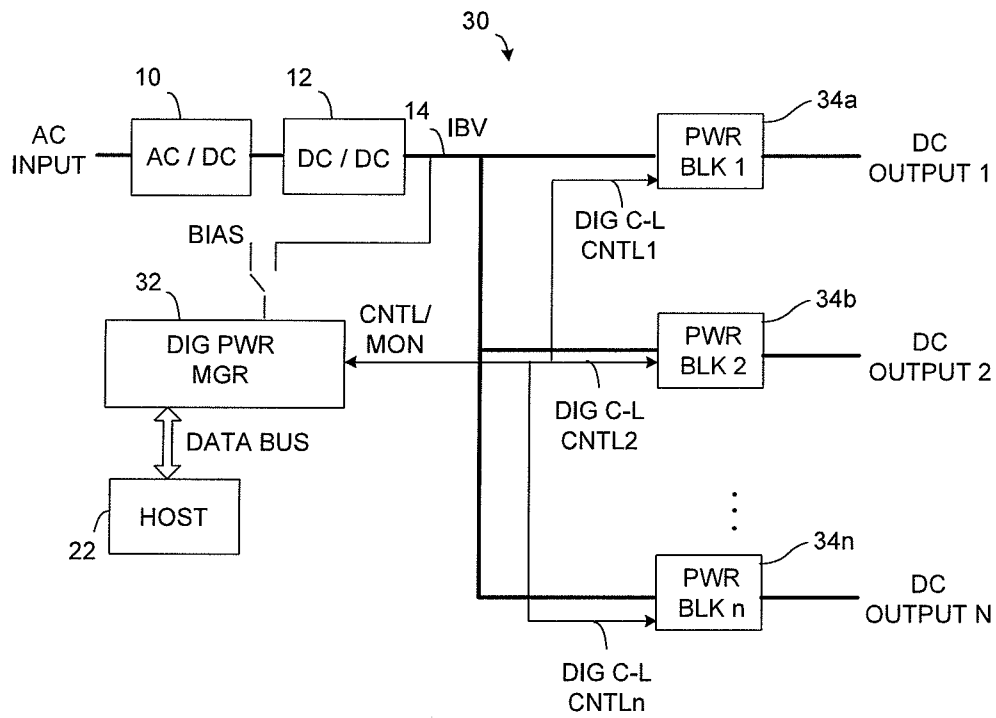


Fig. 5

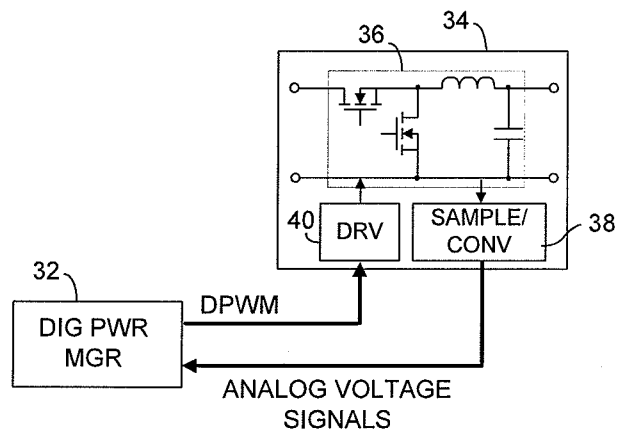


Fig. 6

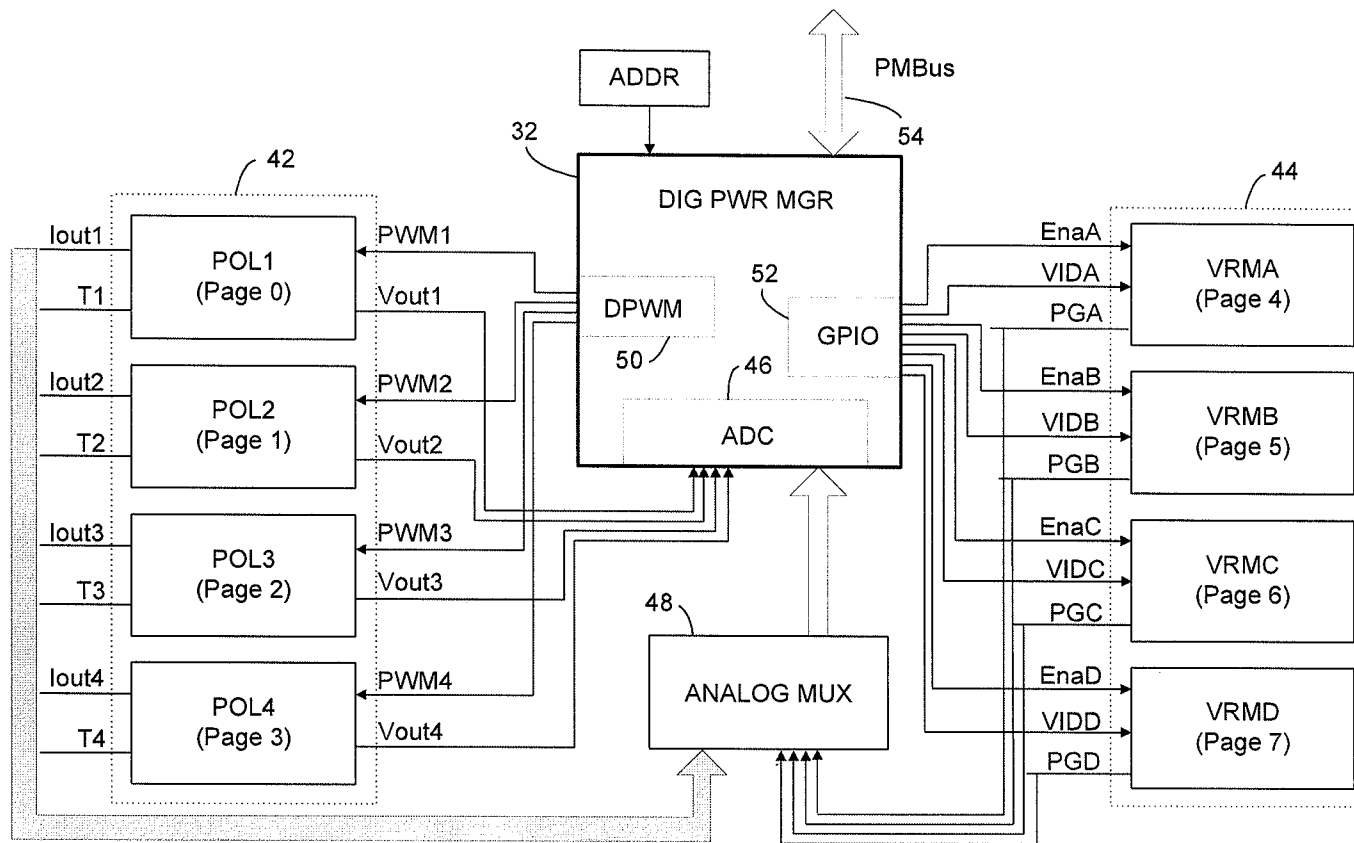


Fig. 7

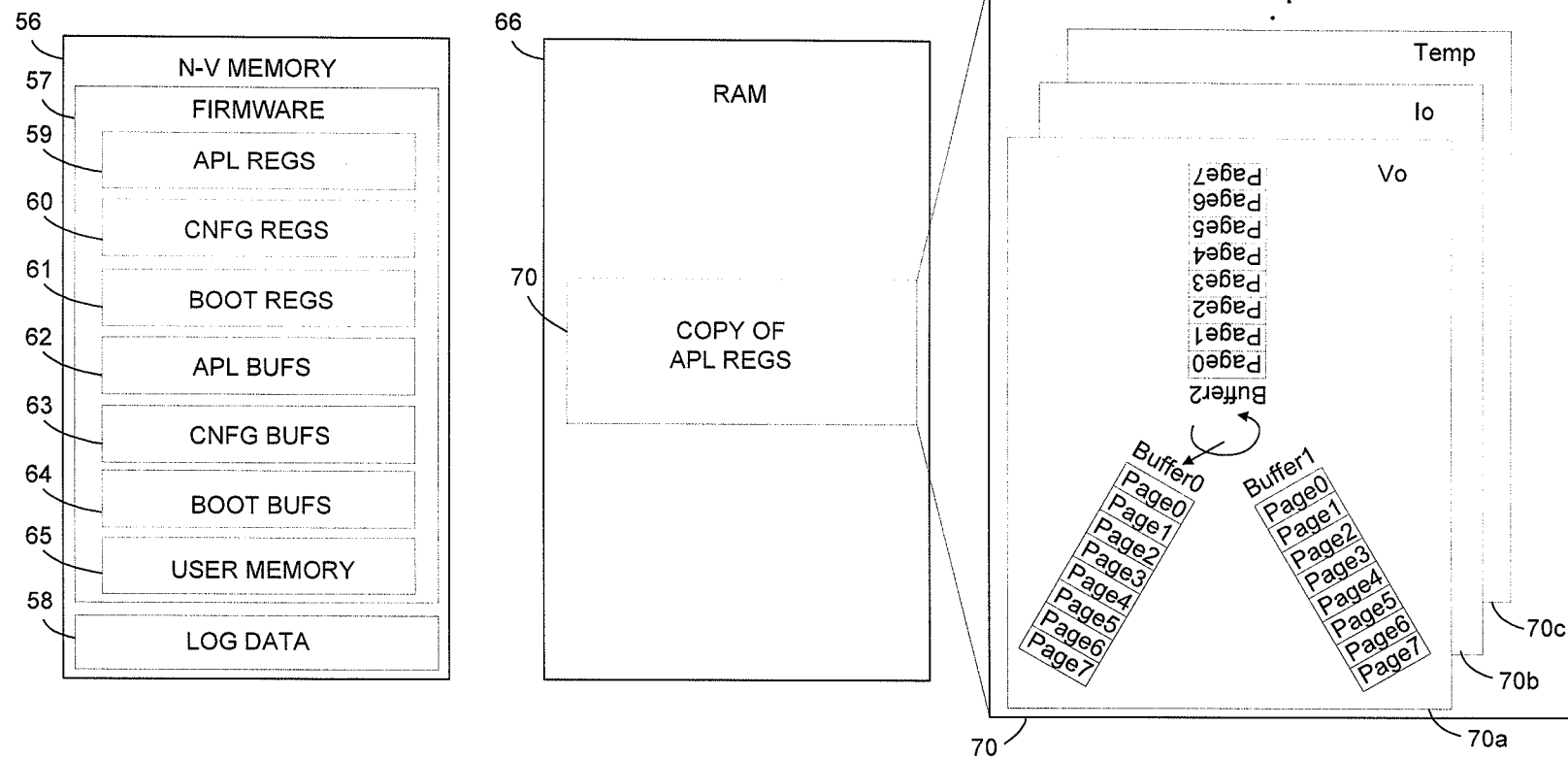
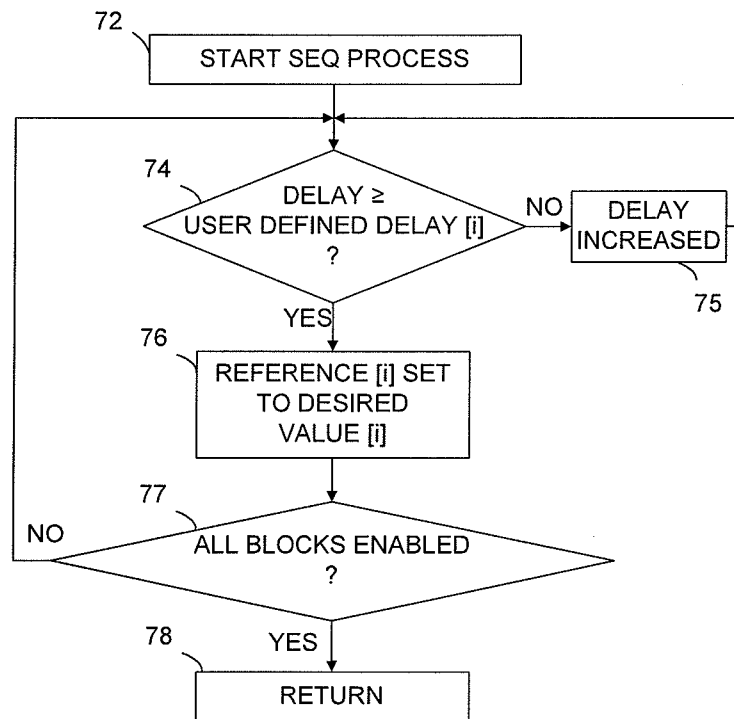
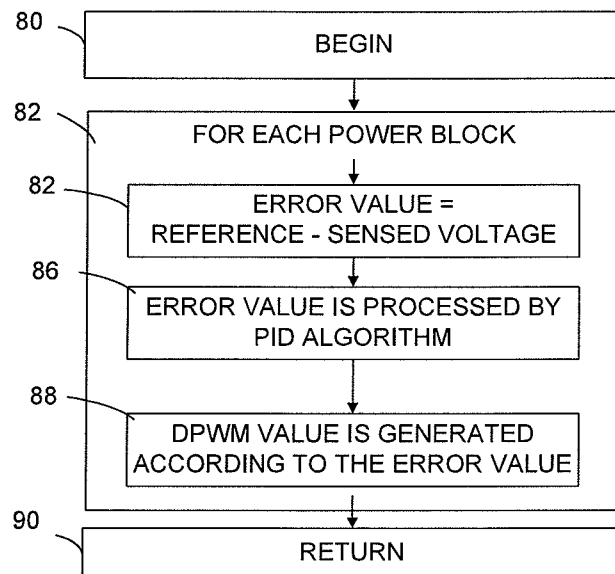


Fig. 8

**Fig. 9****Fig. 10**

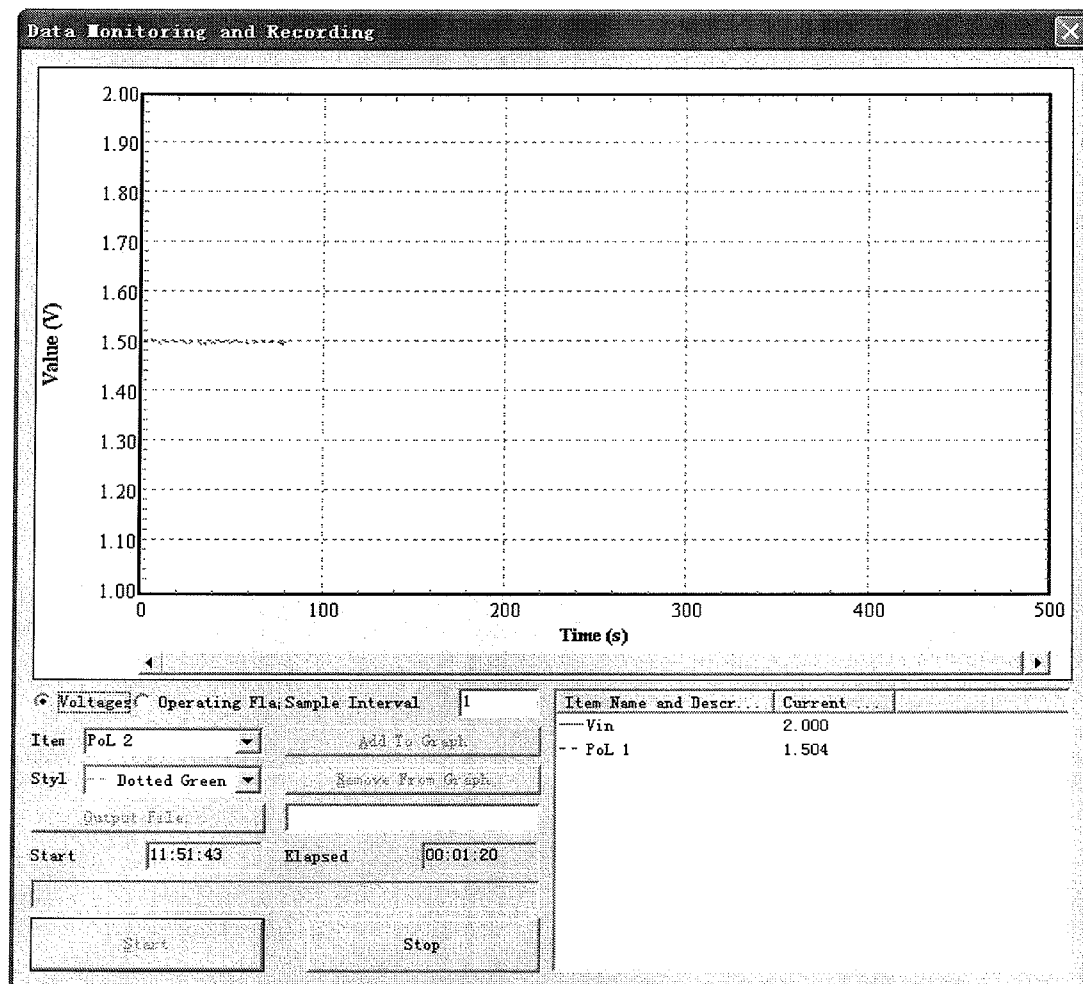


Fig. 11

Delay and Sequence Settings

	Analog z	Analog y	Analog x	VRM D	VRM C	VRM B	VRM A	InLk En	Pol 12	Pol 11	Pol 10	Pol 9	Pol 8	Pol 7	Pol 6	Pol 5	Pol 4	Pol 3	Pol 2	Pol 1	IO PIF	Delay (ms)	Sub Seq Rqd?	
Sequence 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	20	No
Sequence 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	20	No
Sequence 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	20	No
Sequence 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	20	No
Sequence 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	20	No
Sequence 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	20	No
Sequence 7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	20	No
Sequence 8	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	20	No
Sequence 9	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	20	No
Sequence 10	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	20	No
Sequence 11	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	20	No
Power Good Mask	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	0	10	No
Warning Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	No
Reset Signal A Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10	No
Reset Signal B Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	20	No
Reset Signal C Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	30	No
Low Pwr Shut Down	0	0	0	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0		No

OK
Cancel

Automatic edit next cell

I2C command power down delay 0

Delay From Reset In = H 10
Reset in = L, Reset is "instant"
Delay to Reset A (ARST) 10
Delay to Reset B (BRST) 20
Delay to Reset C (CRST) 30

Note: 1=Keep on during Low Power Mode, 0=Turn

Fig. 12

POL Settings

	Pol 1	Pol 2	Pol 3	Pol 4	Pol 5	Pol 6	Pol 7	Pol 8	Pol 9	Pol 10	Pol 11
Analog Setting	No	No	No	No	No	No	No	No	No	No	No
Alternate Voltage (Note 2)	No	No	No	No	No	No	No	No	No	No	No
Ra	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Rb	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Full Scale	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00
Voltage Setting	1.499	1.499	1.499	1.499	1.499	1.499	1.499	1.499	1.499	1.499	1.499
Margin Down %	49.9	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
Margin Up %	50.2	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
Warning Low %	25	90	90	90	90	90	90	90	90	90	90
Warning High %	157	110	110	110	110	110	110	110	110	110	110
Power Good Low %	16	88	88	88	88	88	88	88	88	88	88
Power Good High %	166	112	112	112	112	112	112	112	112	112	112
V Under Voltage	0.23	1.27	1.27	1.27	1.27	1.27	1.27	1.27	1.27	1.27	1.27
V Over Voltage	2.49	1.72	1.72	1.72	1.72	1.72	1.72	1.72	1.72	1.72	1.72
Default PwM %	50	50	50	50	50	50	50	50	50	50	50
Trim Logic (Note 1)	Negative	Negative	Negative	Negative	Negative	Negative	Negative	Negative	Negative	Negative	Negative
Comparator Logic											
Reference Voltage											
Ref Asserted Level											

OK Cancel

Automatic edit next cell

If V Under/Over Voltage is 0, Reference Circuit for Analog Monitoring Channels

Note 1: Positive Trim Logic Note: The higher the trim voltage, the higher the PoL output voltage.

Note 2: To enter alternate settings for Voltage Setting through V Over Voltage, enter the values as: settingA, settingB (i.e., 1.50, 1.35)

Fig. 13

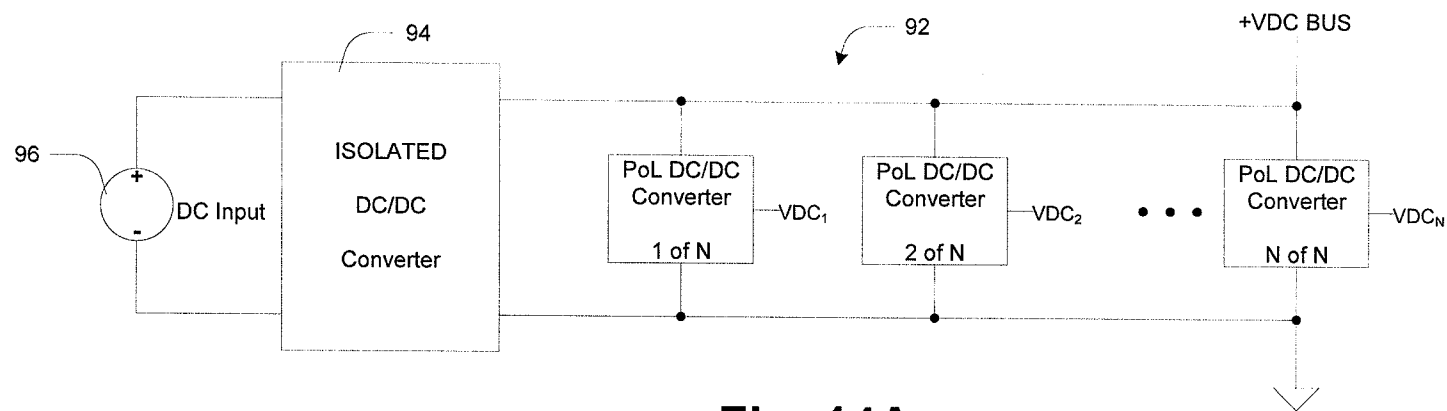


Fig. 14A

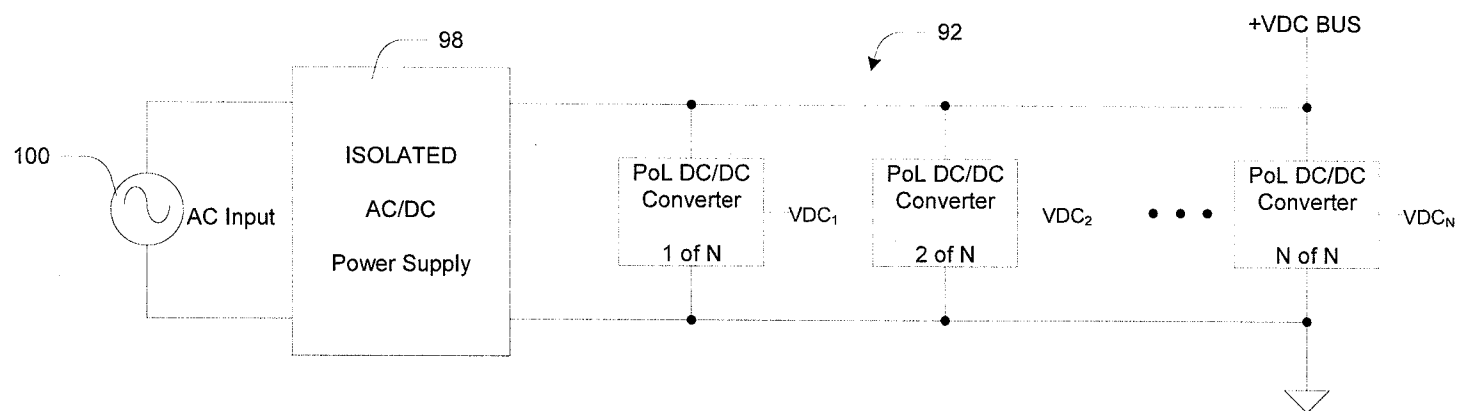


Fig. 14B

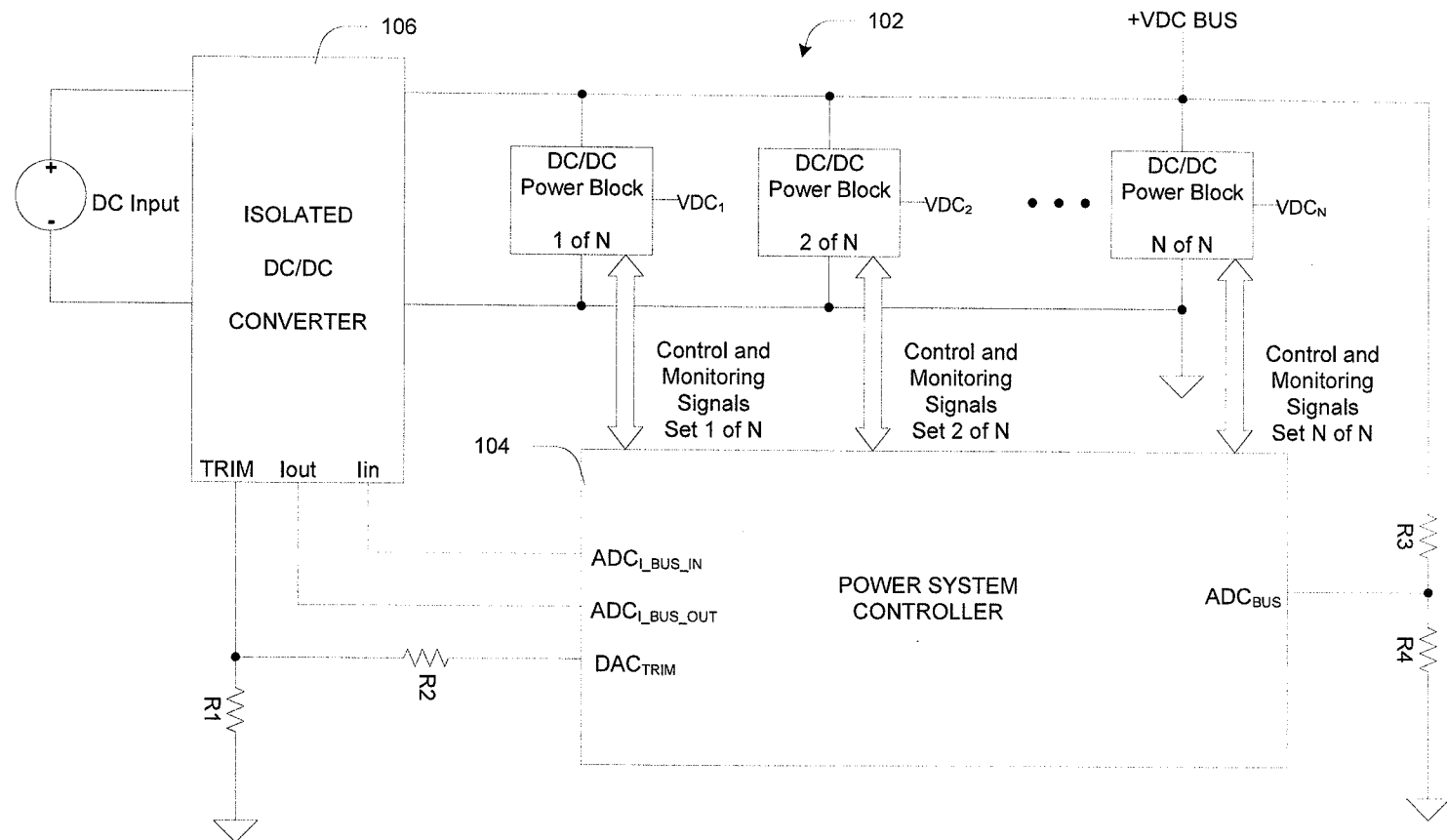


Fig. 15

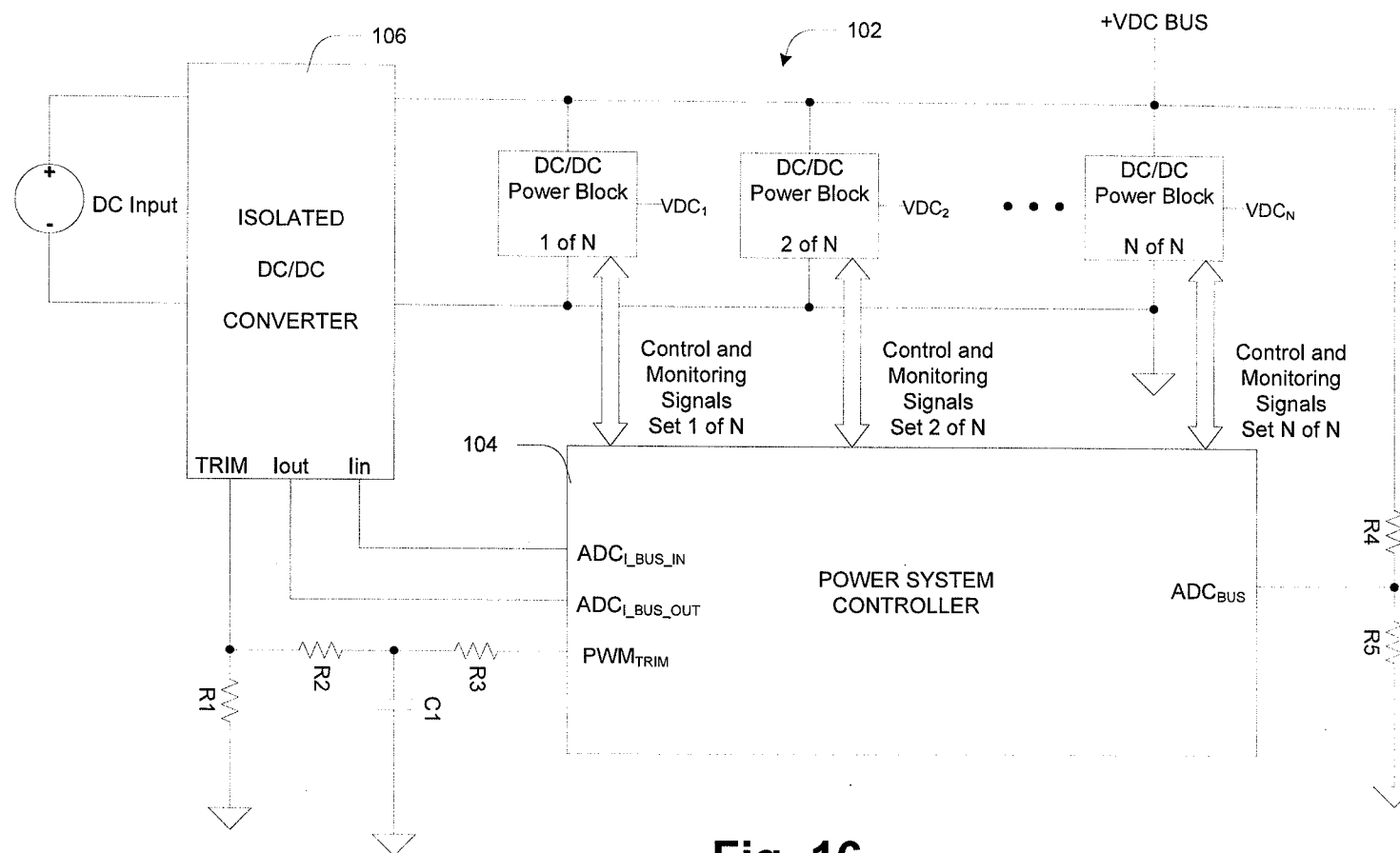


Fig. 16

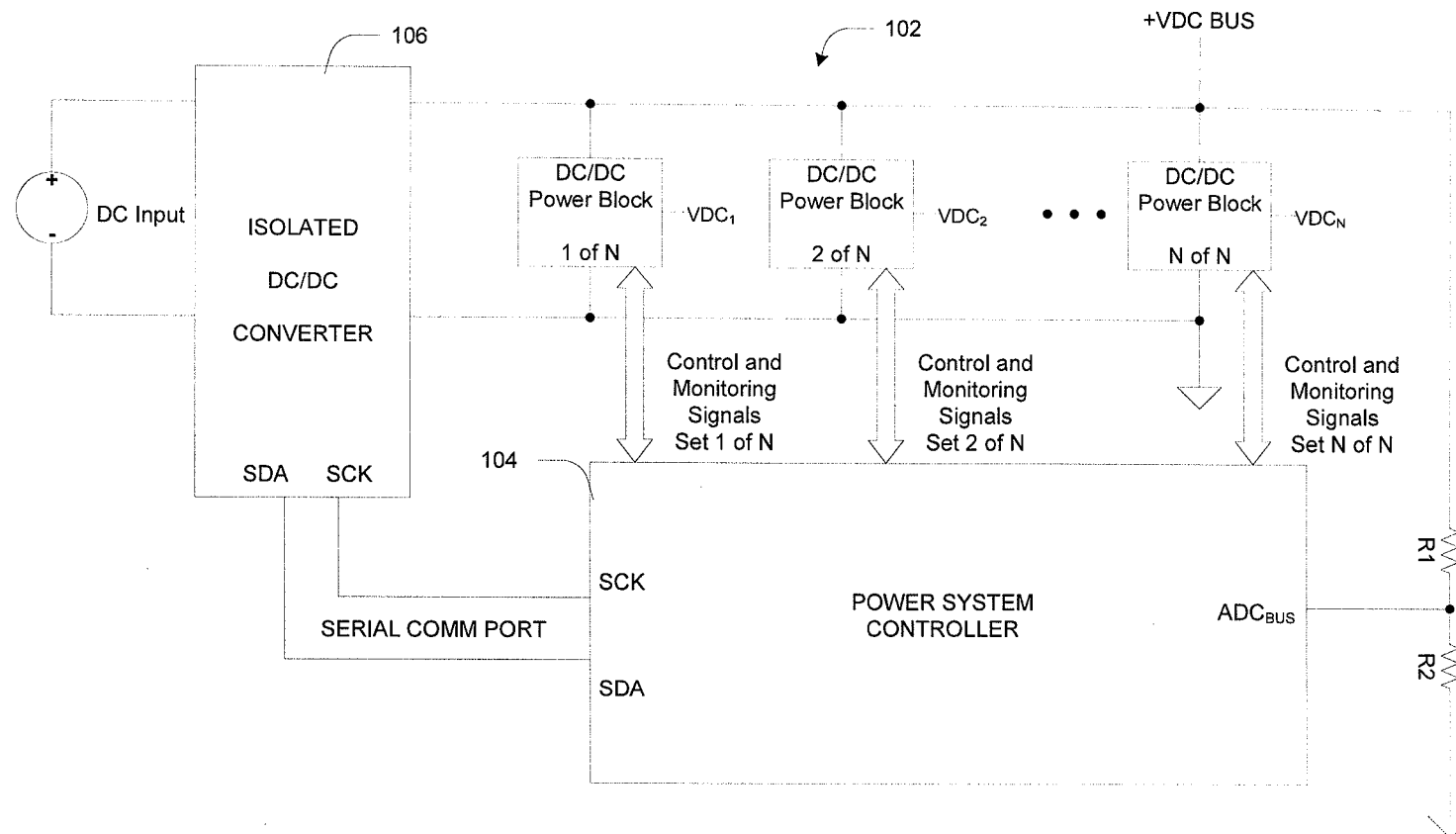


Fig. 17