CLAIMS

What is claimed is:

1. An electronic package, comprising:

a base substrate, the base substrate having a plurality of through substrate vias;

a first die over the base substrate;

a first cavity into the base substrate, wherein the first cavity is at least partially within a footprint of the first die; and

a first component in the first cavity.

2. The electronic package of claim 1, wherein the first component is a second die.

3. The electronic package of claim 2, wherein the second die comprises through substrate vias.

4. The electronic package of claim 2, wherein an active surface of the second die faces an active surface of the first die.

5. The electronic package of claim 2, wherein an active surface of the second die faces away from an active surface of the first die.

6. The electronic package of claim 1, wherein the first component is a passive electrical component.

7. The electronic package of claim 1, wherein the first component is a thermoelectric cooling (TEC) module.

8. The electronic package of claim 1, wherein the first cavity is entirely within the footprint of the first die.

9. The electronic package of claim 1, further comprising:

a second die over the base substrate.

10. The electronic package of claim 9, wherein the first cavity is at least partially within a footprint of the second die.

11. The electronic package of claim 9, wherein the first component electrically couples the first die to the second die.

12. The electronic package of claim 9, further comprising:

a second cavity into the base substrate, wherein the second cavity is entirely within the footprint of the first die.

13. The electronic package of claim 12, further comprising:

a second component in the second cavity.

14. The electronic package of claim 9, wherein the first die is electrically coupled to the second die by one or more traces on the base substrate.

15. The electronic package of claim 1, wherein the base substrate is a passive substrate.

16. The electronic package of claim 1, wherein the base substrate is an active substrate.

17. A method of forming an electronic package, comprising:

forming through substrate vias (TSVs) partially through a base substrate;

thinning the base substrate, wherein the TSVs are not exposed;

attaching a carrier to the base substrate;

forming a cavity into the base substrate, wherein the cavity exposes a plurality of pads;

attaching a component to the plurality of pads;

embedding the component within a mold layer;

planarizing the base substrate, wherein the planarizing exposes the TSVs;

removing the carrier; and

attaching a die to the base substrate.

18. The method of claim 17, wherein an active surface of the component faces an active surface of the die.

19. The method of claim 17, wherein the cavity is at least partially within a footprint of the die.

20. The method of claim 17, wherein the component is a second die.

21. The method of claim 20, wherein the second die comprises through substrate vias.

22. An electronic system, comprising:

a board;

an electronic package coupled to the board, wherein the electronic package comprises:

a base substrate, wherein the base substrate comprises through substrate vias (TSVs), and wherein the base substrate comprises silicon;

a first die over the base substrate;

a second die over the base substrate;

a first cavity into the base substrate, wherein the first cavity is at least partially within a footprint of the first die and at least partially within a footprint of the second die;

a first component in the first cavity;

a second cavity into the base substrate; and

a second component in the second cavity.

23. The electronic system of claim 22, wherein the first component electrically couples the first die to the second die.

~~24. The electronic system of claim 22, wherein the at least one of the first component and the second component comprises through substrate vias.~~

~~25. The electronic system of claim 22, wherein an active surface of the first die faces an active surface of the first component.~~

1. An electronic package, comprising:

a base substrate, the second side opposite the first side;

a component in a cavity of the base substrate, the component having a first side and a second side, the second side opposite the first side, and the component having a first sidewall and a second sidewall between the first side and the second side, the first sidewall laterally opposite the second sidewall;

a first plurality of through substrate vias in the base substrate, the first plurality of through substrate vias laterally spaced apart from the first sidewall of the component;

a second plurality of through substrate vias in the base substrate, the second plurality of through substrate vias laterally spaced apart from the second sidewall of the component;

a mold layer having a first portion laterally between the first plurality of through substrate vias and the first sidewall of the component, the first portion of the mold layer in contact with the first sidewall of the component, and the mold layer having a second portion laterally between the second plurality of through substrate vias and the second sidewall of the component, the second portion of the mold layer in contact with the second sidewall of the component;

a redistribution layer on the first side of the base substrate, the redistribution layer vertically over the component, vertically over the first plurality of through substrate vias, and vertically over the second plurality of through substrate vias;

a first plurality of interconnects coupling the first side of the component to the redistribution layer;

a first die over a first portion of the redistribution layer, the first die over the first plurality of through substrate vias and over a first portion of the component;

a second plurality of interconnects coupling the first die to the first portion of the redistribution layer;

a second die over a second portion of the redistribution layer, the second die over the second plurality of through substrate vias and over a second portion of the component;

a third plurality of interconnects coupling the second die to the second portion of the redistribution layer; and

a plurality of bumps beneath the second side of the base substrate, the plurality of bumps vertically beneath the second side of the component, vertically beneath the first plurality of through substrate vias, and vertically beneath the second plurality of through substrate vias.

2. The electronic package of claim 1, wherein the redistribution layer is electrically coupled to the first plurality of through substrate vias and to the second plurality of through substrate vias.

3. The electronic package of claim 1, wherein the redistribution layer is electrically coupled to the component by first level interconnects.

4. The electronic package of claim 1, further comprising:

a second mold layer laterally between the first die and the second die, the second mold layer beneath the first die and beneath the second die.

5. The electronic package of claim 4, wherein the second mold layer has an uppermost surface at a same level as an uppermost surface of the first die and at a same level as an uppermost surface of the second die.

6. The electronic package of claim 1, wherein the base substrate is a silicon substrate.

7. The electronic package of claim 1, wherein the mold layer is not in contact with the first plurality of through substrate vias and is not in contact with the second plurality of through substrate vias.

8. The electronic package of claim 1, wherein the mold layer has a bottommost surface at a same level as a bottommost surface of the component.

9. An electronic package, comprising:

a base substrate having a first side and a second side, the second side opposite the first side;

an embedded multi-die interconnect bridge in a cavity of the base substrate, the embedded multi-die interconnect bridge having a first side and a second side, the second side opposite the first side, and the embedded multi-die interconnect bridge having a first sidewall and a second sidewall between the first side and the second side, the first sidewall laterally opposite the second sidewall;

first vias in the base substrate, the first vias laterally spaced apart from the first sidewall of the embedded multi-die interconnect bridge;

second vias in the base substrate, the second vias laterally spaced apart from the second sidewall of the embedded multi-die interconnect bridge;

a first mold layer having a first portion laterally between the first vias and the first sidewall of the embedded multi-die interconnect bridge, the first portion of the first mold layer in contact with the first sidewall of the embedded multi-die interconnect bridge, and the first mold layer having a second portion laterally between the second vias and the second sidewall of the embedded multi-die interconnect bridge, the second portion of the first mold layer in contact with the second sidewall of the embedded multi-die interconnect bridge;

a redistribution layer on the first side of the base substrate, the redistribution layer electrically coupled to the embedded multi-die interconnect bridge, the redistribution layer on and electrically coupled to the first vias, and the redistribution layer on and electrically coupled to the second vias;

a first plurality of interconnects coupling the first side of the embedded multi-die interconnect bridge to the redistribution layer;

a first die over a first portion of the redistribution layer, the first die over the first vias and over a first portion of the embedded multi-die interconnect bridge;

a second plurality of interconnects coupling the first die to the first portion of the redistribution layer;

a second die over a second portion of the redistribution layer, the second die over the second vias and over a second portion of the embedded multi-die interconnect bridge;

a third plurality of interconnects coupling the second die to the second portion of the redistribution layer;

a second mold layer laterally between the first die and the second die, the second mold layer beneath the first die and beneath the second die; and

a plurality of bumps beneath the second side of the base substrate, the plurality of bumps vertically beneath the second side of the embedded multi-die interconnect bridge, vertically beneath the first vias, and vertically beneath the second vias.

10. The electronic package of claim 9, wherein the second mold layer has an uppermost surface at a same level as an uppermost surface of the first die and at a same level as an uppermost surface of the second die.

11. The electronic package of claim 9, wherein the base substrate is a silicon substrate.

12. The electronic package of claim 9, wherein the first mold layer is not in contact with the first vias and is not in contact with the second vias.

13. A method of fabricating an electronic package, the method comprising:

forming a base substrate having a first side and a second side, the second side opposite the first side;

providing a component in a cavity of the base substrate, the component having a first side and a second side, the second side opposite the first side, and the component having a first sidewall and a second sidewall between the first side and the second side, the first sidewall laterally opposite the second sidewall;

forming a first plurality of through substrate vias in the base substrate, the first plurality of through substrate vias laterally spaced apart from the first sidewall of the component;

forming a second plurality of through substrate vias in the base substrate, the second plurality of through substrate vias laterally spaced apart from the second sidewall of the component;

forming a mold layer having a first portion laterally between the first plurality of through substrate vias and the first sidewall of the component, the first portion of the mold layer in contact with the first sidewall of the component, and the mold layer having a second portion laterally between the second plurality of through substrate vias and the second sidewall of the component, the second portion of the mold layer in contact with the second sidewall of the component;

forming a redistribution layer on the first side of the base substrate, the redistribution layer vertically over the component, vertically over the first plurality of through substrate vias, and vertically over the second plurality of through substrate vias;

forming a first plurality of interconnects coupling the first side of the component to the redistribution layer;

providing a first die over a first portion of the redistribution layer, the first die over the first plurality of through substrate vias and over a first portion of the component;

forming a second plurality of interconnects coupling the first die to the first portion of the redistribution layer;

providing a second die over a second portion of the redistribution layer, the second die over the second plurality of through substrate vias and over a second portion of the component;

forming a third plurality of interconnects coupling the second die to the second portion of the redistribution layer; and

forming a plurality of bumps beneath the second side of the base substrate, the plurality of bumps vertically beneath the second side of the component, vertically beneath the first plurality of through substrate vias, and vertically beneath the second plurality of through substrate vias.

14. The method of claim 13, wherein the redistribution layer is electrically coupled to the first plurality of through substrate vias and to the second plurality of through substrate vias.

15. The method of claim 13, wherein the redistribution layer is electrically coupled to the component by first level interconnects.

16. The method of claim 13, further comprising:

forming a second mold layer laterally between the first die and the second die, the second mold layer beneath the first die and beneath the second die.

17. The method of claim 16, wherein the second mold layer has an uppermost surface at a same level as an uppermost surface of the first die and at a same level as an uppermost surface of the second die.

18. The method of claim 13, wherein the base substrate is a silicon substrate.

19. The method of claim 13, wherein the mold layer is not in contact with the first plurality of through substrate vias and is not in contact with the second plurality of through substrate vias.

20. The method of claim 13, wherein the mold layer has a bottommost surface at a same level as a bottommost surface of the component.