CLAIMS

1. A semiconductor structure, comprising:

a substrate on which at least one stacked structure is provided, the stacked structure comprising a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction; and

a plurality of leading wire posts, wherein at least two leading wire posts of the plurality of leading wire posts respectively are in contact with the different layers of memory cells in different memory cell groups.

2. The semiconductor structure according to claim 1, wherein

the leading wire posts are arranged along the first direction, and

the leading wire posts are lined up along the first direction.

3. The semiconductor structure according to claim 1, wherein

all the memory cells in a same memory cell group are in contact with at most one leading wire post of the plurality of leading wire posts.

4. The semiconductor structure according to claim 1, wherein

the number of the plurality of leading wire posts is equal to or greater than the number of layers of the memory cells, and each layer of memory cells at least comprises one memory cell in contact with the leading wire post.

5. The semiconductor structure according to claim 1, wherein

the number of leading wire posts in contact with one of the memory cell groups is less than the number of layers of the memory cells in the one memory cell group.

6. The semiconductor structure according to claim 1, wherein the first direction is

parallel to a surface of the substrate, and the second direction is perpendicular to the surface of the substrate;

the stacked structure further comprises a plurality of horizontal signal lines and a plurality of vertical signal lines, wherein the plurality of horizontal signal lines are arranged in the second direction and extend along the first direction, and each of the horizontal signal lines is connected to one layer of memory cells, and the vertical signal lines extend along the second direction and are connected to multiple layers of memory cells in a same memory cell group; and

the leading wire posts are electrically connected to the horizontal signal lines.

7. The semiconductor structure according to claim 6, wherein

each of the memory cells comprises a channel region and a source/drain doped region arranged in a third direction, the source/drain doped region is arranged at two sides of the channel region, and the third direction is parallel to the surface of the substrate.

8. The semiconductor structure according to claim 7, wherein

each of the plurality of horizontal signal lines is a bit line, and each of the plurality of vertical signal lines is a word line,

the bit line is connected to the source/drain doped region, and the word line is connected to the channel region; and

at least one of the plurality of leading wire posts penetrates through the source/drain doped region in at least one of the memory cells, wherein

the source/drain doped region comprise a first source/drain doped region and a second source/drain doped region, the first source/drain doped region is located between the bit line and the channel region, and the second source/drain doped region is located at a side of the channel region deviating away from the first source/drain

doped region; and

the leading wire post penetrates through the first source/drain doped region.

9. The semiconductor structure according to claim 7, wherein

each of the plurality of horizontal signal lines is a word line, and each of the plurality of vertical signal lines is a bit line,

the bit line is connected to the source/drain doped region, and the word line is connected to the channel region; and

at least one of the plurality of leading wire posts penetrates through the channel region in at least one of the memory cells.

10. The semiconductor structure according to claim 7, wherein the memory cell further comprises a bit line contact area, the bit line contact area connecting the bit line to the source/drain doped region, wherein at least one of the plurality of leading wire posts penetrates through the bit line contact area in one of the memory cells.

11. The semiconductor structure according to claim 1, wherein

the numbers of memory cells which the at least two leading wire posts penetrate through are different from each other.

12. The semiconductor structure according to claim 1, wherein

two adjacent leading wire posts of the plurality of leading wire posts are at least spaced by one of the plurality of memory cell groups, wherein

the number of memory cells between the two adjacent leading wire posts is fixed, or

the area of a directly facing region between the two adjacent leading wire posts is directly proportional to the number of memory cell groups between the two adjacent

leading wire posts.

13. The semiconductor structure according to claim 6, wherein

the number of stacked structures is greater than one, the plurality of horizontal signal lines of a same stacked structure comprises a first horizontal signal line to N-th horizontal signal line successively arranged in the second direction, N being a positive integer greater than 1; and

two stacked structures of the stacked structures constitute a structure module, the structural module further comprises a plurality of wires, the wire connects two leading wire posts, which are in contact with different stacked structures of the stacked structures, of the plurality of leading wire posts, and a sum of sequence numbers of the two horizontal signal lines electrically connected to the two leading wire posts being N+1.

14. The semiconductor structure according to claim 13, wherein

the two leading wire posts connected by the wire are arranged to be faced directly, and an extension direction of the wire is perpendicular to the first direction.

15. The semiconductor structure according to claim 13, wherein the memory cell comprises a transistor and a capacitor arranged in a third direction,

in a same structure module, the transistor of one stacked structure in the structure module is arranged facing to the transistor of another stacked structure in the structure module; or

in a same structure module, the transistor of one stacked structure in the structure module is arranged in a same direction as the transistor of another stacked structure in the structure module; or

in a same structure module, the transistor of one stacked structure in the structure module is arranged in an opposite direction to the transistor of another stacked

structure in the structure module.

16. The semiconductor structure according to claim 1, wherein at least one of the plurality of leading wire posts extends in the second direction and penetrates through at least one memory cell in the memory cell group,

the semiconductor structure further comprises a dielectric layer arranged between the leading wire post and the memory cell through which the leading wire post penetrates.

17. The semiconductor structure according to claim 16, wherein a bottom surface of the leading wire post is in contact with the memory cell, or at least a part of a side surface of the leading wire post is in contact with the memory cell.

18. The semiconductor structure according to claim 1, wherein the memory cells in contact with the at least two of the plurality of leading wire posts are arranged in a same memory cell group.

19. A method for manufacturing a semiconductor structure, comprising:

providing a substrate,

forming at least one stacked structure on the substrate, the stacked structure comprising a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction; and

forming a plurality of leading wire posts, wherein the at least two leading wire posts of the plurality of leading wire posts respectively are in contact with different layers of memory cells in different memory cell groups.

20. A semiconductor structure, comprising:

a substrate on which at least one stacked structure is provided, the stacked

structure comprising a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction; and

a plurality of leading wire posts, wherein the at least two leading wire posts of the plurality of leading wire posts are in contact with different memory cells in a same memory cell group.