ABSTRACT

SINGLE DAMASCENE METHOD FOR RF IC PASSIVE COMPONENT INTEGRATION IN COPPER INTERCONNECT PROCESS

A method of integrated circuit component integration in copper interconnects, including the following steps of the first embodiment. A wafer is provided having an exposed top-most planar copper interconnect. The wafer being divided into one or more areas selected from the group consisting of: a spiral inductor area having an exposed planar copper interconnect bottom half of a stacked spiral inductor; a MIM capacitor area having an exposed planar copper interconnect bottom plate and an exposed planar copper interconnect contact point of a MIM capacitor; and a precision resistor area having a two exposed planar copper interconnect routing points of a precision resistor. A first insulator layer is formed over the structure. A metal layer is formed over the first insulator layer. A first patterned masking layer is formed over the metal layer covering at least a portion of the MIM capacitor area exposed planar copper interconnect bottom plate and at least a portion of the area between the precision resistor area planar copper interconnect routing points. The metal layer over the first dielectric insulator layer is etched, without substantially etching the underlying first dielectric insulator layer, using the patterned first masking layer as a mask, to form a metal top plate over at least a portion of the interconnect bottom plate of a MIM capacitor and a patterned metal layer portion between the two planar copper interconnect routing points of a precision resistor. A second insulator layer is formed over the structure. A second patterned masking layer is formed over the second insulator layer exposing portions of the second insulator layer over: the planar copper interconnect bottom half of a stacked spiral inductor; at least a portion of the metal top plate and at least

a portion of the planar copper interconnect contact point of a MIM capacitor; and the two exposed planar copper interconnect routing points of a precision resistor. The second insulator layer is etched using the second patterned masking layer as a mask to form: an inductor trench exposing the planar copper interconnect bottom half of a stacked spiral inductor; a MIM capacitor trench exposing at least a portion of the metal top plate and at least a portion of the planar copper interconnect contact point of a MIM capacitor; and routing point trenches exposing the two exposed planar copper interconnect routing points of a precision resistor. The inductor trench, MIM capacitor trench and the routing point trenches are filled with planarized metal to complete formation of the following devices as selected: the spiral inductor within the spiral inductor area; the MIM capacitor within the MIM capacitor area; and the precision resistor within the precision resistor area.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)