

## Abstract of the Disclosure

### **MEMORY TESTING APPARATUS AND METHOD**

Provided are a memory device testing apparatus and method of operating such an apparatus that can reduce the time required to test a memory device such as a DRAM. The memory testing apparatus includes a pattern generator, a test head, an address pointer, a selector, a failure memory, a failure bit counter and a controller for coordinating the operation of the various elements. Depending on the signals received from the controller, the pattern generator will generate background pattern(s) or test patterns and address information that are, in turn, output to the memory device under test and the selector. During functional testing of the memory device, failure data is accumulated in a failure memory and subsequently output to a failure bit counter using address information from the address pointer while the background or test pattern is being written to the memory device.