CLAIMS

1. A chip, comprising: a plurality of interconnection structures, wherein each of the interconnection structures is connected to at least two processing cores, and all processing cores connected to one interconnection structure are one processing core group;

wherein the processing cores belonging to a same processing core group perform data transmission therebetween through the interconnection structure connected to the processing core group;

wherein, the plurality of the interconnection structures are not directly connected to one another;

the plurality of interconnection structures include a first interconnection structure and a second interconnection structure;

the first interconnection structure is connected to a first processing core;

the first processing core is connected to the second interconnection structure;

the first interconnection structure is further connected to a second processing core; the second interconnection structure is connected to a third processing core; and

the second processing core performs data transmission with the third processing core through the first processing core.

2. The chip according to claim 1, wherein data is capable of being transmitted among processing cores belonging to different processing core groups.

3. The chip according to claim 1, wherein

the plurality of interconnection structures include a third interconnection structure; and

all processing cores connected to the third interconnection structure are not connected to the other interconnection structures.

4. The chip according to any one of claims 1-3, wherein bandwidth of the interconnection structure meets bandwidth requirement of each of the processing cores in the processing core group connected to the interconnection structure.

5. The chip according to claim 4, wherein each of the processing cores comprises at least one transmission unit, and bandwidth of the interconnection structure meets bandwidth requirement of the transmission unit of each processing core connected to the interconnection structure.

6. The chip according to any one of claims 1-5, wherein the plurality of the interconnection structures are provided with at least two clock frequencies; and/or

the plurality of the interconnection structures are provided with at least two bit-width values.

7. A circuit board, comprising one or more chips according to any one of claims 1-6.

8. An electronic device, comprising one or more circuit boards according to claim 7.

9. An inter-core data transmission method, applicable to the chip according to any one of claims 1-6, comprising:

performing data transmission among the processing cores belonging to the same processing core group through the interconnection structure connected to the processing core group; and

performing data transmission between two processing cores belonging to two different processing core groups respectively through at least two of the interconnection structures;

wherein performing data transmission between the two processing cores belonging to two different processing core groups respectively through at least two of the interconnection structures, comprises:

performing data transmission between the two processing cores belonging to two different processing core groups respectively through two interconnection structures via a processing core that belongs to both of the two different processing core groups.

10. A computer storage medium storing a computer program, which, upon execution by a processor, implements the steps of the inter-core data transmission method according to claim 9.

11. An electronic device, comprising a memory, a processor, and a computer program stored in the memory and executable by the processor, wherein the processor executing the program implements the steps of the inter-core data transmission method according to claim 9.

12. A computer program product, comprising computer instructions, wherein, when the computer instructions are executed by a computing device, the computing device performs the steps of the inter-core data transmission method according to claim 9.