



- (51) **International Patent Classification:**
H03K 17/16 (2006.01) *H03K 19/003* (2006.01)
- (21) **International Application Number:**
PCT/US2014/054524
- (22) **International Filing Date:**
8 September 2014 (08.09.2014)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
14/025,529 12 September 2013 (12.09.2013) US
- (71) **Applicant:** MICRON TECHNOLOGY, INC. [US/US];
8000 South Federal Way, P. O. Box 6, Boise, ID 83707 (US).
- (72) **Inventor:** LAURENT, Christophe, Vincent Antoine;
C/O MICRON TECHNOLOGY, INC., 8000 South Federal Way, P. O. Box 6, Boise, ID 83707 (US).
- (74) **Agents:** ALTMAN, Daniel, E. et al.; KNOBBE, MARTENS, OLSON & BEAR, LLP, 2040 Main Street, 14th Floor, Irvine, CA 92614 (US).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

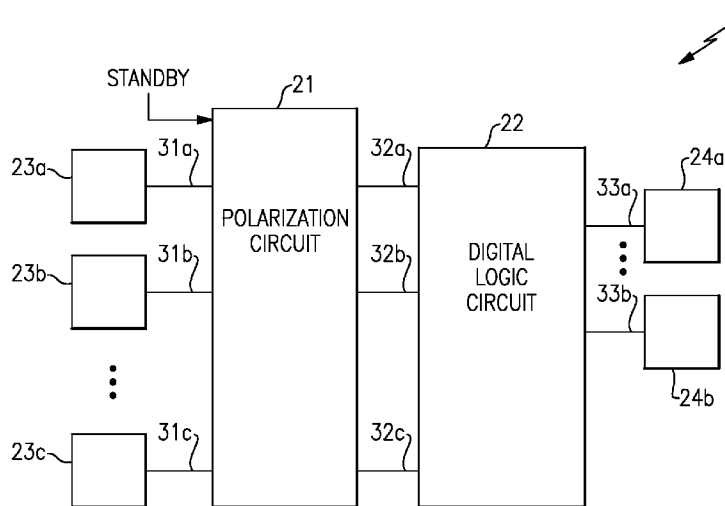
Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) **Title:** APPARATUS AND METHODS FOR LEAKAGE CURRENT REDUCTION IN INTEGRATED CIRCUITS

**FIG.3**

(57) **Abstract:** This disclosure relates to leakage current reduction in integrated circuits (ICs). In one aspect, an IC can include a digital logic circuit and a polarization circuit. The digital logic circuit can have a plurality of inputs and can include a plurality of logic gates. The polarization circuit can receive a standby signal and a digital input signal comprising a plurality of bits. When the standby signal is deactivated, the polarization circuit can control the plurality of inputs of the digital logic circuit based on the digital input signal. However, when the standby signal is activated the polarization circuit can control the plurality of inputs of the digital logic circuit to a low power state associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the digital logic circuit.