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(54) CHARGE-COUPLED AREA ARRAY

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94042, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge-coupled area arrays and, more particularly, to charge-coupled area imaging semiconductor device arrays utilizing light-sensitive charge-coupled device (CCD) elements and shift register charge-coupled (CCD) elements.

Several patent specifications and other publications describe the basic theory of operation of the charge-coupled semiconductor device. These publications include an article by Boyle and Smith published in the April, 1970 *Bell System Technical Journal*, page 587, entitled "Charge-Coupled Semiconductor Devices"; a paper on page 593 of the same *Bell System Technical Journal* by Amelio et al entitled "Experimental Verification of all Charge-Coupled Device Concept"; and U.S. Patent 3728590.

A linear imaging array which utilizes a single line of light-sensitive elements in combination with a pair of vertical registers located on opposite sides of the line of light-sensing elements is disclosed and described in Application 2710/74 (Serial Number 1453341). This Application discloses a technique for providing a linear (single line) array of light-sensitive elements; however, a need existed for providing an area array imaging semiconductor device that used a plurality of lines of light-sensitive elements. This need became very evident as it became more important to transmit pictures electronically by electronic communication apparatus. Pictures made up, for example, of 10,000 black or white dots could not be sent previously with the use of a single light-sensitive line imaging semiconductor device that did not have a mechanical scanning device associated therewith. These types of pictures were previously sent with the use of large, complex and rather and expensive electron or CRT types of devices.

Accordingly, this invention provides an imaging array comprising a plurality of lines of light-sensitive charge-coupled elements associated with portions of a semiconductor substrate, a plurality of shift register lines each having a plurality of charge-coupled elements associated with other portions of the semiconductor substrate, each one of the shift register charge-coupled elements being located adjacent and having a one-to-one correspondence with a particular one of the light-sensitive charge-coupled elements, and means for transferring charge packets generated in the light-sensitive charge-coupled elements to the particular corresponding charge-coupled elements of the shift register lines for subsequent movement within the shaft register lines to an output portion of the array.

The imaging array of the invention preferably includes means for shifting the charge packets along the shift register lines and means for receiving the charge packets at the end of the shift register lines. The means for transferring charge packets generated in the light-sensitive elements to corresponding CCD elements conveniently comprises a pair of light-transparent gate electrode means associated with each of the light-sensitive elements. Preferably, each of the pair of light-transparent gate electrode means comprises a doped polycrystalline silicon electrode. Preferably, the light-sensitive elements of the array have both a region of one conductivity type located in a

region or substrate of opposite type conductivity, and a higher resistivity barrier region of the same one conductivity type located adjacent to the first region.

An imaging system including an imaging array embodying the invention can further include output register means, preferably of CCD elements, electrically connected to the imaging array for receiving and further transferring the charge packets coming from the output portion of the array. Additionally the system can include input register means and electrical input signal means for transferring electrical input signals into the array in the event electrical signals rather than light are used as an input to the system.

The invention will be readily understood from the following illustrative description and the accompanying drawing, in which:—

Fig. 1 is a sectional view, in elevation, showing a single light-sensitive CCD element located in one of the plurality of lines of light-sensitive CCD elements of a CCD area imaging array adjacent to a corresponding single shift register CCD element located in one of the plurality of lines of shift register elements of the same CCD area imaging array;

Fig. 2 is a top plan view of the light-sensitive CCD element and its corresponding shift register CCD element of Fig. 1, on a slightly larger scale and with parts broken away to illustrate particular regions and portions of each of the elements shown beneath the surface layers, and with certain selected overlying layers also shown; and

Fig. 3 is a block diagram of a system utilizing a CCD area array composed of a plurality of lines of light-sensitive CCD elements of the type shown in Fig. 1 and a plurality of shift register lines having shift register CCD devices of the type shown in Fig. 1 in combination with input and output registers and associated elements to provide a total area array imaging system.

Referring to Fig. 1, a semiconductor substrate 10 is shown which, in the disclosed embodiment, is made of P type material. The substrate 10 is preferably a boron doped substrate containing 10^{14} impurities per cubic centimeter and has a thickness of about 150 microns. Although the described embodiment preferably uses a semiconductor substrate made of silicon material, it is evident to those skilled in the art that other semiconductor materials may be used. Futthermore, the conductivity type regions described in the embodiment of Fig. 1, can be of opposite type conductivity, if desired, in order to provide an array with CCD elements using charge packets with opposite the type of minority carriers.

Located on a surface of the substrate 10 is an N type region 12 and an N type region 14. The cross hatched regions within the regions 12 and 14 are the potential wells of each CCD element as shown in Fig. 2. The N type region 12 is part of a light-sensitive CCD element 16 that is used in the CCD area array. The N-type region 14 is part of shift register CCD element 18. Preferably, the N type regions 12 and 14 are formed during a single process step using, for example, ion implantation techniques for creating the N doped regions 12 and 14. Arsenic or phosphorus, for example, is used as the N type dopant for the regions 12 and 14. In the disclosed embodiment, the N type regions 12 and 14 have a thickness of about one-half micron and a phosphorus impurity level of 3×10^{16} atoms per cubic centimeter. The operation and function of the regions 12 and 14 are set forth in U.S. Patent 3739240.

A channel stop region 20 is shown in both Figs. 1 and 2, which region serves to prevent charge packets generated by light striking the light-sensitive regions (N region 12) of the light-sensitive element 16 from being transferred into adjacent light-sensitive elements or other undesired areas of the array. The channel stop region 20 is preferably a P+ type region which can be formed by ion implantation or by diffusion techniques. The P+ channel stop region 20 contains from about 10^{18} to about 10^{20} impurities per cubic centimeter, for example, of boron.

The P+ channel stop region 20, as can be seen by looking at Fig. 2, surrounds three sides of the light-sensitive CCD element 16 and thus blocks charge packets from passing through these three sides of the light-sensitive CCD element 16. There is only one opening that the charge packets generated in the light-sensitive CCD element 16 can be transmitted through and that is through a barrier region 22 which is the electrical gate between the light-sensitive CCD element 16 and its corresponding shift register CCD element 18. The barrier region 22 is preferably of N-type conductivity and has an impurity level for example, of 1×10^{16} impurities per cubic centimeter where the impurities are, for example, arsenic or phosphorus. The barrier region 22 is formed during a separate step in the process of fabricating the array. Preferably, ion implantation techniques are used to form the N-barrier region 22. As can be seen from Fig. 2, a barrier region 23 and a barrier region 25 are located on opposite sides of the N type region 14 of the shift register CCD element

18. The barrier regions 22, 23 and 25 are all formed in the same process step.

As a consequence, all of the N type regions 12 and 14 for the light-sensitive CCD elements 16, and the shift register CCD elements 18 for the entire array are formed during the same process step and the N-type barrier regions 22, 23 and 25 for each of the light-sensitive CCD elements 16 and the shift register CCD elements 18 of the array are also formed during a separate step in the process of fabricating the array. The P+ channel stop regions 20 are formed using a single separate process step to provide a C-shaped channel stop region for each of the light-sensitive CCD elements 16 during the fabrication of the array.

The thickness of the N– barrier regions 22, 23 and 25 is preferably about one-half micron, which is equivalent to the thickness of the N type regions 12 and 14. The channel stop regions 20 are thicker than the buried channel N type regions 12 and 14 in order to serve the function of providing a channel stop for preventing charge packets generated in the light-sensitive CCD elements by light photons striking the N region 12 from entering into adjacent light-sensitive elements or other undesired areas of the array.

In the disclosed embodiment, and with reference to Fig. 1, an insulating layer 24 is located on the active N, N– and P+ surface regions of the semiconductor substrate. Preferably, the insulating layer 24 is a thermal silicon dioxide layer having, for example, a thickness of about 1200 angstroms. This thermal oxide layer is formed using well known thermal oxidation techniques. A second insulating layer 26 is located on the first insulating layer 24 and serves the function of providing a double pin hole protection layer when used in combination with the underlying insulating layer 24 to prevent or significantly minimize the possibility of having electrically conductive material deposited on the surface of the semiconductor substrate penetrating through a pin hole in the insulating layer to electrically short out portions of the array.

Preferably, the second insulating layer 26 is made of silicon nitride and is formed by any of the well known techniques for depositing silicon nitride such as by vapor deposition, R.F. sputtering, etc. The thickness of the silicon nitride layer 26 is preferably about 300 angstroms. Another important function of the silicon nitride layer 26 is that it prevents further growth of the thermal oxide insulating layer 24 which is very sensitive to subsequent thermal process steps such as are used, for example, in the formation of the subsequent layers on the substrate surface. In this manner, the silicon nitride layer 26 serves to provide the double function of a pin hole protection layer as well as a thermal oxidation protection for the thermal oxide insulating layer 24.

A first polycrystalline silicon layer 28 doped with, for example, phosphorus impurities, is deposited on the silicon nitride layer 26. This first polycrystalline silicon layer 28 is deposited by well known techniques used in forming a polycrystalline silicon layer on an insulating surface. The doped polycrystalline silicon layer 28 is etched to form the separated, longitudinal gate electrode pattern shown in Fig. 1. Subsequently, a third insulating layer 30 is formed on the silicon nitride surface and on the exterior surface of the first polycrystalline silicon layer 28. Preferably, the third insulating layer 30 is a thermal silicon dioxide layer which is formed by well known thermal oxidation techniques.

The doped first polycrystalline silicon layer 28 is a current conducting element and thus provides the function of being a gate electrode. The electrode gate formed by the doped polycrystalline silicon layer 28 is the "frame gate" for the light-sensitive element 16 which functions to help permit the charge packets (generated in the light-sensitive element 16 by light impinging thereon) to pass laterally into the corresponding shift register element 18. The charge packets generated within the N type region 12 of the light-sensitive CCD element 16 are shifted laterally into the charge storage region 14 of the shift register CCD element 18 so that they may then be transferred up the shift register line to the output portion of the array. The doped polycrystalline electrode 28 is transparent to light so that it can function as a gate electrode and yet permit light to be transmitted through the electrode 28 and into contact with the light-sensitive portion 12 of the light-sensitive CCD element 16 to thereby generate the charge packets.

A second polycrystalline silicon layer 32 is deposited on the exposed surface portions of the silicon nitride layer 26 and on the surface portion of the thermal oxide region 30. The second polycrystalline silicon layer 32 is selectively doped with phosphorus in regions thereof to provide alternate conductive and nonconductive (insulating) regions where desired. The electrically conductive or electrode portions of the second polycrystalline silicon layer 32 provide with the gate electrodes 28 an orthogonal gate electrode array configuration. The electrode portions of the polycrystalline layer 32 are the "vertical gates" for carrying clock pulses into the array in order to lower the

potential barrier of the buried barrier region 23, for example, of the shift register element 18 to thereby pass the charge packets vertically along the shift register line. An encapsulating insulating layer 34 is provided on the second polycrystalline silicon layer 32 to protect the polycrystalline layer 32 and also to provide electrical insulation from an aluminum light blocking shield 36 which is located on the portion of the insulating layer 34 that is located over the shift register element 18. The insulating layer 34 is preferably a vapor-deposited oxide layer. The thickness of the second polycrystalline silicon layer 32 is preferably about 4000 angstroms. The thickness of the aluminum light shield is preferably about 1 micron and this material thickness serves to prevent light from passing through the aluminum light blocking shield 36.

In one example, an array containing 10,000 photo-sensitive CCD elements was formed of 100×100 light-sensitive CCD elements 16 and 100 shift register CCD columns with each column containing 100 shift register elements 18. The light sensitive CCD elements 16 were formed in a plurality of vertical shift register lines with each one of the shift register elements 18 located adjacent to and, as explained above, electrically coupled to a corresponding light-sensitive element 16 to receive, under certain conditions, charge packets generated within and transmitted from the light-sensitive elements 16. For example, transfer of charge packets from the light-sensitive CCD element 16 to the shift register CCD element 18 occurs when the "vertical gate" electrode portion of the second polycrystalline layer 32 (which is the portion that overlies the region 14) is at a higher electrical potential than the electrical potential applied to the "frame gate" electrode 28.

In more detail, a potential of +5 volts applied to the "vertical gate" electrode portion of the second polycrystalline layer 32 as compared with the holding of the potential of the "frame gate" electrode 28 at 0 volts causes the charge packets to laterally pass through the N– buried barrier region 22 from the light-sensitive CCD element 16 to the shift register CCD element 18. In one embodiment, the width of the buried barrier region 22 is about 0.2 mils wide, the width of the "vertical gate" is about 0.9 mils, the width of the P+ channel stop region 20 is about 0.2 mils, the width of the "frame gate" electrode 28 is about 0.6 mils and the separation distance between "vertical gate" electrodes is about 0.4 mils.

Referring to Fig. 3, a system is disclosed which includes an imaging array 100 which is composed of pluralities of light-sensitive CCD elements 16 and the shift register CCD elements 18. In the embodiment where n 10,000 (100×100) light-sensitive CCD elements 16 are used in combination with 100 columns of vertical shift registers (each column contains 100 CCD shift registers), 50 two-phase vertical shifts (or 100 jumps) are needed to transfer charge packets entering the lowermost shift register elements at the bottom portion of the array 100 to the uppermost shift register elements located at the upper portion of the array 100. Since the system disclosed in Fig. 3 is a two-phase CCD system, clock pulses applied to electrodes ϕv_1 and ϕv_2 which are electrically connected to alternate, adjacent "vertical gates" (electrode portions of the second polycrystalline layer 32) cause the charge packets to be transferred vertically through the shift register CCD elements 18 forming the vertical shift register CCD lines. As disclosed in Application 2710/74 (Serial Number 1,453,341), the pulsed potentials applied to the electrodes ϕv_1 and ϕv_2 causes the charge packets in the shift register CCD elements 18 to be transferred vertically through the vertical shift register CCD lines. A pulsed potential of, for example, about –8 to about +4 volts applied to the electrodes ϕv_1 and ϕv_2 causes the charge packets to be transferred vertically through the shift register CCD elements 18 provided that the pulsed voltages applied to the two electrodes ϕv_1 and ϕv_2 are out-of-phase or complementary to each other. When the potential applied to selected vertical gate electrode portions of the second polycrystalline silicon layer 32 is +4 volts (most positive portion of the potential swing) charge packets are passed through the buried barrier region 23 (or 25) located beneath the vertical gate electrode which is at the most positive potential. The +4 volts applied to the vertical gate electrode lowers the potential barrier of the associated buried barrier region 23 (or 25) located beneath the most positive vertical gate electrode.

Frame electrode ϕ_F electrically connects a clock (not shown) to the frame electrodes 28 of the array 100. The clock supplies a swinging voltage of from about 0 to about +10 volts.

In the embodiment disclosed in detail, 100 bits or charge packets are dumped into output register 102 from the array 100 at one time.

Preferably, the two-phase CCD output register 102 contains 102 gates associated with the electrode ϕH_1 and 102 gates associated with the electrode ϕH_2. ϕH_1 and ϕH_2 are similar to electrodes ϕv_1 and ϕv_2 associated with the array 100. Thus, clocks

connected to electrodes ϕH_1 and ϕH_2 apply a swinging voltage of from about −8 to about +4 volts which causes a corresponding potential to be applied to the gate electrodes associated with each electrode ϕH_1 and ϕH_2. The output register 102 and 204 shift register elements of the type shown by reference numeral 18 in Figs. 1 and 2. Thus, 102 two-phase shifts (or 204 jumps) are needed to move the bits or charge packets from one end of the output register 102 to the other (or output) end thereof.

Electrically connected to the output portion of the output register 102 is an output amplifier 104 with a source electrode S_1 and a drain electrode D_1. The output amplifier 104 is an MOS or FET type of amplifier of the type described in Application 2710/74 (Serial No. 1453341). A compensation amplifier 106 made of a MOS or FET type device with source S_2 and a drain D_2 electrodes is electrically connected to the output amplifier 104 and functions to compensate for the noise generated by reset circuit 108 to which is connected a reset drain electrode R_D. A reset clock (not shown) is connected to the reset circuit 108 by means of electrode ϕ_R which is electrically connected to the reset circuit 108. The operation of the compensation amplifier 106 and the output amplifier 104 which together function as a differential amplifier is disclosed and described in the above-mentioned Application 2710/74 (Serial No. 1453341) which also discusses the need for the reset circuit 108 to clear the apparatus for the next signal.

At the input portion of the system disclosed in Fig. 3, is an input register 110 which is similar to the output register 102. Thus, both the input and output registers use CCD shift register elements of the type shown generally by reference numeral 18 in Figs. 1 and 2. Accordingly, 102 two-phase shifts (or 204 jumps) are needed to move bits or charge packets from one end of the input register 110 to the other end thereof. However, only one shift is needed to move the charge packets vertically into the array 100. A total of 100 bits or charge packets are moved into the array 100 from the input register 110. Clocks (not shown) are electrically connected to electrodes $\phi H_1'$ and $\phi H_2'$ to move the charge packets through the shift registers forming the input register 110. An input section 112 is composed of an input source electrode which is pulsed with a voltage that swings from about −8 to about +4 volts that is connected to an N+ diffused region (not shown). An input gate located over the N+ diffused region is held to a potential of about 0 volts. The input source 112 generates electrical signals to the input register 110 and serves as an alternative method of providing an input to the array 100. Thus, the system of Fig. 3 can be used with a light source input directly striking the light-sensitive elements 16 of the array 100 or with an electrical (electron) input from the input section 112.

WHAT WE CLAIM IS:—

1. An imaging array comprising a plurality of lines of light-sensitive charge-coupled elements associated with portions of a semiconductor substrate, a plurality of shift register lines each having a plurality of charge-coupled elements associated with other portions of the semiconductor substrate, each one of the shift register charge-coupled elements being located adjacent and having a one-to-one correspondence with a particular one of the light-sensitive charge-coupled elements, and means for transferring charge packets generated in the light-sensitive charge-coupled elements to the particular corresponding charge-coupled elements of the shift register lines for subsequent movement within the shift register lines to an output portion of the array.

2. An imaging array as claimed in claim 1 having means for shifting the charge packets along the shift register lines.

3. An imaging array as claimed in claim 2 having output means for receiving charge packets at the end of each shift register line.

4. An imaging array as claimed in claim 1, 2 or 3 in which the means for transferring charge packets generated in the light-sensitive elements to the particular corresponding charge-coupled elements of the shift register lines comprises a pair of light-transparent gate electrode means associated with each of the light-sensitive charge-coupled elements.

5. An imaging array as claimed in claim 4 in which at least one of the pair of light-transparent gate electrode means comprises a conductive polycrystalline silicon electrode.

6. An imaging array as claimed in any preceding claim in which each of the shift register elements is covered with an opaque material.

7. An imaging array as claimed in claim 6 in which the opaque materials is aluminium.

8. An imaging array as claimed in any preceding claim in which the the charge-coupled elements in the shift register lines are separated by barrier regions.

9. An imaging array as claimed in any preceding claim in which each of the light-sensitive elements is separated from adjacent light-sensitive elements by heavily doped channel stop regions formed in the

connected to electrodes ϕH_1 and ϕH_2 apply a swinging voltage of from about −8 to about +4 volts which causes a corresponding potential to be applied to the gate electrodes associated with each electrode ϕH_1 and ϕH_2. The output register 102 and 204 shift register elements of the type shown by reference numeral 18 in Figs. 1 and 2. Thus, 102 two-phase shifts (or 204 jumps) are needed to move the bits or charge packets from one end of the output register 102 to the other (or output) end thereof.

Electrically connected to the output portion of the output register 102 is an output amplifier 104 with a source electrode S_1 and a drain electrode D_1. The output amplifier 104 is an MOS or FET type of amplifier of the type described in Application 2710/74 (Serial No. 1453341). A compensation amplifier 106 made of a MOS or FET type device with source S_2 and a drain D_2 electrodes is electrically connected to the output amplifier 104 and functions to compensate for the noise generated by reset circuit 108 to which is connected a reset drain electrode R_D. A reset clock (not shown) is connected to the reset circuit 108 by means of electrode ϕ_R which is electrically connected to the reset circuit 108. The operation of the compensation amplifier 106 and the output amplifier 104 which together function as a differential amplifier is disclosed and described in the above-mentioned Application 2710/74 (Serial No. 1453341) which also discusses the need for the reset circuit 108 to clear the apparatus for the next signal.

At the input portion of the system disclosed in Fig. 3, is an input register 110 which is similar to the output register 102. Thus, both the input and output registers use CCD shift register elements of the type shown generally by reference numeral 18 in Figs. 1 and 2. Accordingly, 102 two-phase shifts (or 204 jumps) are needed to move bits or charge packets from one end of the input register 110 to the other end thereof. However, only one shift is needed to move the charge packets vertically into the array 100. A total of 100 bits or charge packets are moved into the array 100 from the input register 110. Clocks (not shown) are electrically connected to electrodes $\phi H_1'$ and $\phi H_2'$ to move the charge packets through the shift registers forming the input register 110. An input section 112 is composed of an input source electrode which is pulsed with a voltage that swings from about −8 to about +4 volts that is connected to an N+ diffused region (not shown). An input gate located over the N+ diffused region is held to a potential of about 0 volts. The input source 112 generates electrical signals to the input register 110 and serves as an alternative method of providing an input to the array 100. Thus, the system of Fig. 3 can be used with a light source input directly striking the light-sensitive elements 16 of the array 100 or with an electrical (electron) input from the input section 112.

WHAT WE CLAIM IS:—

1. An imaging array comprising a plurality of lines of light-sensitive charge-coupled elements associated with portions of a semiconductor substrate, a plurality of shift register lines each having a plurality of charge-coupled elements associated with other portions of the semiconductor substrate, each one of the shift register charge-coupled elements being located adjacent and having a one-to-one correspondence with a particular one of the light-sensitive charge-coupled elements, and means for transferring charge packets generated in the light-sensitive charge-coupled elements to the particular corresponding charge-coupled elements of the shift register lines for subsequent movement within the shift register lines to an output portion of the array.

2. An imaging array as claimed in claim 1 having means for shifting the charge packets along the shift register lines.

3. An imaging array as claimed in claim 2 having output means for receiving charge packets at the end of each shift register line.

4. An imaging array as claimed in claim 1, 2 or 3 in which the means for transferring charge packets generated in the light-sensitive elements to the particular corresponding charge-coupled elements of the shift register lines comprises a pair of light-transparent gate electrode means associated with each of the light-sensitive charge-coupled elements.

5. An imaging array as claimed in claim 4 in which at least one of the pair of light-transparent gate electrode means comprises a conductive polycrystalline silicon electrode.

6. An imaging array as claimed in any preceding claim in which each of the shift register elements is covered with an opaque material.

7. An imaging array as claimed in claim 6 in which the opaque materials is aluminium.

8. An imaging array as claimed in any preceding claim in which the the charge-coupled elements in the shift register lines are separated by barrier regions.

9. An imaging array as claimed in any preceding claim in which each of the light-sensitive elements is separated from adjacent light-sensitive elements by heavily doped channel stop regions formed in the

top surface of the semiconductor substrate, the heavily doped channel stop regions surrounding each of the light-sensitive elements on three sides so that every light-sensitive element is exposed on the one open side thereof to the particular corresponding element of the shift register lines.

10. An imaging array as claimed in claim 9 in which each of the light-sensitive elements comprises a region of one conductivity type formed in a region of opposite conductivity type with a higher resistivity barrier region formed on the one conductivity type located adjacent the region on the one open side.

11. An imaging array as claimed in claim 10 in which the one conductivity type is n, the opposite conductivity type is p, and the heavily doped channel stop regions are of p-type conductivity.

12. An imaging array as claimed in claim 10 or 11 in combination with means for lowering the potential of the barrier regions on the open sides of the light-sensitive elements to permit charge packets generated in the light-sensitive elements to pass into the particular corresponding charge-coupled elements in the shift register lines.

13. An imaging array substantially as herein described with reference to Figs. 1 and 2 of the accompanying drawing.

14. An imaging system substantially as herein described with reference to Fig. 3 of the accompanying drawing.

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