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A METHOD TO IMPROVE THE COUPLING RATIO OF TOP GATE TO FLOATING GATE IN FLASH

ABSTRACT

A structure is disclosed to improve the coupling ratio of top gate to floating gate in flash memory cells. Parallel active regions are surrounded by isolation regions and are disposed over a semiconductor region of a substrate. The isolation regions have a portion within and a portion above the semiconductor region. The semiconductor region under the active regions is doped in the vicinity of the surface to adjust the threshold voltage. Insulator spacers are disposed against the sidewalls of the portion of the isolation regions that are above the semiconductor region and they taper so they are wider near the semiconductor region, and thus the spacing between neighboring insulator spacers on the same active region decreases closer to the semiconductor region. Conductive floating gates spaced along the active regions are separated from the semiconductor region by a floating gate insulator layer, are disposed between insulator spacers and extend about to the height of the isolation regions. Top gates, comprised of conductive stripes that are perpendicular to the active regions, are disposed over floating gates from which they are separated by a top gate insulator layer.

(Fig. 2a)

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