CLAIMS

1. An apparatus, comprising:

an integrated circuit, comprising:

logic analyzer circuitry having a first input receiving a plurality of signals, and a first output for providing selected samples of the signals appearing at the first input; and

a first block having a first input coupled to the logic analyzer circuitry for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer circuitry for directly providing a distinct set of one or more signals thereto that are based upon the one or more signals at the first input of the first block according to a predetermined function, the predetermined function being configurable.

2. The apparatus of claim 1, wherein the logic analyzer circuitry includes a second output for providing an indication of a detection, by the logic analyzer circuitry, of at least one trigger event, wherein the first block includes a second input coupled to the second output of the logic analyzer circuitry, and wherein the output of the first block is selectively based upon the signals received at the first and second inputs thereof.

3. The apparatus of claim 2, wherein the first block is configurable as an accumulator, the accumulator being enabled by the second output of the logic analyzer circuitry.

4. The apparatus of claim 2, wherein the first block is configurable to perform a function that is enabled by the second output of the logic analyzer circuitry.

5. The apparatus of claim 1, wherein the logic analyzer circuitry comprises a multiplexer block coupled to the first input of the logic analyzer circuitry, and a trigger event block coupled to an output of the input multiplexer block for detecting at least one trigger event,

wherein the distinct set of one or more signals is provided to an input of the trigger event block.

6. The apparatus of claim 1, wherein the logic analyzer circuitry comprises an output control block for selectively sampling signals appearing at the first input of the logic analyzer circuitry and at the output of the first block.

7. The apparatus of claim 1, wherein the first block comprises field programmable circuitry.

8. The apparatus of claim 1, wherein the logic analyzer circuitry comprises an input multiplexer block having a first input coupled to the first input of the logic analyzer circuitry and a second input coupled to the first output of the first block.

9. The apparatus of claim 1, wherein the distinct set of one or more signals provided to the logic analyzer circuitry by the first block is available for at least one of selectively sampling and selectively detecting a trigger event by the logic analyzer circuitry.

10. An integrated circuit, comprising:

logic analyzer circuitry having a first input receiving a plurality of signals, and a first output for providing selected samples of the signals appearing at the first input; and

a first block having a first input coupled to the logic analyzer circuitry for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer circuitry for directly providing a distinct set of one or more signals thereto that are based upon the one or more signals at the first input of the first block according to a predetermined function, the predetermined function being configurable.

11. The integrated circuit of claim 1, wherein the logic analyzer circuitry includes a second output for providing an indication of a detection, by the logic analyzer circuitry, of at least one trigger event, wherein the first block includes a second input coupled to the second output of the logic analyzer circuitry, and wherein the output of the first block is selectively based upon the signals received at the first and second inputs thereof.

12. The integrated circuit of claim 11, wherein the first block is configurable to perform a function that is enabled by the second output of the logic analyzer circuitry.

13. The integrated circuit of claim 10, wherein the first block comprises field programmable circuitry.

14. The integrated circuit of claim 10, further comprising an interface for configuring the predetermined function of the first block.

15. The integrated circuit of claim 10, wherein the logic analyzer circuitry comprises a multiplexer block coupled to the first input of the logic analyzer circuitry, and a trigger event block coupled to an output of the input multiplexer block for detecting at least one trigger

event, wherein the distinct set of one or more signals is provided to an input of the trigger event block.

16. The integrated circuit of claim 10, wherein the logic analyzer circuitry comprises an output control block for selectively sampling signals appearing at the first input of the logic analyzer circuitry and at the output of the first block.

17. The integrated circuit of claim 10, wherein the distinct set of one or more signals provided to the logic analyzer circuitry by the first block is available for at least one of selectively sampling and selectively detecting a trigger event by the logic analyzer.

18. A system, comprising:

an integrated circuit, comprising:

an embedded logic analyzer block having an input for receiving a plurality of signals and a trigger event block for detecting an occurrence of an event based in part upon the plurality of signals;

a block coupled to the embedded logic analyzer block and having an output that is based upon the detection of the occurrence of the event, the output being provided to the embedded logic analyzer block for sampling or storage therein.

19. The system of claim 18, wherein the block is configurable to perform a function that is enabled based in part upon the detection of the occurrence of the event.

20. The system of claim 18, wherein the output is based in part upon at least one of the plurality of signals appearing at the input of the embedded logic analyzer block.

CLAIMS

1. An apparatus, comprising:

an integrated circuit, comprising:

logic analyzer circuitry having a first input receiving a plurality of signals, and a first output for providing selected samples of the signals appearing at the first input; and

a first block having a first input coupled to the logic analyzer circuitry for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer circuitry for directly providing a distinct set of one or more signals thereto that are based upon the one or more signals at the first input of the first block according to a predetermined function, the predetermined function being configurable.

2. The apparatus of claim 1, wherein the logic analyzer circuitry includes a second output for providing an indication of a detection, by the logic analyzer circuitry, of at least one trigger event, wherein the first block includes a second input coupled to the second output of the logic analyzer circuitry, and wherein the output of the first block is selectively based upon the signals received at the first and second inputs thereof.

3. The apparatus of claim 2, wherein the first block is configurable as an accumulator, the accumulator being enabled by the second output of the logic analyzer circuitry.

4. The apparatus of claim 2, wherein the first block is configurable to perform a function that is enabled by the second output of the logic analyzer circuitry.

5. The apparatus of claim 1, wherein the logic analyzer circuitry comprises a multiplexer block coupled to the first input of the logic analyzer circuitry, and a trigger event block coupled to an output of the input multiplexer block for detecting at least one trigger event,

wherein the distinct set of one or more signals is provided to an input of the trigger event block.

6. The apparatus of claim 1, wherein the logic analyzer circuitry comprises an output control block for selectively sampling signals appearing at the first input of the logic analyzer circuitry and at the output of the first block.

7. The apparatus of claim 1, wherein the first block comprises field programmable circuitry.

8. The apparatus of claim 1, wherein the logic analyzer circuitry comprises an input multiplexer block having a first input coupled to the first input of the logic analyzer circuitry and a second input coupled to the first output of the first block.

9. The apparatus of claim 1, wherein the distinct set of one or more signals provided to the logic analyzer circuitry by the first block is available for at least one of selectively sampling and selectively detecting a trigger event by the logic analyzer circuitry.

10. An integrated circuit, comprising:

logic analyzer circuitry having a first input receiving a plurality of signals, and a first output for providing selected samples of the signals appearing at the first input; and

a first block having a first input coupled to the logic analyzer circuitry for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer circuitry for directly providing a distinct set of one or more signals thereto that are based upon the one or more signals at the first input of the first block according to a predetermined function, the predetermined function being configurable.

11. The integrated circuit of claim 10, wherein the logic analyzer circuitry includes a second output for providing an indication of a detection, by the logic analyzer circuitry, of at least one trigger event, wherein the first block includes a second input coupled to the second output of the logic analyzer circuitry, and wherein the output of the first block is selectively based upon the signals received at the first and second inputs thereof.

12. The integrated circuit of claim 11, wherein the first block is configurable to perform a function that is enabled by the second output of the logic analyzer circuitry.

13. The integrated circuit of claim 10, wherein the first block comprises field programmable circuitry.

14. The integrated circuit of claim 10, further comprising an interface for configuring the predetermined function of the first block.

15. The integrated circuit of claim 10, wherein the logic analyzer circuitry comprises a multiplexer block coupled to the first input of the logic analyzer circuitry, and a trigger event block coupled to an output of the input multiplexer block for detecting at least one trigger

event, wherein the distinct set of one or more signals is provided to an input of the trigger event block.

16. The integrated circuit of claim 10, wherein the logic analyzer circuitry comprises an output control block for selectively sampling signals appearing at the first input of the logic analyzer circuitry and at the output of the first block.

17. The integrated circuit of claim 10, wherein the distinct set of one or more signals provided to the logic analyzer circuitry by the first block is available for at least one of selectively sampling and selectively detecting a trigger event by the logic analyzer.

18. A system, comprising:

an integrated circuit, comprising:

an embedded logic analyzer block having an input for receiving a plurality of signals and a trigger event block for detecting an occurrence of an event based in part upon the plurality of signals;

a block coupled to the embedded logic analyzer block and having an output that is based upon the detection of the occurrence of the event, the output being provided to the embedded logic analyzer block for sampling or storage therein.

19. The system of claim 18, wherein the block is configurable to perform a function that is enabled based in part upon the detection of the occurrence of the event.

20. The system of claim 18, wherein the output is based in part upon at least one of the plurality of signals appearing at the input of the embedded logic analyzer block.