12 Jul 02
20020425 47

162162

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 01/69679 A1

(51) International Patent Classification[7]: H01L 23/522, 21/60

(21) International Application Number: PCT/NO01/00113

(22) International Filing Date: 15 March 2001 (15.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20001360 15 March 2000 (15.03.2000) NO

(71) Applicant *(for all designated States except US)*: **THIN FILM ELECTRONICS ASA** [NO/NO]; P.O. Box 1872 Vika, N-0124 Oslo (NO).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **NORDAL, Per-Erik** [NO/NO]; Båstadryggen 19, N-1387 Asker (NO). **GUDESEN, Hans, Gude** [NO/BE]; Rue Fulton 17, B-1000 Brussels (BE). **LEISTAD, Geirr, I.** [NO/NO]; Jongsstubben 19, N-1337 Sandvika (NO). **GUSTAFSSON, Göran** [SE/SE]; Trumslagaregatan 33, S-582 16 Linköping (SE).

(74) Common Representative: **LEISTAD, Geirr, I.**; Thin Film Electronics ASA, P.O. Box 1872 Vika, N-0124 Oslo (NO).

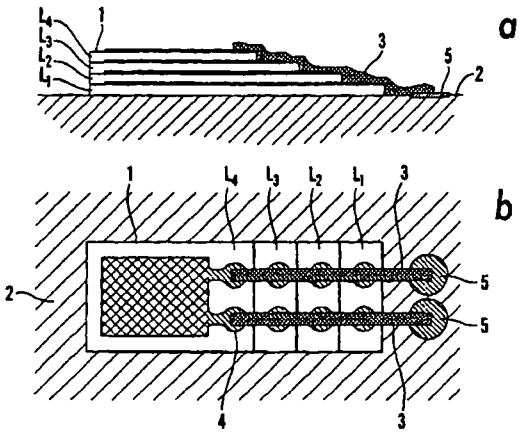
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK



(57) Abstract: In a memory and/or data processing device having at least two stacked layers which are supported by a substrate or forming a sandwich self-supporting structure, wherein the layers comprise memory and/or processing circuitry with mutual connections between the layers and/or to circuitry in the substrate, the layers are mutually arranged such that contiguous layers form a staggered structure on at least one edge of the device and at least one electrical edge conductor is provided passing over the edge on one layer and down one step at a time, enabling the connection to an electrical conductor in any of the following layers in the stack. A method for manufacturing a device of this kind comprises steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

WO 01/69679 A1

ACTION