

PATENT SPECIFICATION

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(54) TELEVISION LINE DEFLECTION CIRCUIT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED of Abacus House, 33 Gutter Lane, London EC2V 8AH a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a circuit arrangement for producing a sawtooth current having a trace and a retrace period through a line deflection coil for television display apparatus, which deflection coil is part of a resonant circuit which also comprises a trace capacitor and a retrace capacitor to the deflection coil at line frequency during the trace period of the sawtooth current, which switching arrangement comprises a first diode and a controlled switch connected in parallel with the said diode via a second diode, said sawtooth current in operation flowing through the first diode during one part of the trace period and through the second diode and the controlled switch during the other part of the trace period, the series arrangement of a winding of a first inductive element and a capacitor being connected in parallel with said first diode, the junction of said second diode and said controlled switch being connected through a winding of a second inductive element to a supply terminal for receiving a d.c. supply whereby current when supplied to said controlled switch through the winding of said second inductive element causes energy to be stored therein, and switching means for blocking any current in the second diode during the retrace period.

Such a circuit arrangement is known from published Dutch Patent Application 7303252. By adjusting the conduction time of the controlled switch the trace voltage and consequently also the amplitude of the deflection current can be brought to a given value as a function of the supply voltage. Auxiliary supply voltages which are produced by the circuit are each adjusted to a given value, but not independent from one another. For this purpose the transformation ratio of two windings of the second inductive element is also available as a parameter. For certain values thereof the switching means appears to be essential as otherwise the retrace pulses would be cut off by the conducting second diode which would result in a distortion of the deflection current. The switching means consists, for example, of a fourth diode which is placed in series with one winding of the second inductive element.

It appears, however, that the desired trace voltage cannot be obtained for every value of the supply voltage, especially if the supply voltage is lower than the desired value of the trace voltage. This is the case with television receivers which are fed by a battery. It is obvious that a higher supply voltage from the battery voltage can be obtained by means of a converter which raises the voltage, enabling the supply voltage thus obtained to supply energy to the deflection circuit. The advantages of the known circuit, namely the fact that only one controlled switch is required and the self-stabilising operation thereof for the deflection current produced and for the auxiliary supply voltages produced are, however, lost.

It is an object of the invention to provide a circuit arrangement which may combine the advantages of a converter which supplies a high voltage i.e. an up converter, with those of the known circuit.

The invention provides a circuit arrangement of the type described in the opening paragraph and further comprising a third diode an electrode of which is connected to a point of the first inductive element, the other electrode thereof being connected to said supply terminal through a portion of the second inductive element, the winding sense of said portion and the direction of conduction of the third diode having being such that in operation current can flow

therethrough during the retrace period of the deflection current for restoring energy loss in said resonant circuit. In this respect it should be noted that the switching means, for example, a fourth diode, of the known circuit arrangement is only necessary with a given design thereof whilst in the circuit according to the invention it is necessary in all circumstances.

The invention will be further explained by way of non-limitative example with reference to the accompanying drawings, in which :-

Figure 1 shows an embodiment of the circuit arrangement according to the invention, Figure 2 shows waveforms occurring therein;

Figure 3 shows a variation of the circuit arrangement of Figure 1, and

Figure 4 shows an embodiment of the circuit arrangement according to the invention suitable for a colour television receiver.

Figure 1 only shows the most important components of the line-deflection circuit of a television receiver not further shown. A deflection coil L_y , a trace capacitor C_t and a retrace capacitor C_r constitute a resonant network with which a diode D_1 is in parallel. Parallel to diode D_1 is the series arrangement of a diode D_2 and an npn transistor Tr , wherein the directions of conduction of the two diodes have been chosen such that diode D_1 conducts in the first half and diode D_2 in the second half of the trace period of the deflection current. The series arrangement of a winding L_1 and a capacitor C_1 is included between the junction point A of components D_1 , D_2 , C_r and L_y and earth. The other ends of components D_1 , C_r and C_t as well as the emitter of transistor Tr are connected to this same earth. Through a choke coil L_2 and a diode D_3 the collector of transistor Tr is connected to the positive terminal of a power supply source which supplies a d.c. voltage V_B , the negative terminal of this voltage supply source being connected to earth. The anode of a diode D_3 is connected to a tap P of coil L_2 , the cathode of diode D_3 being connected to a tap Q of winding L_1 .

During the first half of the trace period diode D_1 conducts. The voltage across capacitor C_t is applied to coil L_y through which coil deflection current i_y flows in the direction opposite to that of the arrow shown in Figure 1. At the beginning of the trace period the transistor Tr is in the non-conducting state. There is a positive voltage at its collector and consequently diode D_2 is also non-conducting. At a given instant transistor Tr is made conductive by means of a pulse-shaped drive signal which is derived from a line oscillator, not shown. The collector current of transistor Tr flows through coil L_2 and diode D_3 whilst D_2 remains blocked as the anode voltage thereof, being the cathode voltage of diode D_1 is slightly more negative than the cathode voltage.

Approximately in the middle of the trace period current i_y reverses its direction so that it now flows through diode D_2 and transistor Tr , whilst diode D_1 is rendered non-conducting. At the end of the trace period transistor Tr is cut off by means of the drive signal supplied to its base. An oscillation, the retrace pulse, is produced at point A, whilst the energy stored in coil L_2 and which is derived from the source produces a current through diode D_3 which current compensates for the losses occurring in the circuit. At the end of the retrace period the voltage in point A becomes negative again, which renders D_1 conductive. This is the beginning of a new cycle. Diode D_3 remains conductive until transistor Tr is made conductive whereafter the current through diode D_3 is taken over by the collector current of transistor Tr . Current continues to flow through coil L_2 during the entire cycle so that the ripple current through the voltage source is low and produces few interferences.

In Figure 2a the voltage v_A at point A, in Figure 2b that at point P, in Figure 2c the collector voltage of transistor Tr and in Figure 2d the collector current of this transistor is plotted versus time t . T indicates the line period, i.e., approximately $64\mu s$, whilst δT indicates the part of period T in which transistor Tr is conducting. From the above it appears that the shortest possible duration of δT is approximately equal to half the trace period and that the longest possible duration thereof is approximately equal to the entire trace period. If, for example, the duration of the retrace period is 20% of the period then the value of ratio δ is between 0.4 and 0.8.

A d.c. voltage V_0 is present across capacitor C_1 . The d.c. voltage across capacitor C_t , or the d.c. voltage component of the trace voltage across it if the capacitor has a comparatively small capacitance for S-correction, is equal to voltage V_0 . Also the average value of voltage μA is equal to V_0 . If the value of voltage V_B is known then a desired value can be given for voltage V_0 , as a consequence of which also the amplitude of a current i_y is given. For voltage V_0 three parameters are important, namely ratio δ , ratio $1:n$ of the total number of turns of coil L_2 to the number of turns drawn above point P and the ratio $1:m$ of the total number of turns of winding L_1 to the number of turns drawn above point Q.

The voltage at point Q is equal to $(1-m)V_0 + mV_A$. The voltage at point P (see Figure 2b) is equal to this voltage in the time $(1-\delta)T$ in which diode D_3 conducts and is equal to $(1-n)V_B$ in the time δT in which transistor Tr conducts. In the same time δT the collector voltage of transistor Tr (see Figure 2c) is substantially zero. In time $(1-\delta)T$ diodes D_2 and D_3 do not conduct. In that time the voltage at the interconnected cathodes thereof, consequently at the collector of transistor Tr , assumes a value which is equal to the highest anode voltage: this is

voltage V_A during the retrace period. In the time interval after the retrace period and before transistor Tr becomes conductive this is the anode voltage of diode D_4 : because the voltage at point P is in this interval equal to $(1-m)V_0 - a \mu_A$ is then zero, the collector voltage being equal to $(1-m)V_0 - (1-n)V_B$.

The voltage across coil L_1 can be computed on the basis of these results. As the average value over one cycle of this voltage must be zero this results in a relation between voltage V_0 and V_B as a function of the three parameters considered. This relation is:

$$V_0 = \frac{1 - (1-n)\delta}{1 - (1-m)\delta} V_B$$

(1)

A certain value can be given to voltage V_0 by the choice of parameters m , n and δ . By means of feed-back and a pulse duration modulation of the pulses which drive the base of transistor Tr ratio δ can be adjusted in known manner in such a way that the value of voltage V_0 is independent of variations of voltage V_B . In the simple case that $n=1$ and $m=0$, in which the anode of diode D_3 is connected to the node of coil L_2 and diode D_4 and the cathode of diode D_3 to the node of winding L_1 and capacitor C_1 V_0 may expressed as follows:-

$$V_0' = \frac{V_B}{1-\delta}$$

With $\delta = 0.8$, $V_0 = 5 V_B$.

From the above-mentioned general formula (1) it appears that V_0 and V_B are equal to one another if $m = n$ which means that V_0 cannot be adjusted or controlled by means of δ . This occurs, for example, if $m = n = 1$, which is the case when diode D_3 is applied between point A and the node of coil L_2 and diode D_4 . It is, consequently, clear that the circuit must satisfy yet another condition. This condition may be found by assuming the collector voltage of transistor Tr to be positive in the time interval after the retrace period and before the transistor becomes conducting. If this voltage is zero then a time variation of the base control has no influence and this voltage must not become negative as otherwise the collector-base diode of the transistor would become conductive. This leads to the condition that $(1-m)V_0$ must exceed $(1-n)V_B$. In this respect it may be mentioned that this condition is identical to the condition that diode D_3 must not conduct in time δT .

If in the latter mentioned condition the value of $\frac{V_0}{V_B}$ of formula (1) is filled in then it is found that n must exceed m . From this it follows that V_0 always exceeds V_B . For this reason the circuit is suitable for use with a television receiver in which the supply voltage is low, for example a receiver fed by a battery. The ratio of V_0 to V_B is larger as n is larger than m and it can be proved that a variation range of voltage V_B can be compensated for by a smaller variation range of ratio δ also as n is larger than m .

For these reasons it may be advantageous to choose n as large as possible, even larger than 1, and to choose m as low as possible, even to produce a negative-voltage across it. In this manner the circuit shown in Figure 3 is obtained. Herein not the anode of diode D_3 but tht of diode D_4 is connected to a tap of coil L_2 whilst not the cathode of diode D_3 but capacitor C_1 is connected to a tap of winding L_1 . A restriction is, however, that both the denominator and the numerator in formula (1) must be positive which means that m must exceed $1 - \frac{1}{\delta_{\max}}$, where $\delta_{\max}$ is the maximum value of δ . For example, if $\delta_{\max} = 0.8$ then m must exceed -0.25 . As n exceeds m the above condition that the denominator and the numerator must be positive is then satisfied.

With a negative value for m the value $n = 0$ is theoretically possible: In Figure 1 the anode of diode D_3 is then connected to the voltage source. It is, however, obvious that such a circuit does not work in practice because the current flowing through coil L_2 cannot find a path during time δT at the instant that transistor Tr is switched-off. It will also be appreciated that the mathematically theoretically possible condition that both the denominator and the numerator in formula (1) would then need to be negative results in a circuit which cannot be realised in practice.

In connection with the consideration mentioned above it should be noted that diode D_4 is necessary in all circumstances, this in contradistinction to the diode in a similar place as described in the above-mentioned Dutch Patent Application, which diode is not required in all the circuits described in that Application. For the average value of the voltage at point P in Figure 1 being V_B , the average value of the voltage in point A is equal to V_0 . If diode D_4 were removed from the circuits of the present application then diodes D_2 and D_3 would be in parallel with one another with opposite directions of conductivity with the voltage $V_0 - V_B$ effectively applied across them, which is not possible.

In practice both winding portions above and below the taps of coils L_1 or L_2 may each be constructed as two separate, interconnected windings. In the case of coil L_2 a first winding is thus obtained between the positive terminal of the voltage source and diode D_4 whilst a second winding could be between the same terminal and diode D_3 . Said first winding and

diode D_4 may be interchanged, although the situation in which the winding is connected direct to a point of fixed potential is preferred. The same applies to the possible interchanging of second winding of coil L_2 and diode D_3 .

In Figures 1 and 3 winding L_1 is constructed as a primary winding of a transformer T whose two secondary windings L_3 and L_4 are shown in the drawing. Retrace pulses are produced across these secondary windings which, after rectification, supply d.c. voltages for feeding other parts of the receiver. One of these voltages may be the high voltage for the final anode of the picture display tube. If voltage V_0 is stabilised then these voltages are stabilised too. The modulator (not shown in the drawing) in which the pulse duration modulation is effected in known manner is supplied with information about the value of voltage V_0 , for example by means of a further secondary winding L_5 of transformer T (see Figure 1).

Figure 4 shows a further embodiment of a circuit arrangement according to the invention which is suitable for a colour television receiver. Herein the network D_1 , C , L_1 , C' and a second, similar network D_1' , C' , L_1' , C' are arranged in a manner which is further described in our Patent Application 941/74 (Serial No. 1459 922). A parabolic signal of field frequency is supplied through a coil L_0 whereby the line deflection current is submitted to the so-called east-west modulation. In this circuit $m = 0$ and $n = 1$ which offers the advantage that no leakage inductances are present so that currents may vary in a transient manner without causing disturbances. Winding L_5 is fed back to the driver stage Dr which stage provides the modulated drive for the base of transistor Tr. In known manner coil J_2 may be a winding of transformer T. The linearity is improved because the anode of diode D_2 is connected to a tap of winding L_1 . It is obvious that D_4 may be replaced by a transistor as it may also be in Figures 1 and 3. In a practical embodiment of this Figure 4 circuit voltage V_0 is approximately 36 V for a nominal value of the battery voltage V_B of 12 V, so that the nominal value of ratio δ is approximately 0.67. The self induction value of coil L_5 is approximately $430 \mu H$.

WHAT WE CLAIM IS:-

1. A circuit arrangement for producing a sawtooth current having a trace and a retrace period through a line deflection coil for television display apparatus, which deflection coil is part of a resonant circuit which also comprises a trace capacitor and a retrace capacitor, a switching arrangement for applying in operation the voltage present across the trace capacitor to the deflection coil at line frequency during the trace period of the sawtooth current, which switching arrangement comprises a first diode and a controlled switch connected in parallel with the said diode via a second diode, said sawtooth current in operation flowing through the first diode during one part of the trace period and through the second diode and the controlled switch during the other part of the trace period, the series arrangement of a winding of a first inductive element and a capacitor being connected in parallel with said first diode, the junction of said second diode and said controlled switch being connected through a winding of a second inductive element to a supply terminal for receiving a d.c. supply whereby current when supplied to said controlled switch through the winding of said second inductive element causes energy to be stored therein, switching means for blocking any current in the second diode during the retrace period, a third diode an electrode of which is connected to a point of the first inductive element, the other electrode thereof being connected to said supply terminal through a portion of the second inductive element, the winding sense of said portion and the direction of conduction of the third diode being such that in operation, current can flow therethrough during the retrace period of the deflection current for restoring energy loss in said resonant circuit.
2. A circuit arrangement as claimed in Claim 1, in which the ratio m of the number of turns of the winding of the first inductive element between the capacitor and the third diode to the number of turns between the capacitor and the first diode is less than the ratio n of the number of turns of the portion of the second inductive element between the supply terminal and the third diode to the number of turns between said supply terminal and the controlled switch.
3. A circuit arrangement as claimed in Claim 1, in which the ratio n of the number of turns of the portion of the second inductive element between the supply terminal and the third diode to the number of turns between said supply terminal and the controlled switch equals one.
4. A circuit arrangement as claimed in Claim 1, in which the ratio m of the number of turns of the winding of the first inductive element between the capacitor and the third diode to the number of turns between the capacitor and the third diode to the number of turns between the capacitor and the first diode exceeds $1 - \frac{1}{\delta_{\max}}$, wherein $\delta_{\max}$ is, in operation, the maximum possible value of the ratio δ of the time interval during which the controlled switch conducts to the entire line period.
5. A circuit arrangement as claimed in Claim 2, in which $m = 0$ and $n = 1$.
6. A circuit arrangement as claimed in any of the preceding Claims, in which the first and the second inductive element have one common core.



diode D_4 may be interchanged, although the situation in which the winding is connected direct to a point of fixed potential is preferred. The same applies to the possible interchanging of second winding of coil L_2 and diode D_3 .

In Figures 1 and 3 winding L_1 is constructed as a primary winding of a transformer T whose two secondary windings L_3 and L_4 are shown in the drawing. Retrace pulses are produced across these secondary windings which, after rectification, supply d.c. voltages for feeding other parts of the receiver. One of these voltages may be the high voltage for the final anode of the picture display tube. If voltage V_0 is stabilised then these voltages are stabilised too. The modulator (not shown in the drawing) in which the pulse duration modulation is effected in known manner is supplied with information about the value of voltage V_0 , for example by means of a further secondary winding L_5 of transformer T (see Figure 1).

Figure 4 shows a further embodiment of a circuit arrangement according to the invention which is suitable for a colour television receiver. Herein the network D_1, C, L, C and a second, similar network D_1', C', L', C' are arranged in a manner which is further described in our Patent Application 941/74 (Serial No. 1459 922). A parabolic signal of field frequency is supplied through a coil L_6 whereby the line deflection current is submitted to the so-called east-west modulation. In this circuit $m = 0$ and $n = 1$ which offers the advantage that no leakage inductances are present so that currents may vary in a transient manner without causing disturbances. Winding L_5 is fed back to the driver stage Dr which stage provides the modulated drive for the base of transistor Tr. In known manner coil L_2 may be a winding of transformer T. The linearity is improved because the anode of diode D_2 is connected to a tap of winding L_1 . It is obvious that D_4 may be replaced by a transistor as it may also be in Figures 1 and 3. In a practical embodiment of this Figure 4 circuit voltage V_0 is approximately 36 V for a nominal value of the battery voltage V_B of 12 V, so that the nominal value of ratio δ is approximately 0.67. The self induction value of coil L_7 is approximately $430 \mu H$.

WHAT WE CLAIM IS:-

1. A circuit arrangement for producing a sawtooth current having a trace and a retrace period through a line deflection coil for television display apparatus, which deflection coil is part of a resonant circuit which also comprises a trace capacitor and a retrace capacitor, a switching arrangement for applying in operation the voltage present across the trace capacitor to the deflection coil at line frequency during the trace period of the sawtooth current, which switching arrangement comprises a first diode and a controlled switch connected in parallel with the said diode via a second diode, said sawtooth current in operation flowing through the first diode during one part of the trace period and through the second diode and the controlled switch during the other part of the trace period, the series arrangement of a winding of a first inductive element and a capacitor being connected in parallel with said first diode, the junction of said second diode and said controlled switch being connected through a winding of a second inductive element to a supply terminal for receiving a d.c. supply whereby current when supplied to said controlled switch through the winding of said second inductive element causes energy to be stored therein, switching means for blocking any current in the second diode during the retrace period, a third diode an electrode of which is connected to a point of the first inductive element, the other electrode thereof being connected to said supply terminal through a portion of the second inductive element, the winding sense of said portion and the direction of conduction of the third diode being such that in operation, current can flow therethrough during the retrace period of the deflection current for restoring energy loss in said resonant circuit.

2. A circuit arrangement as claimed in Claim 1, in which the ratio m of the number of turns of the winding of the first inductive element between the capacitor and the third diode to the number of turns between the capacitor and the first diode is less than the ratio n of the number of turns of the portion of the second inductive element between the supply terminal and the third diode to the number of turns between said supply terminal and the controlled switch.

3. A circuit arrangement as claimed in Claim 1, in which the ratio n of the number of turns of the portion of the second inductive element between the supply terminal and the third diode to the number of turns between said supply terminal and the controlled switch equals one.

4. A circuit arrangement as claimed in Claim 1, in which the ratio m of the number of turns of the winding of the first inductive element between the capacitor and the third diode to the number of turns between the capacitor and the third diode to the number of turns between the capacitor and the first diode exceeds $1 - \frac{1}{\delta_{\max}}$, wherein $\delta_{\max}$ is, in operation, the maximum possible value of the ratio δ of the time interval during which the controlled switch conducts to the entire line period.

5. A circuit arrangement as claimed in Claim 2, in which $m = 0$ and $n = 1$.

6. A circuit arrangement as claimed in any of the preceding Claims, in which the first and the second inductive element have one common core.

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7. A circuit arrangement for producing a sawtooth deflection current through a line deflection coil for television display apparatus substantially as herein described with reference to the accompanying drawings.

8. A television display apparatus comprising a circuit arrangement as claimed in any of the preceding Claims.

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