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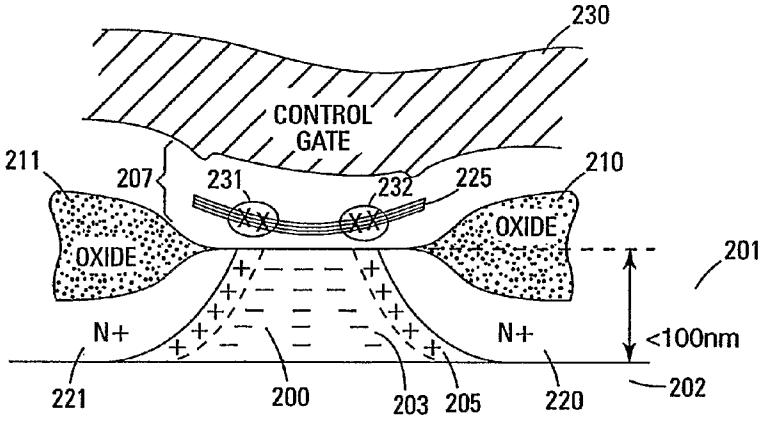
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(54) **Title:** NROM FLASH MEMORY DEVICES ON ULTRATHIN SILICON



(57) **Abstract:** An NROM flash memory cell is implemented in an ultra-thin silicon-on-insulator structure. In a planar device, the channel between the source/drain areas is normally fully depleted. An oxide layer provides an insulation layer between the source/drain areas and the gate insulator layer on top. A control gate is formed on top of the gate insulator layer. In a vertical device, an oxide pillar extends from the substrate with a source/drain area on either side of the pillar side. Epitaxidal regrowth is used to form ultra-thin silicon body regions along the sidewalk of the oxide pillar. Second source/drain areas are formed on top of this structure. The gate insulator and control gate are formed on top.

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