

PROCESS FOR FABRICATING A THERMO-OPTIC COMPONENT

FIELD OF THE INVENTION

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The present invention relates to the field of photonics. It in particular relates to a process for fabricating a thermo-optic component, i.e. a component the optical properties of which (refractive index to the first order) are modified via a local or global variation in temperature, generated by a heat source internal or external to the component.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

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Silicon photonics is increasingly receiving interest because this technology allows optical communication links to be improved via provision of many integrated functionalities, such as switches and optical phase-shifters, modulators, filters, lasers, etc.

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Switches and optical phase-shifters, in particular, must be able to efficiently convey a high number of signals while meeting specifications in respect of compactness, low power consumption and high switching speed. Because silicon has a high thermo-optic effect, compact and rapid thermo-optic switches have been able to be developed on silicon-on-insulator (SOI) substrates; mention may especially be made of components such as ring resonators or Mach-Zehnder interferometers.

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Document US2015253510 provides a compact thermo-optic switch that greatly minimizes the power required to achieve switching, because an optical waveguide thereof is formed suspended above the carrier substrate, mainly encircled by air and attached to said carrier substrate by way of pillars that limit heat flow:

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the thermal confinement improves the efficiency (limits the power consumption) of the switch. The architecture of this thermo-optic switch is obtained using an SOI substrate; the silicon surface layer and the buried oxide form the core of the optical waveguide and one portion of the optical confinement layer around the core, respectively, and a heating element is placed on the waveguide. Steps of structuring and etching, from the front side, the SOI substrate allow deep trenches and an air gap to be formed between the waveguide and the carrier substrate. One drawback of such an architecture may result from the fact that a plurality of peripheral regions of the thermo-optic component make contact with air: its transient response to temperature the variations generated by the heating element will therefore be degraded. In particular, the time required, on stoppage of the heating element, for the waveguide to return to a temperature T_0 from a higher temperature T_1 , i.e. the fall time, is increased because of the thermal inertia generated by the surrounding air.

SUBJECT OF THE INVENTION

The present invention relates to an alternative solution to those known in the prior art. The invention relates to a process for fabricating a thermo-optic component that permits good thermal insulation, favourable to the efficiency of the thermo-optic effect, while preserving a very good transient dynamic component response. The fabricating process also allows the component to be endowed with a high integration density and an excellent mechanical stability, while simplifying the fabricating steps.

BRIEF DESCRIPTION OF THE INVENTION

The present invention relates to a process for fabricating a thermo-optic component comprising the following steps:

a) providing a silicon-on-insulator (SOI) substrate comprising:

- 5 - a surface layer made of single-crystal silicon, extending in a main plane and placed on a dielectric layer, itself placed on a carrier made of silicon, and
- at least one buried cavity, which is formed in the carrier and which opens under the dielectric layer,
- 10 b) forming an optical waveguide extending in the main plane and comprising a core formed in the surface layer and encircled by an optical confinement layer including the dielectric layer,
- c) producing at least one heating element, on the optical
- 15 waveguide, said heating element being positioned, in the main plane, plumb with a segment of the optical waveguide, or on either side of said segment, the heating element and the segment of the optical waveguide being located plumb with the -at least one- buried cavity.

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According to some advantageous features of the invention, which may be implemented alone or in any achievable combination:

- in step b), an aperture is produced, through the optical waveguide, in order to place the -at least one- cavity under
- 25 an exterior pressure;
- said aperture is preserved, or plugged so as to hermetically seal the -at least one- cavity;
- the -at least one- cavity remains hermetically sealed throughout steps a), b) and c);
- 30 • the dielectric layer is made of silicon oxide and has a thickness comprised between 100 nm and 3 microns;
- the surface layer has a thickness comprised between 100 nm and 500 nm;

- the optical confinement layer comprises an additional dielectric layer having a thickness comprised between 0.5 and 1.5 microns;
- the -at least one- cavity has lateral dimensions, in the main plane, comprised between 10 microns and a few millimetres, and a depth, along an axis normal to the main plane, comprised between a few microns and 100 microns, and advantageously between 5 and 10 microns.

The invention also relates to a thermo-optic component produced using the fabricating process such as above, forming a switch, a phase-shifter, a modulator, a laser emitter, an amplifier, a directional coupler, a filter and/or a multiplexer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following detailed description, with reference to the appended figures, in which:

- Figures 1a to 1d show process sequences for providing the SOI substrate of step a) of the fabricating process according to the invention;
- Figure 2 shows step b) of the fabricating process according to the invention;
- Figure 3 shows step c) of the fabricating process according to the invention;
- Figures 4a and 4b show two architectures, seen from above, of thermo-optic components produced with the fabricating process according to the invention.

The figures are schematic representations which, for the sake of legibility, are not necessarily to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to the lateral dimensions along the x- and y-axes.

In the figures, the same references may be used for elements of the same nature.

The various possibilities (variants and embodiments illustrated and/or detailed in the description below) must be understood as not being exclusive from one another and may be combined together.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to a process for fabricating a thermo-optic component. By thermo-optic component what is meant is any type of optoelectronic device, such as a switch, a phase-shifter, a modulator, a directional coupler, a filter and an optical multiplexer, a laser emitter, an amplifier, etc., the optical properties of which (in particular, its refractive index to the first order) are modified by a local (or global) temperature variation generated by a heat source internal or external to the device.

The fabricating process makes provision to produce an optical waveguide 50 based on single-crystal silicon and a heating element 60, in proximity to a segment of the waveguide 50: the temperature variations generated by the heating element 60 in a segment 52' of the silicon core of the waveguide 50 will have the effect of modifying the refractive index of the silicon, thus changing the effective index of the optical mode in said guide 50.

The fabricating process comprises a step a) of providing a silicon-on-insulator (SOI) substrate 10 comprising a surface layer 4 made of single-crystal silicon, extending in a main plane (x, y) and placed on a dielectric layer 3, itself placed on a silicon carrier 1 (Figure 1d). The SOI substrate 10 preferentially takes the form of a circular wafer having a diameter comprised between 150 mm and 450 mm, the thickness of the carrier 1 typically varying between 300 microns and 1000 microns.

Advantageously, to meet the requirements of photonic applications, the surface layer 4 has a thickness comprised between 100 nm and 500 nm. This surface layer 4 is intended to form the core of an optical waveguide 50.

Again advantageously, but non-limitingly, the dielectric layer 3 is made of silicon oxide and has a thickness comprised between 100 nm and 3 microns.

The SOI substrate 10 further comprises at least one buried cavity 2, which is formed in the carrier 1 and which opens under the dielectric layer 3. Below, for the sake of simplicity reference will be made to a buried cavity 2, but it will be understood that the SOI substrate 10 advantageously comprises a plurality of cavities 2, which will be distributed in the main plane (x, y) in accordance with the architecture, with the type and with the number of thermo-optic components 100 intended to be provided on said SOI substrate 10. It will also be noted that all the buried cavities 2 do not necessarily have the same dimensions (length and width in the main plane (x, y), and depth along the z-axis normal to the main plane (x, y)), because they may be associated with various architectures or types of component.

The buried cavity 2 may have lateral dimensions, in the main plane (x, y), comprised between 10 microns and a few millimetres, and a depth comprised between a few microns and 100 microns, and

advantageously between 5 and 10 microns. It may have any shape in the main plane (x, y), for example, square, rectangular, polygonal, circular, annular, etc.

5 The buried cavity 2 of the SOI substrate 10 may be filled with a sacrificial solid material or be devoid thereof. In the latter case, it may be filled with air or with gas at atmospheric pressure or at a determined controlled pressure.

By way of example, the sacrificial material will possibly be
10 chosen from silicon oxide, for example low-density or doped silicon oxide, doped polysilicon, porous silicon, etc. The sacrificial material will optionally have an etch rate with respect to the other materials of the SOI substrate 10, namely with respect to the thermal silicon oxide and to the single-
15 crystal silicon, that is high enough to avoid significant etching of the substrate 10 when this sacrificial material is removed subsequently in the process.

The production of such an SOI substrate 10 with buried cavity 2
20 is preferably based on the thin-layer-transfer process known as the Smart Cut™ process.

Prior to the transfer of the surface layer 4, the carrier 1 used is a single-crystal silicon substrate the front side 1a of which has been etched to form the -at least one- cavity 2 (Figure 1a).

25 In the variant in which the cavity 2 is filled with a sacrificial material, said material is then deposited in the cavity 2 so as to lie flush with the silicon surface of the front side 1a.

Conventional steps of photolithography, masking, etching, deposition and polishing, which will not be described here, are
30 used to form the cavities, and to fill them if required.

A donor substrate 40 made of single-crystal silicon is implanted via its front side 40a, so as to define a buried weakened plane 41 substantially parallel to the front side 40a and delineating,

with the latter, the thin layer 3, 4 to be transferred (Figure 1b). The implantation is usually done with light species such as hydrogen or helium ions or a combination of these two species. The weakened plane 41 is so named because it comprises nano-

5 cracks in lenticular form generated by the implanted light species.

According to one preferred option, the thin layer 3, 4 to be transferred comprises, from the front side 40a of the donor substrate 40 to the buried weakened plane 41, a dielectric layer

10 3 and a silicon layer 4, which will form the buried dielectric layer 3 and the silicon surface layer 4 of the SOI substrate 10, respectively. It will therefore be understood that the implantation energy for the light species is chosen and adjusted so as to form the buried weakened plane (relatively localized at

15 the implantation peak) at the depth corresponding to the desired thickness of the surface layer 4, taking into account finishing steps (mentioned below) which consume some of the material of said layer 4.

20 The donor substrate 40 and the carrier 1 are then joined, by direct bonding between the front sides 40a, 1a of said substrates 40, 1, to form a bonded structure (Figure 1c). As well known in the field of direct bonding, cleans and/or activations of the surface of the front sides 40a, 1a will possibly be carried out

25 to obtain an excellent quality bond. It is possible for the substrates to be joined under a controlled atmosphere; this especially allows the pressure in the cavities (which are buried subsequent to said joining operation) to be controlled, when said cavities are devoid of sacrificial material.

30 The cleave in the buried weakened plane 41 preferably results from application of a heat treatment at medium temperature, typically between 350°C and 500°C, because of growth in microcracks via coalescence and pressurization of gaseous

species (Figure 1d). Alternatively or conjointly, the cleave may result from application of a mechanical stress to the bonded structure.

At the end of this cleave, on the one hand an intermediate SOI substrate and on the other hand the rest 40' of the donor substrate are obtained. Finishing sequences comprising cleans, surface treatments (etching, polishing, etc.) and/or heat treatments are conventionally applied to the intermediate SOI substrate, so as to ensure the silicon surface layer 4 again has a good surface finish (roughness and number of defects) and a good crystal quality. Following this, the SOI substrate 10 is available.

Although the production of the SOI substrate 10 with buried cavity 2 has been described here with reference to the Smart-Cut process, such an SOI substrate 10 may also be produced using other thin-layer-transfer processes known in the art.

The fabricating process according to the invention then comprises a step b) of forming an optical waveguide 50 extending in the main plane (x, y) and comprising a core 52, 52' formed in the surface layer 4 and encircled by an optical confinement layer 53 including the dielectric layer 3 (Figure 2).

The formation of the optical waveguide 50 requires the surface layer 4 to be etched locally, so as to define the dimensions and the shape of the guide in the main plane (x,y).

Figures 4a and 4b illustrate two different architectures of the waveguide 50, in the case of a Mach-Zehnder interferometer and in the case of a ring resonator, seen from above, i.e. in the main plane (x, y), respectively. The core 52, 52' of the waveguide 50, one or more segments 52' of which are located plumb with the one or more cavities 2 (dashed lines in Figures 4a and

4b) may be seen therein. The length of the core 52 in the main plane (x, y) may vary depending on the targeted architecture; its width is conventionally comprised between 0.2 and 1 micron, and preferably between 0.3 and 0.6 microns.

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The formation of the optical waveguide 50 also requires an additional dielectric layer 3' to be deposited, on the core 52, 52', so as to encapsulate the latter in a cladding, here called the optical confinement layer 53, including the dielectric layer 3 of the SOI substrate 10. The additional dielectric layer 3' is preferably made of silicon oxide. Its thickness is typically comprised between 0.5 and 1.5 microns.

In step b), advantageously after the waveguide 50 has been formed, an aperture (not shown) may be produced, through the optical waveguide 50, in order to place the -at least one- cavity 2 under an exterior pressure. The aperture is typically produced through the confinement layer 53, outside the region comprising the silicon core 52, 52'. This aperture will possibly be preserved, or be plugged to seal the cavity 2 after this placement under exterior pressure.

In the case where the buried cavity 2 is filled with a sacrificial material, (at least) one aperture is formed so as to allow said material to be accessed and a, wet or dry, etch aiming to remove the material and to empty the buried cavity 2 of its solid material to be carried out. Once again, the aperture will possibly be preserved or plugged after the cavity 2 has been emptied.

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It will be recalled that the cavity 2 is hermetically sealed at the end of step a) and may, in certain embodiments, remain in this state in steps b) and/or c), or even after fabrication of the thermo-optic component, during use thereof. The hermetic

character of the cavity 2 makes it possible to avoid effects due to unwanted penetration of gaseous or liquid species into this cavity 2 during the fabricating process, these effects potentially generating problems with drying, bonding of the upper membrane, various types of contamination, degradation of the upper membrane, etc. Keeping the cavity 2 hermetic during use of the component may also allow the reproducibility of the operating point (especially in terms of thermal environment and mechanical deformation) to be ensured.

The fabricating process then comprises a step c) of producing at least one heating element 60, on the optical waveguide 50 (Figure 3). This heating element 60 is placed, in the main plane (x, y) plumb with the buried cavity 2. Advantageously, the dimensions in this plane of the heating element 60 are smaller than those of the cavity 2, as illustrated in Figures 3, 4a and 4b.

Thus, again in the main plane (x, y), the heating element 60 is positioned either plumb with the core segment 52' of the optical waveguide 50, or on either side of said segment 52' (Figures 4a, 4b). This segment 52' corresponds to the portion of the waveguide 50 that will undergo the temperature variations applied by the heating element 60, and that will therefore endow the component 100 with its thermo-optic properties.

According to one particular exemplary embodiment, the heating element 60 is formed by depositing a Ti/TiN stack directly on the confinement layer 53, plumb with the segment 52' of the waveguide. The stack may have a thickness of about 100 nm.

The heating element 60 further comprises two metal contact pads, which are intended to be connected to a current source. When a current is applied, the heating element 60 dissipates heat via

Joule heating and thus increases the temperature experienced by the core segment 52' of the waveguide 50.

5 The fabricating process according to the invention is simple and effective: it limits the technological steps required to define and insulate the thermo-optic component 100, which steps are especially based on chemical etches that are often difficult to control; it also allows a high integration density to be
10 achieved. The presence of (at least) one buried cavity 2 in the SOI substrate 10 facilitates the thermal insulation of the waveguide segment 52' intended to generate the thermo-optic effect, this allowing thermal losses via conduction to be limited, the air or gas in the cavity forming an excellent
15 insulator. In parallel, the thermal continuity of the optical confinement layer 53 around the core 52 of the optical waveguide 50 ensures a low transient response time during the temperature variations of the heating element 60, thus endowing the component 100 with a very good responsiveness. The presence of the
20 dielectric layer 3 under the core 52' of the optical waveguide allows a good compromise to be obtained between component response speed and the energy efficiency of the control thereof. The fabricating process according to the invention further procures thermo-optic components 100 that are robust because
25 complex etches via the front side or via the back side of the SOI substrate 10 are not required to form the insulation, these etches being liable to decrease the mechanical strength of the component.

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Needless to say, the invention is not limited to the embodiments described and variant embodiments may be employed without departing from the scope of the invention such as defined by the claims.

CLAIMS

1. Process for fabricating a thermo-optic component (100) comprising the following steps:

5 a) providing an SOI substrate (10) comprising:

- a surface layer (4) made of single-crystal silicon, extending in a main plane (x, y) and placed on a dielectric layer (3), itself placed on a carrier (1) made of silicon, and

10 - at least one buried cavity (2), which is formed in the carrier (1) and which opens under the dielectric layer (3), then,

b) forming an optical waveguide (50) extending in the main plane (x, y) and comprising a core (52, 52') formed in the surface layer (4) and encircled by an optical confinement layer (53) including the dielectric layer (3), then,

15 c) producing at least one heating element (60), on the optical waveguide (50), said heating element (60) being positioned, in the main plane (x, y), plumb with a segment (52') of the optical waveguide (50), or on either side of said segment (52'), the heating element (60) and the segment (52') of the optical waveguide being located plumb with the -at least one- buried cavity (2).

25 2. Process for fabricating a thermo-optic component (100) according to the preceding claim, wherein, in step b), an aperture is produced through the optical waveguide (50), in order to place the -at least one- cavity (2) under an exterior pressure.

30 3. Process for fabricating a thermo-optic component (100) according to the preceding claim, wherein said aperture is plugged so as to hermetically seal the -at least one- cavity (2).

4. Process for fabricating a thermo-optic component (100) according to Claim 1, wherein the -at least one- cavity (2) remains hermetically sealed throughout steps a), b) and c).

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5. Process for fabricating a thermo-optic component (100) according to one of the preceding claims, wherein the dielectric layer (3) is made of silicon oxide and has a thickness comprised between 100 nm and 3 microns.

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6. Process for fabricating a thermo-optic component (100) according to one of the preceding claims, wherein the surface layer (4) has a thickness comprised between 100 nm and 500 nm.

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7. Process for fabricating a thermo-optic component (100) according to one of the preceding claims, wherein the optical confinement layer (53) comprises an additional dielectric layer (3') having a thickness comprised between 0.5 and 1.5 microns.

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8. Process for fabricating a thermo-optic component (100) according to one of the preceding claims, wherein the -at least one- cavity (2) has lateral dimensions, in the main plane (x, y), comprised between 10 microns and a few millimetres, and a depth, along an axis (z) normal to the main plane (x, y), comprised between a few microns and 100 microns, and advantageously between 5 and 10 microns.

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9. Thermo-optic component (100) produced using the fabricating process according to one of the preceding claims, forming a switch, a phase-shifter, a modulator, a laser emitter, an amplifier, a directional coupler, a filter and/or a multiplexer.

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