cyan light;

extended color light comprising visible light and near-infra red light;

green light;

infra-red light;

magenta light;

near-infra red light;

red light;

yellow light; and

white light.

21. The imager array of claim 1, wherein:

a first array of adjacent pixels in a first focal plane have a first capture band;

a second array of adjacent pixels in a second focal plane have a second capture band, where the first and second capture bands are the same;

the peripheral circuitry is configured so that the integration time of the first array of adjacent pixels is a first time period; and

the peripheral circuitry is configured so that the integration time of the second array of adjacent pixels is a second time period, where the second time period is longer than the first time period.

21. The imager array of claim 1, wherein at least one of the focal planes includes an array of adjacent pixels, where the pixels in the array of adjacent pixels are configured to capture different colors of light.

22. The imager array of claim 21, wherein the array of adjacent pixels employs a Bayer filter pattern.

23. The imager array of claim 22, wherein:

the plurality of focal planes is arranged as a 2 x 2 array of focal planes;

a first focal plane in the array of focal planes includes an array of adjacent pixels that employ a Bayer filter pattern;

a second focal plane in the array of focal planes includes an array of adjacent pixels configured to capture green light;

a third focal plane in the array of focal planes includes an array of adjacent pixels configured to capture red light; and

a fourth focal plane in the array of focal planes includes an array of adjacent pixels configured to capture blue light.

24. The imager array of claim 22, wherein the plurality of focal planes is arranged as a two dimensional array of focal planes having at least three focal planes in one dimension.

25. The imager array of claim 22, wherein the plurality of focal planes is arranged as a two dimensional array of focal planes having at least three focal planes in both dimensions.

26. The imager array of claim 1, wherein the control circuitry comprises a global counter.

27. The imager array of claim 26, wherein the control circuitry is configured to stagger the start points of image read-out such that each focal plane has a controlled temporal offset with respect to a global counter.

28. The imager array of claim 26, wherein the control circuitry is configured to separately control the integration times of the pixels in each focal plane based upon the capture band of the pixels in the focal plane using the global counter.

29. The imager array of claim 26, wherein the control circuitry is configured to separately control the frame rate of each focal plane based upon the global counter.

30. The imager array of claim 26, wherein the control circuitry further comprises a pair of pointers for each focal plane.

31. The imager array of claim 30, wherein the offset between the pointers specifies an integration time.

32. The imager array of claim 30, wherein the offset between the pointers is programmable.

33. The imager array of claim 1, wherein the control circuitry comprises a row controller dedicated to each focal plane.

34. The imager array of claim 1, wherein:

the imager array includes an array of M x N focal planes;

the control circuitry comprises a single row decoder circuit configured to address each row of pixels in each row of M focal planes.

35. The imager array of claim 34, wherein:

the control circuitry is configured to generate a first set of pixel level timing signals so that the row decoder and a column circuit sample a first row of pixels within a first focal plane; and

the control circuitry is configured to generate a second set of pixel level timing signals so that the row decoder and a column circuit sample a second row of pixels within a second focal plane.

36. The imager array of claim 1, wherein each focal plane has dedicated sampling circuitry.

37. The imager array of claim 1, wherein at least a portion of the sampling circuitry is shared by a plurality of the focal planes.

38. The imager array of claim 37, wherein:

the imager array includes an array of M x N focal planes;

the sampling circuitry comprises M analog signal processors (ASPs) and each ASP is configured to sample pixels read-out from N focal planes.

39. The imager array of claim 38, wherein:

each ASP is configured to receive pixel output signals from the N focal planes via N inputs; and

each ASP is configured to sequentially process each pixel output signal on its N inputs.

40. The imager array of claim 38, wherein:

the control circuitry is configured so that a single common analog pixel signal readout line is shared by all pixels in a group of N focal planes; and

the control circuitry is configured to control the capture of image data to time multiplex the pixel output signals received by each of the M ASPs.

41. The imager array of claim 37, wherein:

the imager array includes an array of M x N focal planes;

the sampling circuitry comprises a plurality of analog signal processors (ASPs) and each ASP is configured to sample pixels read-out from a plurality of focal planes;

the control circuitry is configured so that a single common analog pixel signal readout line is shared by all pixels in the plurality of focal planes; and

the control circuitry is configured to control the capture of image data to time multiplex the pixel output signals received by each of the plurality of ASPs.

42. The imager array of claim 1, wherein the sampling circuitry comprises analog front end (AFE) circuitry and analog-to-digital conversion (ADC) circuitry.

43. The imager array of claim 42, wherein the sampling circuitry is configured so that each focal plane has a dedicated AFE and at least one ADC is shared between at least two focal planes.

44. The imager array of claim 43, wherein the sampling circuitry is configured so that at least one ADC is shared between a pair of focal planes.

45. The imager array of claim 43, wherein the sampling circuitry is configured so that at least one ADC is shared between four focal planes.

46. The imager array of claim 45, wherein the sampling circuitry is configured so that at least one AFE is shared between at least two focal planes.

47. The imager array of claim 46, wherein the sampling circuitry is configured so that at least one AFE is shared between a pair of focal planes.

48. The imager array of claim 47, wherein the sampling circuitry is configured so that two pairs of focal planes that each share an AFE collectively share an ADC.

49. The imager array of claim 1, wherein the control circuitry is configured to separately control the power down state of each focal plane and associated AFE circuitry or processing timeslot therein.

50. The imager array of claim 49, wherein the control circuitry configures the pixels of at least one inactive focal plane to be in a constant reset state.

51. The imager array of claim 1, wherein at least one focal plane includes reference pixels to calibrate pixel data captured using the focal plane.

52. The imager array of 51, wherein:

the control circuitry is configured to separately control the power down state of the focal plane's associated AFE circuitry or processing timeslot therein; and

the control circuitry is configured to power down the focal plane's associated AFE circuitry or processing timeslot therein without powering down the associated AFE circuitry or processing timeslot therein for readout of the reference pixels of the focal plane.

cyan light;

extended color light comprising visible light and near-infra red light;

green light;

infra-red light;

magenta light;

near-infra red light;

red light;

yellow light; and

white light.

21. The imager array of claim 1, wherein:

a first array of adjacent pixels in a first focal plane have a first capture band;

a second array of adjacent pixels in a second focal plane have a second capture band, where the first and second capture bands are the same;

the peripheral circuitry is configured so that the integration time of the first array of adjacent pixels is a first time period; and

the peripheral circuitry is configured so that the integration time of the second array of adjacent pixels is a second time period, where the second time period is longer than the first time period.

22. The imager array of claim 1, wherein at least one of the focal planes includes an array of adjacent pixels, where the pixels in the array of adjacent pixels are configured to capture different colors of light.

23. The imager array of claim 22, wherein the array of adjacent pixels employs a Bayer filter pattern.

24. The imager array of claim 23, wherein:

the plurality of focal planes is arranged as a 2 x 2 array of focal planes;

a first focal plane in the array of focal planes includes an array of adjacent pixels that employ a Bayer filter pattern;

a second focal plane in the array of focal planes includes an array of adjacent pixels configured to capture green light;

a third focal plane in the array of focal planes includes an array of adjacent pixels configured to capture red light; and

a fourth focal plane in the array of focal planes includes an array of adjacent pixels configured to capture blue light.

25. The imager array of claim 23, wherein the plurality of focal planes is arranged as a two dimensional array of focal planes having at least three focal planes in one dimension.

26. The imager array of claim 23, wherein the plurality of focal planes is arranged as a two dimensional array of focal planes having at least three focal planes in both dimensions.

27. The imager array of claim 1, wherein the control circuitry comprises a global counter.

28. The imager array of claim 27, wherein the control circuitry is configured to stagger the start points of image read-out such that each focal plane has a controlled temporal offset with respect to a global counter.

29. The imager array of claim 27, wherein the control circuitry is configured to separately control the integration times of the pixels in each focal plane based upon the capture band of the pixels in the focal plane using the global counter.

30. The imager array of claim 27, wherein the control circuitry is configured to separately control the frame rate of each focal plane based upon the global counter.

31. The imager array of claim 27, wherein the control circuitry further comprises a pair of pointers for each focal plane.

32. The imager array of claim 31, wherein the offset between the pointers specifies an integration time.

33. The imager array of claim 31, wherein the offset between the pointers is programmable.

34. The imager array of claim 1, wherein the control circuitry comprises a row controller dedicated to each focal plane.

35. The imager array of claim 1, wherein:

the imager array includes an array of M x N focal planes;

the control circuitry comprises a single row decoder circuit configured to address each row of pixels in each row of M focal planes.

36. The imager array of claim 35, wherein:

the control circuitry is configured to generate a first set of pixel level timing signals so that the row decoder and a column circuit sample a first row of pixels within a first focal plane; and

the control circuitry is configured to generate a second set of pixel level timing signals so that the row decoder and a column circuit sample a second row of pixels within a second focal plane.

37. The imager array of claim 1, wherein each focal plane has dedicated sampling circuitry.

38. The imager array of claim 1, wherein at least a portion of the sampling circuitry is shared by a plurality of the focal planes.

39. The imager array of claim 38, wherein:

the imager array includes an array of M x N focal planes;

the sampling circuitry comprises M analog signal processors (ASPs) and each ASP is configured to sample pixels read-out from N focal planes.

40. The imager array of claim 39, wherein:

each ASP is configured to receive pixel output signals from the N focal planes via N inputs; and

each ASP is configured to sequentially process each pixel output signal on its N inputs.

41. The imager array of claim 39, wherein:

the control circuitry is configured so that a single common analog pixel signal readout line is shared by all pixels in a group of N focal planes; and

the control circuitry is configured to control the capture of image data to time multiplex the pixel output signals received by each of the M ASPs.

42. The imager array of claim 38, wherein:

the imager array includes an array of M x N focal planes;

the sampling circuitry comprises a plurality of analog signal processors (ASPs) and each ASP is configured to sample pixels read-out from a plurality of focal planes;

the control circuitry is configured so that a single common analog pixel signal readout line is shared by all pixels in the plurality of focal planes; and

the control circuitry is configured to control the capture of image data to time multiplex the pixel output signals received by each of the plurality of ASPs.

43. The imager array of claim 1, wherein the sampling circuitry comprises analog front end (AFE) circuitry and analog-to-digital conversion (ADC) circuitry.

44. The imager array of claim 43, wherein the sampling circuitry is configured so that each focal plane has a dedicated AFE and at least one ADC is shared between at least two focal planes.

45. The imager array of claim 44, wherein the sampling circuitry is configured so that at least one ADC is shared between a pair of focal planes.

46. The imager array of claim 44, wherein the sampling circuitry is configured so that at least one ADC is shared between four focal planes.

47. The imager array of claim 46, wherein the sampling circuitry is configured so that at least one AFE is shared between at least two focal planes.

48. The imager array of claim 47, wherein the sampling circuitry is configured so that at least one AFE is shared between a pair of focal planes.

49. The imager array of claim 48, wherein the sampling circuitry is configured so that two pairs of focal planes that each share an AFE collectively share an ADC.

50. The imager array of claim 1, wherein the control circuitry is configured to separately control the power down state of each focal plane and associated AFE circuitry or processing timeslot therein.

51. The imager array of claim 50, wherein the control circuitry configures the pixels of at least one inactive focal plane to be in a constant reset state.

52. The imager array of claim 1, wherein at least one focal plane includes reference pixels to calibrate pixel data captured using the focal plane.

53. The imager array of 52, wherein:

the control circuitry is configured to separately control the power down state of the focal plane's associated AFE circuitry or processing timeslot therein; and

the control circuitry is configured to power down the focal plane's associated AFE circuitry or processing timeslot therein without powering down the associated AFE circuitry or processing timeslot therein for readout of the reference pixels of the focal plane.