Description

This invention relates to a progressive scan video processor that generates noninterlaced lines of video from an interlaced video signal.

Recent interest in the development of high definition television systems has been directed to techniques intended to enhance the subjective performance of present systems within the constraints of existing standards. In one approach, progressive or noninterlaced scanning is used. The incoming video signal, supplied in a conventional two-to-one vertical interlaced format, is first stored in a memory and then subsequently read out of the memory at a double line rate in a noninterlaced or line progressively scanned manner. Each line of incoming video generates two lines of display video. (See "Fernseh- & Kino-Technik Vol 37 (1983) Mai, No 5, pages 190-191).

One form of a progressive scan video processor is a line interpolation progressive scan system using line stores to generate time compressed lines of luminance and chrominance video from the luminance and chrominance information contained in the interlaced video lines within the same field. To avoid the loss of sharpness in vertical transitions that may occur when using line interpolation progressive scan, vertical peaking information is inserted into the noninterlaced time compressed lines of display video. To properly display the peaking portions in the display video, the vertical peaking information alternates in polarity from one time compressed video line to the next time compressed line of video.

In accordance with an aspect of the invention, the memory storage requirement in a line progressive video processing system is kept small by providing two time compression stages operated in parallel. Each of the time compression stages processes interlaced luminance and chrominance signals which are generated at a first line rate. Each processor extracts vertical peaking information from the interlaced luminance information to generate a time compressed enhanced luminance signal that is generated at a second faster line rate that is a multiple of the first line rate. The enhanced luminance signal contains vertical peaking information in the proper opposite polarities in alternate lines of time compressed display video.

In accordance with another aspect of the invention, the time compression stages are adaptable for use with conventional interlaced digital video signal processors that generate interlaced luminance signals that are already enhanced with vertical detail information. In a line progressive scan video processing system, vertical peaking of opposite polarities is derived from the vertical detail information. The time compression stages, in accordance with this aspect of the invention, process the interlaced luminance signal so as to first extract the vertical detail information, generate vertical peaking information of opposing polarities from the extracted vertical detail information, and then reinsert the vertical detail information and the vertical peaking information into the luminance channel to produce time compressed lines of luminance video that contain both vertical detail information and vertical peaking information of opposing polarities in alternate time compressed lines.

FIGURE 1 illustrates a progressive scan video processor embodying the invention;

FIGURE 2 illustrates a specific embodiment of a speed-up processor used in the circuit of FIGURE 1; and

FIGURE 3a-3m illustrate waveforms useful in explaining the operation of the circuits of FIGURES 1 and 2.

In progressive scan video processor 20, illustrated in FIGURE 1, a composite color video signal V_{in} is developed at a terminal 21 by conventional television receiver circuitry, not illustrated. Video signal V_{in} comprises an interlaced signal, such as a color NTSC signal, wherein 525 video lines are generated each frame, at a 30Hz frame rate with a two-to-one interlace factor, wherein the video line rate of f_H is 15.734 kilohertz, and wherein the frequency f_{sc} of the color subcarrier is 3.58 megahertz. Video processor 20 may be suitably modified to process interlaced video signals in other formats. Video signal V_{in} is applied to a signal sampling circuit, shown as an analog-to-digital converter (ADC) 22,clocked at a $4f_{sc}$ rate, to develop digital samples of the video signal at the $4f_{sc}$ rate. The sampled video signal is coupled to a system clock generator 35 for developing various clock signals in progressive scan video processor 20 that are synchronized with the synchronizing signals in the video signal, such as with the color burst signal and the horizontal sync signal. System clock generator 35 generates a clock signal f_H,ck, illustrated in FIGURE 3a, that repeats at the horizontal line rate f_H; a clock signal $f_H/2$,ck, illustrated in FIGURES 3b and 3c, that repeats at half of the line rate, or at a rate of $f_H/2$; a clock signal $\overline{f_H/2,ck}$, illustrated in FIGURE 3e, that is 180° out of phase with the clock signal $f_H/2$,ck, a clock signal f_{sc},ck, repeating at the color subcarrier frequency f_{sc}, a clock signal $2f_{sc}$,ck, repeating at a rate of two times the color subcarrier frequency, a clock signal $4f_{sc}$,ck, repeating at a rate of four times the color subcarrier frequency, and a clock signal $8f_{sc}$,ck, repeating at a rate of eight times the color subcarrier frequency.

Sampled interlaced video signal V_{in} is applied to a line comb filter 23 which comprises a 1-H delay unit 24, an adder 25 which arithmetically

adds the delayed video line to the undelayed video line, and a subtractor 26 which arithmetically subtracts the delayed video line from the undelayed video line.

Delay unit 24 may comprise a CCD delay line that stores samples of the interlaced video signal. For digital samples comprising digital words in binary format wherein each digital sample comprises one byte eight bits in length, for example, delay unit 24 may comprise a digital memory such as a random access memory (RAM). Assume for illustrative purposes that ADC 22 generates digital samples as digital words of eight bit bytes, and delay unit 24 comprises a random access memory. The storage capacity of 1-H delay 24 is large enough to store sufficient samples of the incoming video signal V_{in} to adequately sample the highest video frequencies occurring in the video signal. For an NTSC video signal having a luminance bandwidth of approximately 4.2 megahertz, a sampling rate of $4f_{sc}$ is adequate to satisfy the above criterion. Clock signal $4f_{sc}$,ck is therefore coupled to the sample clock terminal of delay unit 24.

At a sampling rate of $4f_{sc}$, the capacity required for delay unit 24 to store one video line is 910 samples. Assuming delay unit 24 comprises a RAM, then the memory size of delay unit 24 is 910 eight bit bytes or 7280 bits. Define a standard memory size, 1 RMU, as 227 eight bit bytes, then the memory capacity of 1-H delay 24 comprises approximately 4 RMU, a capacity sufficient to store one line of NTSC video at a sampling rate of $4f_{sc}$.

A combed luminance signal Y_{cm} is developed by comb filter 23 at the output of adder 25. The digital samples of combed luminance signal Y_{cm} are developed at a $4f_{sc}$ rate. A combed signal is developed by comb filter 23 at the output of subtractor 26 that contains chrominance information in the frequency range around the color subcarrier frequency f_{sc} and that contains luminance vertical detail information at lower frequencies, below frequencies of 1.5 to 1.8 megahertz, for example. The digital samples at the output of subtractor 26 are also developed at the $4f_{sc}$ rate.

A bandpass filter 32 removes from the output of subtractor 26 frequencies below and above the modulated chrominance frequencies to develop a chrominance signal C. Chrominance signal C is coupled to chrominance processor 33. Chrominance processor 33 provides automatic color control and other processing functions and performs color demodulation to develop digital samples of the color mixture signal I at one output and digital samples of the quadrature related color mixture signal Q at another output. Because the frequency range of the color mixture signals are much narrower than that of the luminance signal, the sample rate of the I and Q digital signals is at the lower, f_{sc} rate.

The combed signal at the output of subtractor 26 is coupled to a low pass filter 27 to separate the luminance vertical detail information from the chrominance information. A luminance signal Y_D at the output of filter 27 contains separated luminance vertical detail information.

Vertical detail signal Y_D and combed luminance signal Y_{cm} are added in an adder 29 to restore vertical detail information into the luminance channel. Horizontal peaking is provided by a horizontal peaking stage 30, and contrast adjustment of the luminance signal both automatically and under viewer control is accomplished by a contrast stage 31 to develop a luminance signal Y. The digital samples of luminance signal Y are developed at the $4f_{sc}$ rate.

In addition to vertical detail restoration, enhancement of vertical transitions in the luminance signal may be accomplished by providing vertical peaking during vertical transitions. The vertical detail luminance signal Y_D is coupled to a nonlinear processor, vertical peaking stage 28, of conventional design, to develop a luminance peaking signal Y_P that contains only preshoot and overshoot information of vertical transitions. Vertical peaking signal Y_P is coupled to adder 29 via the arm and contact terminal #1 of a controllable switch 34. The throw position of switch 34 is controlled by the logical state of a control terminal 39. When the state of control terminal 39 is high, for example, the arm of switch 34 makes contact with terminal #1 as illustrated by the dotted line arm position of FIGURE 1. When the state of control terminal 39 is low, the arm of switch 34 makes contact with terminal #2 as illustrated by the solid line arm position of FIGURE 1. Thus, if it is desired to enhance luminance signal Y by incorporating vertical peaking, a highstate is developed at control terminal 39; whereas if it desired to omit vertical peaking from luminance signal Y, a low state is developed at control terminal 39.

As thus far described, the video processing of interlaced video signal V_{in} has been performed in a conventional manner using known prior art circuits and techniques to generate interlaced luminance signal Y and interlaced color mixture signals I and Q. Such video processing stages encompassed within the box labeled IVPU, may be provided using one or more conventionally designed integrated circuits.

Progressive scan video processor 20 will be seen to use a conventional interlaced video processor unit, such as processor unit IVPU, to generate noninterlaced lines of luminance from interlaced lines of luminance. In accordance with an aspect of the invention, each of the three interlaced component signals Y,I,Q is coupled to each of two speed-

up processors, PSP1 and PSP2. The two processors are operated in parallel to generate two sets of time compressed, double line rate luminance and color mixture video component signals, that are multiplexed for noninterlaced display. Because the entire speed-up processing requires relatively large memory capacity, parallel operation reduces the memory storage requirements of an individual unit by one half.

In accordance with an aspect of the invention, the vertical detail information is extracted from the interlaced luminance signal developed by the IVPU unit and then separately time compressed. In accordance with another aspect of the invention, vertical peaking information is derived from the extracted vertical detail information and inserted into the time compressed luminance signal generated by speed-up processors PSP1 and PSP2.

To precondition interlaced video processor unit IVPU to operate as part of progressive scan video processor 20, vertical peaking signal V_P is omitted from interlaced luminance signal Y. Vertical peaking is omitted because the peaking will be performed later in progressive scan speed-up processors PSP1 and PSP2, as described below.

A signal P is coupled to terminal 39 of switch 34. Signal P exhibits a low state when progressive scan video processing is being performed. Signal P may be generated by, for example, grounding terminal 39. With control terminal 39 in the low state, the arm of switch 34 makes contact with terminal #2, preventing signal Y_P from being inserted into interlaced luminance signal Y.

In FIGURE 1, each of the three interlaced video component signals,Y,I,Q, is coupled to each of the two progressive scan speed-up processors PSP1 and PSP2. Speed-up processors PSP1 and PSP2 are similarly designed and are controlled for parallel processing operation by means of various clock and control signals coupled to sampling clock terminals CK1 through CK4 and control terminals R/ $\overline{W}$ and CKM of the speed-up units, as described later on.

Digital samples coupled to either one of the speed-up processors PSP1 and PSP2 are written into memory when the corresponding control terminal R/ $\overline{W}$ is in the low state. Digital samples are read out of the memory when the control terminal R/ $\overline{W}$ is in the high state. Clock signal $f_H/2,ck$ illustrated in FIGURE 3c, is coupled to control terminal R/ $\overline{W}$ of speed-up processor PSP1. The 180° out-of-phase clock signal $\overline{f_H/2,ck}$ is coupled to control terminal R/ $\overline{W}$ of speed-up processor PSP2. Thus, when one of the speed-up processors is writing into its memory video samples of the component signals Y, I and Q, the other speed-up processor is reading out of its memory the previously stored line of video samples.

Assume the component signals Y, I and Q, coupled to each of speed up processors PSP1 and PSP2, contain samples of the nth interlaced video line between times t_1 and t_3, as schematically represented in FIGURE 3g. During this interval, control terminal R/ $\overline{W}$ of speed-up processor PSP2 is low as illustrated in FIGURE 3e. Write clock terminals CK1 and CK3 in speed-up processor PSP2 are enabled, permitting the luminance digital samples Y developed at the $4f_{sc}$ rate and the color mixture samples, I and Q, each developed at the f_{sc} rate, to be written into their respective memory locations, as schematically indicated by the vertical line sampling clocks illustrated in FIGURE 3f between times t_1 and t_3.

Internal to the speed-up processor, in a manner that is described later, vertical peaking is added to the vertical detail information contained in the luminance signal.

During the interval t_1 through t_3, control terminal R/ $\overline{W}$ of speed-up processor PSP1 is in the high state, as illustrated in FIGURE 3c. Read clock terminals CK2 and CK4 of speed-up processor PSP1 are enabled. As schematically indicated by the vertical line sampling clocks of FIGURE 3d, the stored samples of luminance information are read out of memory at the $8f_{sc}$ rate, double the $4f_{sc}$ rate at which they were written into the memory, and the stored samples of I and Q color mixture information are read out of memory at the $2f_{sc}$ rate, double the rate at which they were written into memory. Thus, for each interlaced video line of the three component signals Y, I and Q stored in speed-up processor PSP1 there are generated two, time compressed, double line rate, $2f_H$ lines of display video.

Internal to speed-up processor PSP1, as described later, the vertical peaking information is opposing in polarity in alternate lines of the time compressed, double line rate luminance signal. As illustrated in FIGURE 3h, when line n of the interlaced video signal V_{in} is developed at terminal 21 of FIGURE 1, time compressed signals are developed at the luminance output signal line 70Y of speed-up processor PSP1 that contain luminance information from the previous line n-1. During the interval t_1 through t_2, a time compressed line of luminance display video Y''_{2X-} is generated, containing vertical peaking information of one polarity. During the interval t_2 through t_3, a time compressed line of luminance display video Y''_{2X+} is generated, containing vertical peaking information of the opposite polarity. Such alternating of the polarities of the vertical peaking information is required in line interpolation progressive scanning to properly locate preshoots and overshoots in vertical transitions.

To generate time compressed, double line rate

color mixture signals on the I and Q output signal lines 70I and 70Q, respectively, of speed-up processor PSP1, an interlaced video line of the I and Q component signals that is stored in the speed-up processor is read out of memory twice, and at the faster, $2f_{sc}$ rate. Thus, as illustrated in FIGURE 3j, the previous line n-1 of video is read out of memory both during the intervals t_1 through t_2 and t_2 through t_3, as the time compressed I and Q signal components I''_{2x} and Q''_{2x}.

During the next interlaced video line interval, between time t_3 and time t_5 of FIGURES 3a-3m, the operating modes of speed-up processors PSP1 and PSP2 interchange, with speed-up processor PSP1 operating in the write mode and speed-up processor PSP2 operating in the read mode.

To generate a complete sequence of pairs of noninterlaced lines of display video from the information contained in the interlaced lines of video signal V_{in}, the outputs of speed-up processors PSP1 and PSP2 are multiplexed onto respective signal lines 40Y, 40I and 40Q by a multiplexer MUX 1. Output signal lines 70Y, 70I, 70Q of speed-up processors PSP1 and PSP2 are coupled to respective input ports of MUX 1, with input ports A1, B1, C1 receiving signals from speed-up processor PSP1 and with input ports A2, B2, C2 receiving signals from speed-up processor PSP2. The control clock signal, $f_H/2$,ck, is coupled to the select terminal, SEL, of MUX 1. When select terminal SEL is high, the signals coupled to input ports A1, B1, C1 are transferred to output ports A3, B3, C3, respectively. When select terminal SEL is low, the signals coupled to input ports A2, B2, C2 are transferred to the output ports.

The time compressed, double line rate luminance' signal Y_{2x} developed at output port A3 on a signal line 40Y is schematically illustrated in FIGURE 3L. Video lines of the signal Y_{2x} alternate between a time compressed line of luminance that contains vertical peaking in one polarity and a time compressed line of luminance that contains vertical peaking in the opposite polarity. The time compressed, double line rate color mixture signals I_{2x} and Q_{2x}, developed at output ports B3 and C3, respectively, are illustrated schematically in FIGURE 3m. During one line interval, $1/f_H$, of the interlaced video signal V_{in} , a time compressed video line of the signals I_{2x} and Q_{2x} is twice generated for display in a pair of noninterlaced scan lines.

The time compressed component signals Y_{2x}, I_{2x}, Q_{2x} are coupled to respective digital-to-analog converters 36Y, 36I, 36Q for conversion to analog component signals.

Multiplexer MUX 1 may be eliminated if output signal lines 70Y, 70I and 70Q of each of the speed-up processors PSP1 and PSP2 are tri-state outputs, wherein the signal lines are in an open-circuit state when the speed-up processor is in the write mode of operation. In this case, output signal lines 70Y, 70I and 70Q of PSP1 are tied to output signal lines 70Y, 70I and 70Q of PSP2, respectively. The tied-together output signal lines are then directly coupled to digital-to-analog converters 36Y, 36I and 36Q, respectively.

The analog signals from converters 36Y, 36I, 36R are combined in a color matrix 37 to generate time compressed, double line rate, noninterlaced video lines of red, green and blue analog signals R_{2x}, G_{2x}, B_{2x}. The information contained in red, green and blue analog video signals are displayed on the picture tube screen of the television receiver that generates a progressively scanned raster.

FIGURE 2 illustrates a specific embodiment, in accordance with an aspect of the invention, of a progressive scan speed-up processor PSP1 or PSP2 of FIGURE 1. Items in FIGURES 1 and 2 similarly identified function in a similar manner or represent similar quantities.

In accordance with an aspect of the invention, vertical detail information from interlaced luminance signal Y is extracted by speed-up processor PSP of FIGURE 2 in order to generate vertical peaking signals of opposing polarities in alternate time compressed lines of display video. Interlaced luminance signal Y of FIGURE 2 is coupled to a low pass filter 50 that removes the high frequency content of the luminance signal:

To regenerate a vertical detail luminance signal, a line combing operation is performed on the output of low pass filter 50. The output of low pass filter 50 is coupled via a latch 51 to a memory unit 60a of a memory bank 60. Memory unit 60a serves as a 1-H delay. Digital samples are developed at the output of low pass filter 50 at the $4f_{sc}$ rate. To reduce tie memory size of 1-H delay 60a, latch 51 passes to the input of delay 60a every fourth digital sample developed at the output of low pass filter 50. With low pass filter 50 being clocked at the $4f_{sc}$ rate, latch 51 and 1-H delay 60a are clocked at one quarter that rate, i.e. are clocked at the f_{sc} rate. No loss of resolution occurs by reducing the sample rate to the f_{sc} rate because only relatively low frequency vertical detail information is being processed. At the f_{sc} clock rate, the size of memory unit 60a required to store one video line of digital samples is 227 bytes or 1 RMU.

The delayed digital samples at the output of 1-H delay 60a are coupled to the negative input of a subtractor 53. Undelayed digital samples at the input of delay 52 are directly coupled to the positive input of subtractor 53. A reconstructed luminance signal Y''_D is developed at the output of subtractor 53 that contains vertical detail information that is substantially the same as the vertical

detail information contained in the signal Y_D of interlaced luminance signal Y.

Reconstructed vertical detail signal Y''_D is coupled to a vertical peaking circuit 57 to generate from the vertical detail a vertical peaking signal Y''_P. The vertical detail signal Y''_D, and the vertical peaking signal Y''_P are added in an adder 58 to generate a peaked vertical detail signal Y''_V that contains enhanced vertical detail information having peaked vertical transitions. Since vertical peaking is scaled as a function of contrast, vertical peaking stage 37 receives a contrast control signal to control the amount of peaking provided. A vertical peaking circuit responsive to contrast setting is described in copending U.S. Patent Application Serial Number 599,536, by R. T. Fling, entitled, "PIECE WISE LINEAR DIGITAL SIGNAL PROCESSOR FOR DIGITAL VIDEO VERTICAL DETAIL PROCESSING", herein incorporated by reference, a copy being filed herewith.

Digital samples of the enhanced vertical detail signal Y''_V, developed at the f_{sc} rate, are coupled to a memory unit 60b of memory block 60. Memory unit 60b functions as a speed-up or time compression stage to time compress the signal Y''_V into a time compressed, double-line rate signal Y''_{2xV} with digital samples thereof being developed at the $2f_{sc}$ rate. To write into memory digital samples of the signal Y''_V, control terminal R/ $\overline{W}$ is low during one line time, $1/f_H$. During this interval, sampling clock terminal CK1 is enabled and digital samples of the signal Y''_V are written into memory by the clock signal f_{sc}.ck. During the next line time, control terminal R/ $\overline{W}$ is high, to enable sampling clock terminal CK2. Stored samples of the signal Y''_V are read out of memory at twice the write rate by the clock signal $2f_{sc}$.ck.

The time compressed enhanced vertical detail signal Y''_{2xV} contains vertical peaking information that is to be displayed on the picture tube screen of the television receiver in pairs of noninterlaced display lines that have the peaking information opposing in polarity in alternate lines. To develop a vertical detail signal with peaking information of opposing polarities, the time compressed enhanced vertical detail signal Y''_{2xV} is directly coupled to an input port D2 of a multiplexer MUX 2 and is coupled to an input port D1 of the multiplexer via an inverter 59. The clock signal f_H.ck, developed at control clock terminal CKM, is coupled to the select terminal of MUX 2.

During the time period of a compressed video line when the high state of the clock signal f_H.ck is developed at select terminal SEL, the signal Y''_{2xV-} is transferred from input port D1 to output port D3 of MUX 2. During the next time compressed line period when select terminal SEL is low, then the signal Y''_{2xV+} is transferred from input port D2 to output port D3. The signal Y_{2xV-} is the signal Y''_{2xV} after inversion, and the signal Y_{2xV+} is the signal Y''_{2xV} without inversion.

The signal Y''_{2xV-+} generated at output port D3 comprises time compressed lines of the signal Y''_{2xV-} containing vertical peaking of one polarity alternating with time compressed lines of the signal Y_{2xV+} containing vertical peaking of the opposite polarity. This enhanced vertical detail information is combined with the high frequency luminance information to develop the restored luminance signal appearing at the luminance output signal line 70Y of speed-up processor PSP.

To generate the high frequency luminance information that is combined with the enhanced vertical detail signal Y''_{2xV-+}, vertical detail information in interlaced luminance signal Y is deleted. To accomplish the deletion, luminance signal Y is coupled to the positive input of a subtractor 55 via a delay 56, which compensates for processing delays in the vertical detail extraction and speed-up channel. The extracted vertical detail signal Y''_D is coupled to the negative input of subtractor 55 via a linear interpolator 54.

Linear interpolator 54 generates four digital samples at its output for every one digital sample coupled to its input. A straight line interpolation is used, to generate digital samples at the output of the interpolator that contains three interpolated samples between two successive real samples. Thus, the sample rate of the interpolated vertical detail signal Y''_{ID} at the output of interpolator 54 is $4f_{sc}$, four times that of the signal Y''_D.

Vertical detail signal Y''_{ID} is subtracted from luminance signal Y to remove low frequency luminance information. A high frequency luminance signal Y''_{cm} is developed at the output of subtractor 55. Luminance signal Y''_{cm} contains substantially the same high frequency information as that contained in luminance signal Y_{cm} that is part of interlaced luminance signal Y.

Digital samples of high frequency luminance signal Y''_{cm}, developed at the $4f_{sc}$ rate, are coupled to a memory unit 60c of memory bank 60. Memory unit 60c functions as a speed-up or time compression stage for the luminance signal Y''_{cm} to generate two time compressed lines of a high frequency luminance signal Y''_{2xcm} for each line of luminance signal Y''_{cm}.

Digital samples of luminance signal Y''_{cm} are written into memory during one line period, $1/f_H$, when control terminal R/ $\overline{W}$ is low, enabling sampling clock terminal CK3 to clock samples into memory at the $4f_{sc}$ rate. Digital samples of the time compressed, high frequency luminance signal Y''_{2xcm} are developed during the next $1/f_H$ line period, when control terminal R/ $\overline{W}$ is high, enabling sampling clock terminal CK4 to clock out of

memory unit 60c, digital samples at an $8f_{sc}$ rate.

Because high frequency luminance information is being stored in memory unit 60c, one video line of high frequency luminance information contains 910 digital samples or bytes, equal to a memory size of approximately 4 RMU.

To restore the enhanced vertical detail information into the time compressed, high frequency luminance signal Y''_{2xcm}, the vertical detail signal $Y''_{2xV.+}$ is coupled to an input of an adder 61 via an interpolator 62. Interpolator 62 is a linear interpolator similar in design to interpolator 54 except that the input sample rate is $2f_{sc}$ and the output sample rate is $8f_{sc}$.

A time compressed, enhanced vertical detail signal, Y''_{2xV}, at a sampling rate of $8f_{sc}$, is developed at the output of interpolator 62 and coupled to adder 61. Time compressed high frequency luminance signal Y''_{2xcm} is coupled to the other input of adder 61 to generate on luminance output signal line 70Y of speed-up processor PSP, a time compressed luminance signal containing enhanced vertical detail information with vertical peaking of opposite polarities in alternate time compressed lines of display video.

To generate the time, compressed I and Q signals on output signal lines 60I and 60Q of progressive scan speed-up processor PSP, digital samples of the I and Q signals, each developed at the f_{sc} rate, are coupled to respective memory units 60d and 60e. Memory units 60d and 60e function in a manner identical to that of unit 60b to provide speed-up or time compression of the I and Q signals to generate the time compressed, double line rate signals I''_{2x} and Q''_{2x}. Because the I and Q signals contain relatively low frequency information, less memory is required for memory units 60d and 60e than for memory unit 60c. To store one video line of the I or Q signals requires 227 bytes of storage or 1 RMU of memory for each of memory units 60d and 60e.

By inserting the enhanced vertical detail information to the high frequency luminance information, after the signals containing these types of information are time compressed rather than before the signals are time compressed, only memory unit 60c, that stores high frequency luminance information, requires relatively large amounts of storage. Furthermore, by providing for parallel operation of two speed-up processors, PSP1 and PSP2, not only the generation of an enhanced luminance signal containing vertical peaking of opposite polarities in alternate time compressed lines of video, but also the actual time compression of the luminance signal are accomplished using integrated circuit building blocks that are substantially alike and that require
relatively little memory storage capacity.

Claims

1. A progressive scan video processor, comprising:

   means (IVPU) for generating a line-interlaced luminance signal ($Y = Ycm + Y_D$) which has been separated from chrominance video and which contains vertical detail information (Y_D). said interlaced luminance signal being generated at a given line rate (f_H);

   characterized by:

   means (60a,53,57) for generating a peaked vertical detail signal ($Y''_D + Y''_P$) that contains vertical detail information (Y''_D) derived from said luminance signal; and

   means (58,60b,55,60c) including a first time compression section (60c) responsive to said interlaced luminance signal, and a second time compression section (60b) responsive to said peaked vertical detail signal, for generating a time compressed, non-interlaced, enhanced luminance signal that contains vertical detail information with peaking, said time compressed luminance signal being generated at a second, faster, line rate ($2f_H$) that is a multiple Of said given rate.

2. A video processor according to claim 1 including means (59,MUX2) responsive to said peaked vertical detail signal ($Y''_D + Y''_P$) for generating a version of said peaked vertical detail signal ($Y''_{2\ xV+.}$) alternating in polarity at said second line rate and means (61) for combining said version of said peaked vertical detail signal with said interlaced luminance signal (Y''_{CM}) in said multiple line rate time compressed luminance signal.

3. A video processor according to any preceding claim wherein said interlaced luminance signal is a sampled signal having a first sampling rate ($4f_{sc}$), said vertical detail and peaking signals have a sampling rate which is a submultiple (f_{sc}) of said first sampling rate, and interpolating means (62) is included for generating, from said submultiple sampling rate signals, interpolated signals at said first sampling rate for combination with said sampled luminance signal.

4. A video processor according to any preceding claim including two time compression stages (PSP1, PSP2) each operable in response to said luminance and peaked vertical detail signals for producing said time compressed luminance signal, said two compression stages being operative alternately at said given line rate in producing successive pairs of com-

memory unit 60c, digital samples at an $8f_{sc}$ rate.

Because high frequency luminance information is being stored in memory unit 60c, one video line of high frequency luminance information contains 910 digital samples or bytes, equal to a memory size of approximately 4 RMU.

To restore the enhanced vertical detail information into the time compressed, high frequency luminance signal Y''_{2xcm}, the vertical detail signal Y''_{2xV+} is coupled to an input of an adder 61 via an interpolator 62. Interpolator 62 is a linear interpolator similar in design to interpolator 54 except that the input sample rate is $2f_{sc}$ and the output sample rate is $8f_{sc}$.

A time compressed, enhanced vertical detail signal, Y''_{2xV}, at a sampling rate of $8f_{sc}$, is developed at the output of interpolator 62 and coupled to adder 61. Time compressed high frequency luminance signal Y''_{2xcm} is coupled to the other input of adder 61 to generate on luminance output signal line 70Y of speed-up processor PSP, a time compressed luminance signal containing enhanced vertical detail information with vertical peaking of opposite polarities in alternate time compressed lines of display video.

To generate the time, compressed I and Q signals on output signal lines 60I and 60Q of progressive scan speed-up processor PSP, digital samples of the I and Q signals, each developed at the f_{sc} rate, are coupled to respective memory units 60d and 60e. Memory units 60d and 60e function in a manner identical to that of unit 60b to provide speed-up or time compression of the I and Q signals to generate the time compressed, double line rate signals I''_{2x} and Q''_{2x}. Because the I and Q signals contain relatively low frequency information, less memory is required for memory units 60d and 60e than for memory unit 60c. To store one video line of the I or Q signals requires 227 bytes of storage or 1 RMU of memory for each of memory units 60d and 60e.

By inserting the enhanced vertical detail information to the high frequency luminance information, after the signals containing these types of information are time compressed rather than before the signals are time compressed, only memory unit 60c, that stores high frequency luminance information, requires relatively large amounts of storage. Furthermore, by providing for parallel operation of two speed-up processors, PSP1 and PSP2, not only the generation of an enhanced luminance signal containing vertical peaking of opposite polarities in alternate time compressed lines of video, but also the actual time compression of the luminance signal are accomplished using integrated circuit building blocks that are substantially alike and that require
relatively little memory storage capacity.

Claims

1. A progressive scan video processor, comprising:

   means (IVPU) for generating a line-interlaced luminance signal ($Y = Ycm + Y_D$) which has been separated from chrominance video and which contains vertical detail information (Y_D), said interlaced luminance signal being generated at a given line rate (f_H);

   characterized by:

   means (60a,53,57) for generating a peaked vertical detail signal ($Y''_D + Y''_P$) that contains vertical detail information (Y''_D) derived from said luminance signal; and

   means (58,60b,55,60c) including a first time compression section (60c) responsive to said interlaced luminance signal, and a second time compression section (60b) responsive to said peaked vertical detail signal, for generating a time compressed, non-interlaced, enhanced luminance signal that contains vertical detail information with peaking, said time compressed luminance signal being generated at a second, faster, line rate ($2f_H$) that is a multiple Of said given rate.

2. A video processor according to claim 1 including means (59,MUX2) responsive to said peaked vertical detail signal ($Y''_D + Y''_P$) for generating a version of said peaked vertical detail signal (Y''_{2xV+}) alternating in polarity at said second line rate and means (61) for combining said version of said peaked vertical detail signal with said interlaced luminance signal (Y''_{CM}) in said multiple line rate time compressed luminance signal.

3. A video processor according to any preceding claim wherein said interlaced luminance signal is a sampled signal having a first sampling rate ($4f_{sc}$), said vertical detail and peaking signals have a sampling rate which is a submultiple (f_{sc}) of said first sampling rate, and interpolating means (62) is included for generating, from said submultiple sampling rate signals, interpolated signals at said first sampling rate for combination with said sampled luminance signal.

4. A video processor according to any preceding claim including two time compression stages (PSP1, PSP2) each operable in response to said luminance and peaked vertical detail signals for producing said time compressed luminance signal, said two compression stages being operative alternately at said given line rate in producing successive pairs of com-

pressed lines of said time compressed luminance signal.

5. A video processor according to claim 4, wherein each of said alternately operative compression stages includes also at least one other time compression section (60d,60c) responsive to said chrominance video to generate time compressed color information signals ($I''_{2\,x}$, $Q''_{2\,x}$) at said multiple line rate ($2f_H$).

6. A video processor according to claim 5 including a multiplexer (MUX1) for alternately providing to common signal matrixing means (37), at said given line rate, two time-compressed lines at a time, the time compressed luminance and color information signals provided by said two compression stages.

Revendications

1. Système de traitement de balayage vidéo progressif, comprenant :

un moyen (IVPU) pour produire un signal de luminance à lignes entrelacées ($Y = Ycm + Y_D$) qui a été séparé du signal vidéo de chrominance et qui contient l'information de détail vertical (Y_D), ledit signal entrelacé de luminance étant produit à une fréquence de lignes donnée (f_H) ;

caractérisé par :

un moyen (60a, 53,57) pour produire un signal de détail vertical accentué ($Y''_D + Y''_P$) qui contient l'information de détail vertical (Y_D) dérivée dudit signal de luminance ; et

un moyen (58, 60b, 55, 60c) comprenant une première section de compression dans le temps (60c) sensible audit signal entrelacé de luminance et une seconde section de compression dans le temps (60b) sensible audit signal accentué de détail vertical pour produire un signal amélioré de luminance, non entrelacé, comprimé dans le temps, qui contient l'information de détail vertical avec accentuation, ledit signal de luminance comprimé dans le temps étant produit a une seconde fréquence de lignes plus rapide ($2f_H$) qui est un multiple de ladite fréquence donnée.

2. Système de traitement vidéo selon la revendication 1, comprenant un moyen (59, MUX2) répondant audit signal de détail vertical accentué ($Y''_D + Y''_P$) pour produire une version dudit signal de détail vertical accentué ($Y''_{2\,xv+.}$) alternant en polarité à ladite seconde fréquence de lignes et un moyen (61) pour combiner ladite version dudit signal accentué de détail vertical audit signal entrelacé de luminance (Y''_{CM}) dans ledit signal de luminance comprimé dans le temps au multiple de la fréquence de lignes.

3. Système de traitement vidéo selon toute revendication précédente, où ledit signal entrelacé de luminance est un signal échantillonné ayant une première fréquence d'échantillonnage ($4f_{sc}$), lesdits signaux de détail vertical et d'accentuation ayant une fréquence d'échantillonnage qui est un sous-multiple (f_{sc}) de ladite première fréquence d'échantillonnage et un moyen d'interpolation (62) est incorporé pour produire, desdits signaux à une fréquence d'échantillonnage sous-multiple, des signaux interpolés à ladite fréquence d'échantillonnage pour une combinaison avec ledit signal échantillonné de luminance.

4. Système de traitement vidéo selon toute revendication précédente, comprenant deux étages de compression dans le temps (PSP1, PSP2), chacun fonctionnant en réponse auxdits signaux de luminance et de détail vertical accentué pour produire ledit signal de luminance comprimé dans le temps, lesdits deux étages de compression fonctionnant alternativement à ladite fréquence donnée de lignes pour produire des paires successives de lignes comprimées dudit signal de luminance comprimé dans le temps.

5. Système de traitement vidéo selon la revendication 4, où chacun desdits étages de compression fonctionnant alternativement comprend également au moins une autre section de compression dans le temps (60d, 60c) répondant à ladite vidéo de chrominance pour produire des signaux d'information de couleur comprimés dans le temps ($I''_{2\,x}$, $Q''_{2\,x}$) à ladite fréquence de lignes multiple ($2f_H$).

6. Système de traitement vidéo selon la revendication 5, comprenant un multiplexeur (MUX1) pour appliquer alternativement, à un moyen formant matrice commune de signaux (37), à ladite fréquence donnée de lignes, à deux lignes comprimées dans le temps à la fois, les signaux comprimés dans le temps de luminance et d'information de couleur produits par lesdits deux étages de compression.

Ansprüche

1. Progressivabtastungs-Videoprozessor mit

einer Anordnung (IVPU) zum Erzeugen eines zeilenverschachtelten Leuchtdichtesignals

* C L M S *

($Y = Ycm + Y_D$), welches von einem Farbartvideosignal abgetrennt wurde und Vertikaldetailinformation (Y_D) enthält und welches mit einer vorgegebenen Zeilenfrequenz (f_H) erzeugt wird; gekennzeichnet durch:

eine Anordnung (60a, 53, 57) zum Erzeugen eines versteilerten Vertikaldetailsignals ($Y"_D + Y"_P$), welches Vertikaldetailinformation ($Y"_D$) enthält, die aus dem Leuchtdichtesignal gewonnen wurde; und

eine Anordnung (58, 60b, 55, 60c), welche einen ersten Zeitkompressionsabschnitt (60c), der auf das zeilenverschachtelte Leuchtdichtesignal anspricht, und einen zweiten Zeitkompressionsabschnitt (60b), der auf das versteilerte Vertikaldetailsignal anspricht, enthält, um ein zeitlich komprimiertes, nichtzeilenverschachteltes, angehobenes Leuchtdichtesignal zu erzeugen, welches Vertikaldetailinforamtion mit Versteilerung enthält und mit einer zweiten, höheren Zeilenfrequenz ($2F_H$), die ein Vielfaches der vorgegebenen Frequenz ist, erzeugt wird.

2. Videoprozessor nach Anspruch 1, mit einer auf das versteilerte Vertikaldetailsignal ($Y"_D + Y"_P$) ansprechenden Anordnung (59, MUX2) zum Erzeugen einer Version des versteilerten Vertikaldetailsignals ($Y"_{2xv+.}$), deren Polarität mit der zweiten Zeilenfrequenz alterniert, und mit einer Anordnung (61) zum Kombinieren der besagten Version des versteilerten Vertikaldetailsignals mit dem verschachtelten Leuchtdichtesignal ($Y"_{CM}$) in dem mehrfachzeilenfrequenten, zeitlich komprimierten Leuchtdichtesignal.

3. Videoprozessor nach einem der vorhergehenden Ansprüche, bei dem das verschachtelte Leuchtdichtesignal ein abgetastetes Signal ist, welches eine erste Abtastrate ($4f_{sc}$) aufweist, wobei das Vertikaldetailsignal und die versteilerten Signale eine Abtastrate haben, welche ein Untervielfaches (f_{sc}) der ersten Abtastrate ist, und in welchem eine Interpolieranordnung (62) vorgesehen ist, um aus den Signalen mit der untervielfachen Abtastrate interpolierte Signale mit der ersten Abtastrate zur Kombination mit dem abgetasteten Leuchtdichtesignal zu erzeugen.

4. Videoprozessor nach einem der vorhergehenden Ansprüche mit zwei Zeitkomprimierstufen (PSP1, PSP2), die jeweils in Ansprache auf das Leuchtdichtesignal und das versteilerte Vertikaldetailsignal arbeiten, um das zeitkomprimierte Leuchtdichtesignal zu erzeugen, und welche alternierend mit der vorgegebenen Zeilenfrequenz arbeiten, um aufeinander-folgende Paare von komprimierten Zeilen des Leuchtdichtesignals zu erzeugen.

5. Videoprozessor nach Anspruch 4, bei welchem jede der alternierend arbeitenden Kompressionsstufen ausserdem noch mindestens einen anderen Zeitkompressionsabschnitt (60d, 60c), der auf das Farbartvideo anspricht, um zeitkomprimierte Farbinformationssignale ($I"_{2x}$, $Q"_{2x}$) mit der mehrfachen Zeilenfrequenz (2_{fH}) zu erzeugen.

6. Videoprozessor nach Anspruch 5, mit einem Multiplexer (MUX1), der mit der vorgegebenen Zeilenfrequenz gleichzeitig zwei zeitkomprimierte Zeilen der zeitkomprimierten Leucht dichte-und Farbinformationssignale, die durch die beiden Kompressionsstufen geliefert werden, an eine gemeinsame Signalmatrizieranordnung (37) zu liefern.