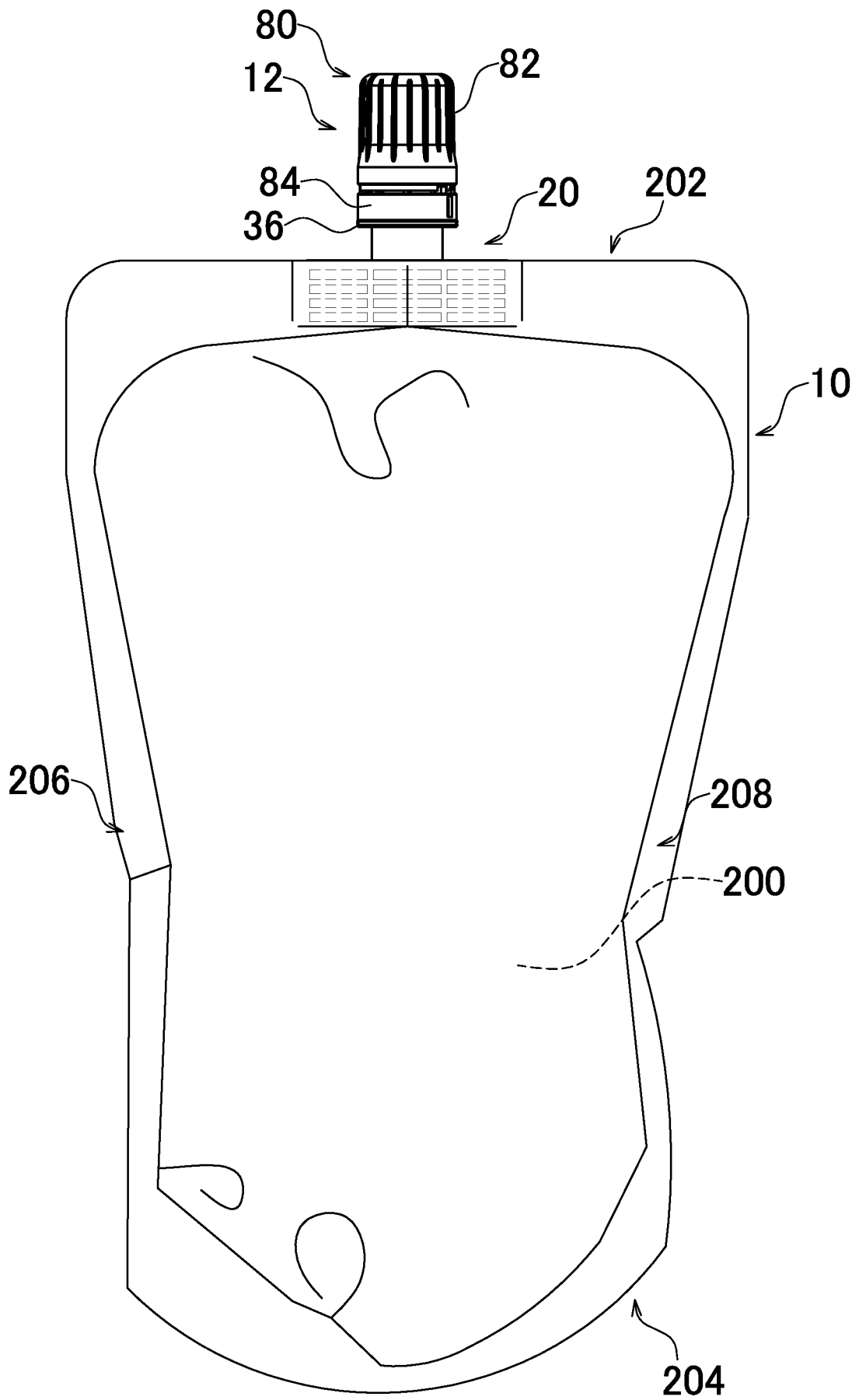


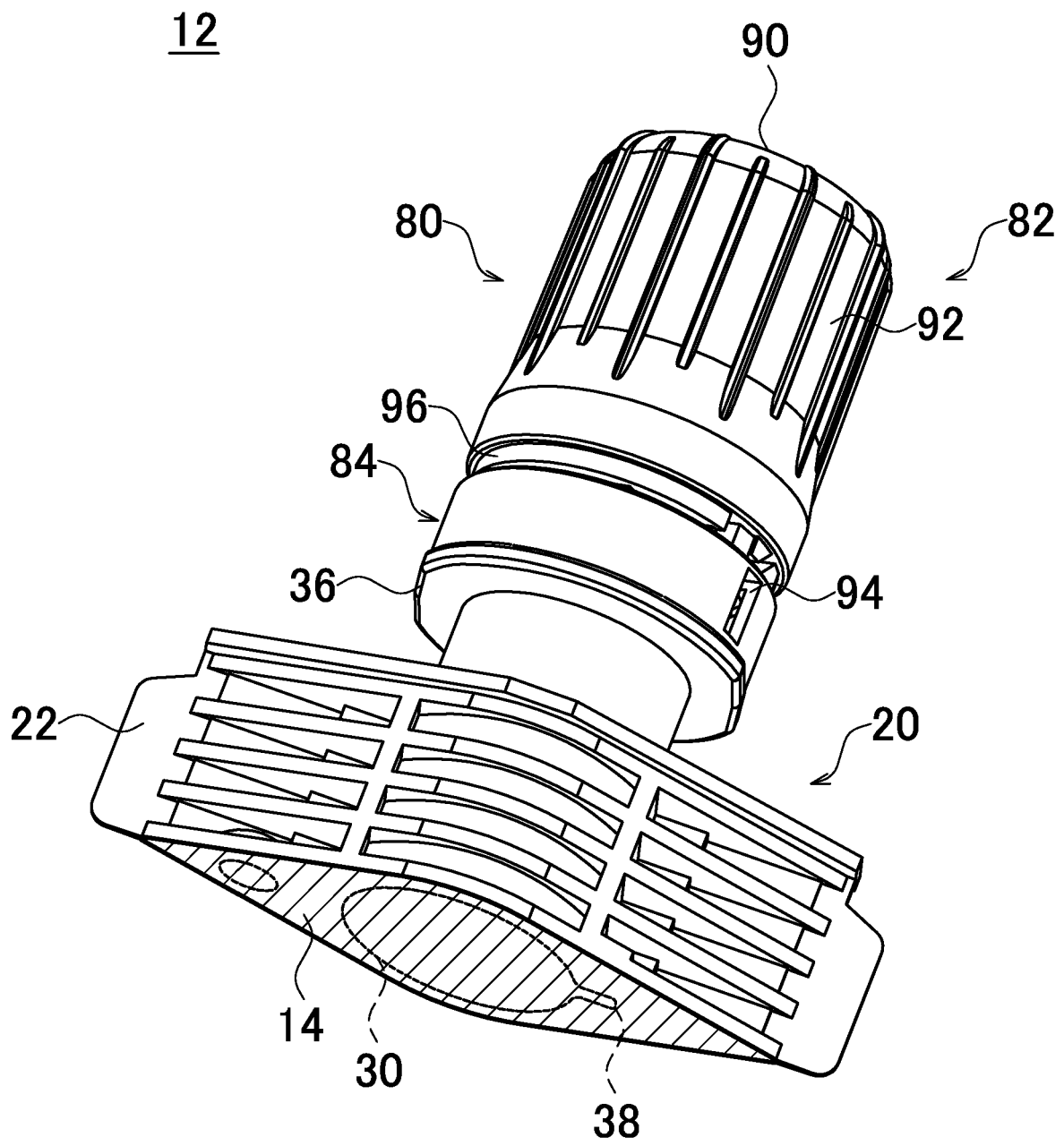
[図1]

図1



[図2]

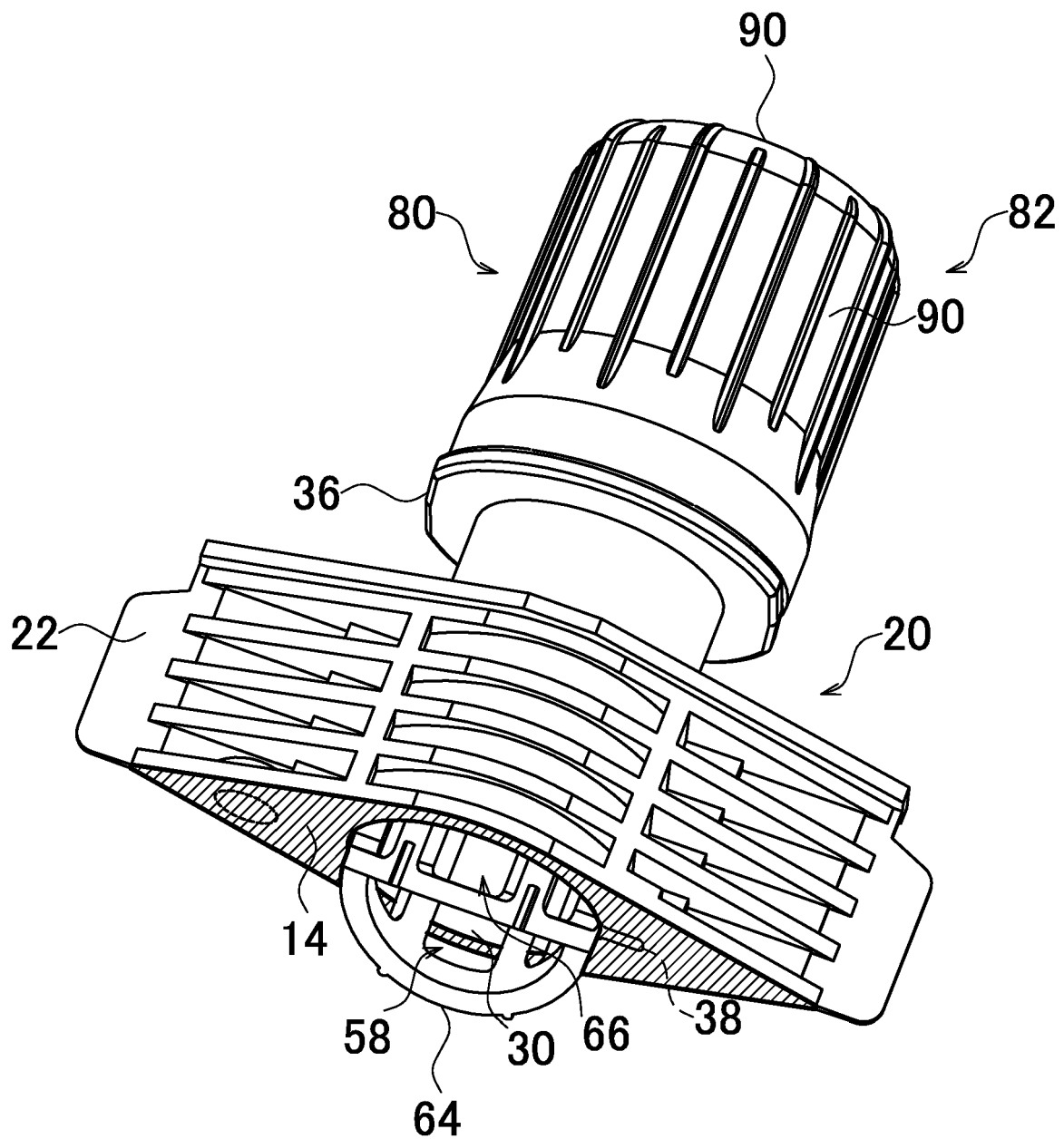
図2



80 { 82 { 90
92
84 { 94
96

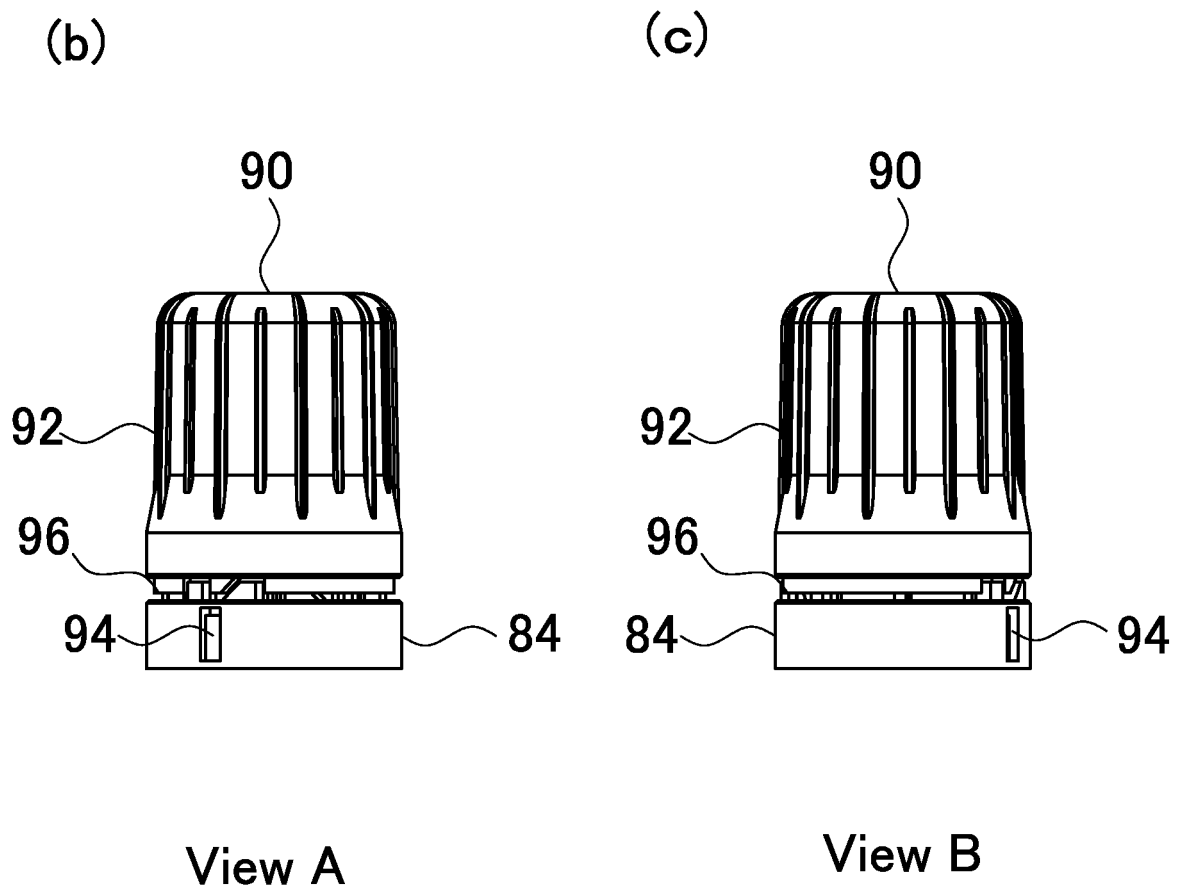
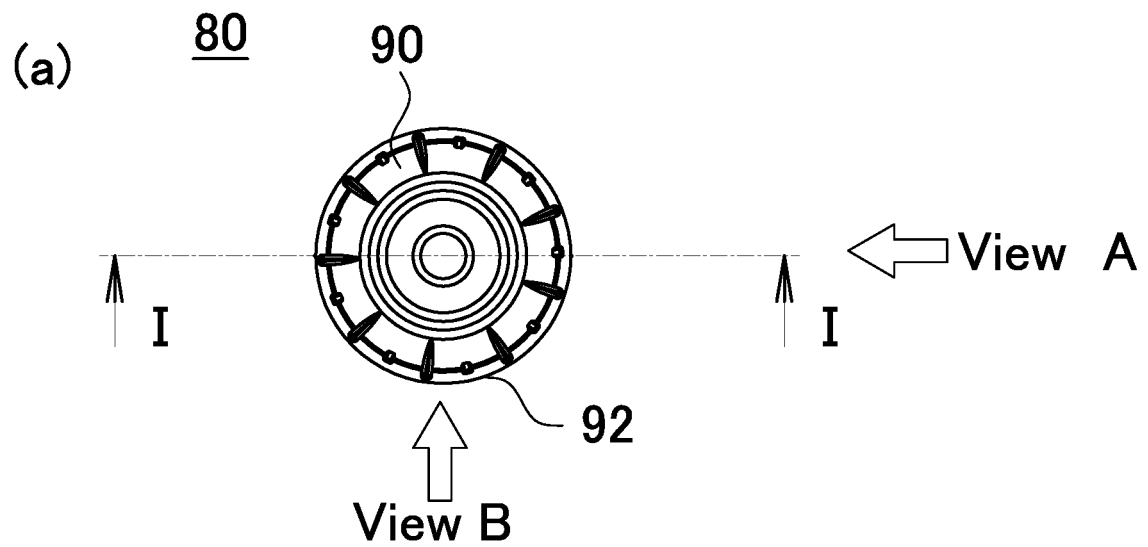
[図3]

図3

12

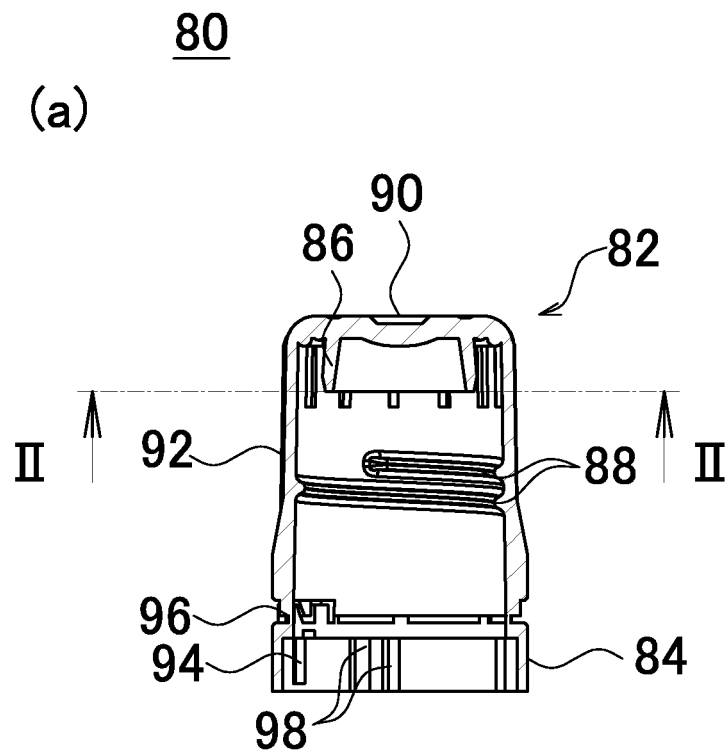
[図4A]

図4A

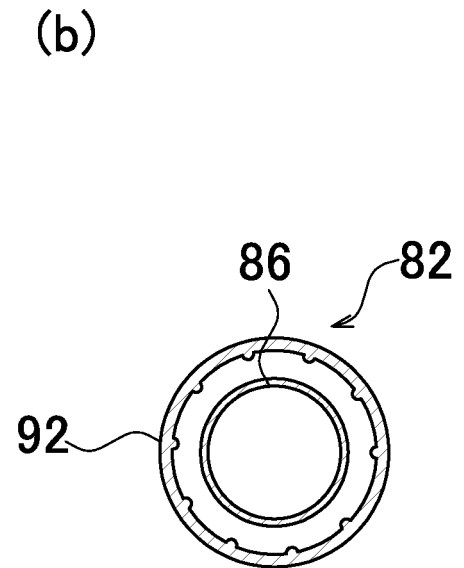


[図4B]

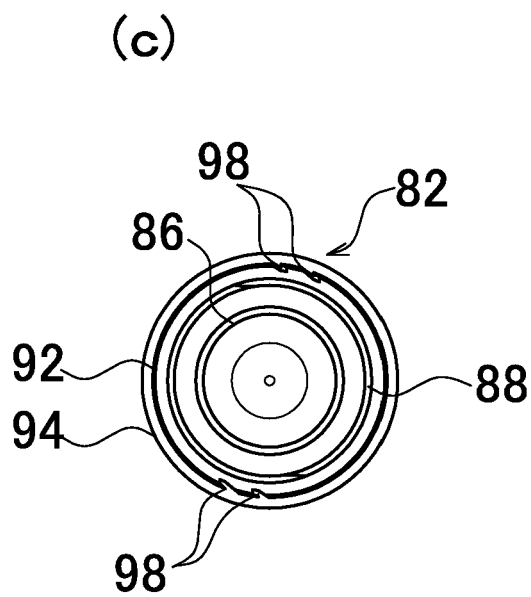
図4B



断面 I - I

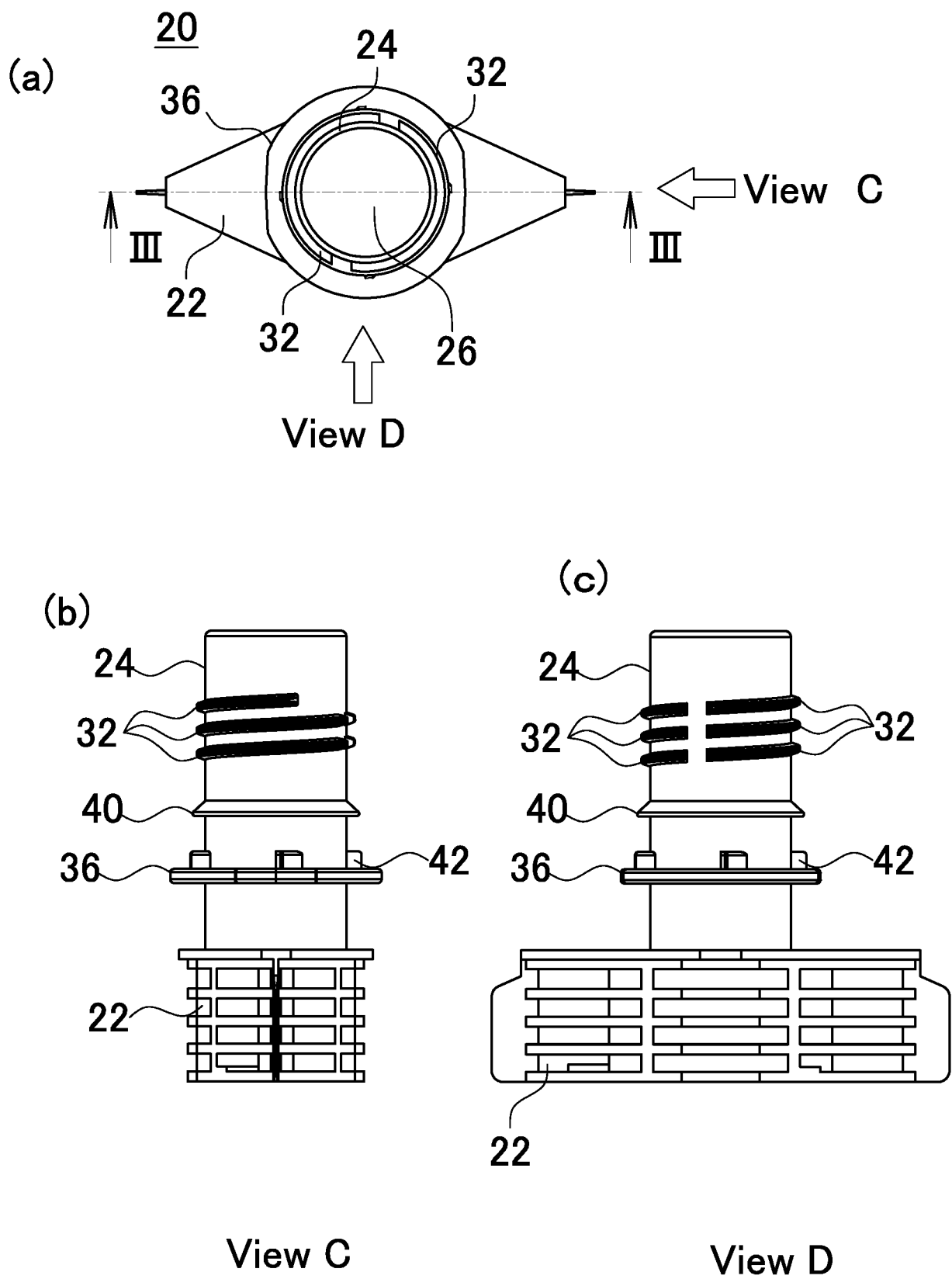


端断面 II - II



[図5A]

図5A

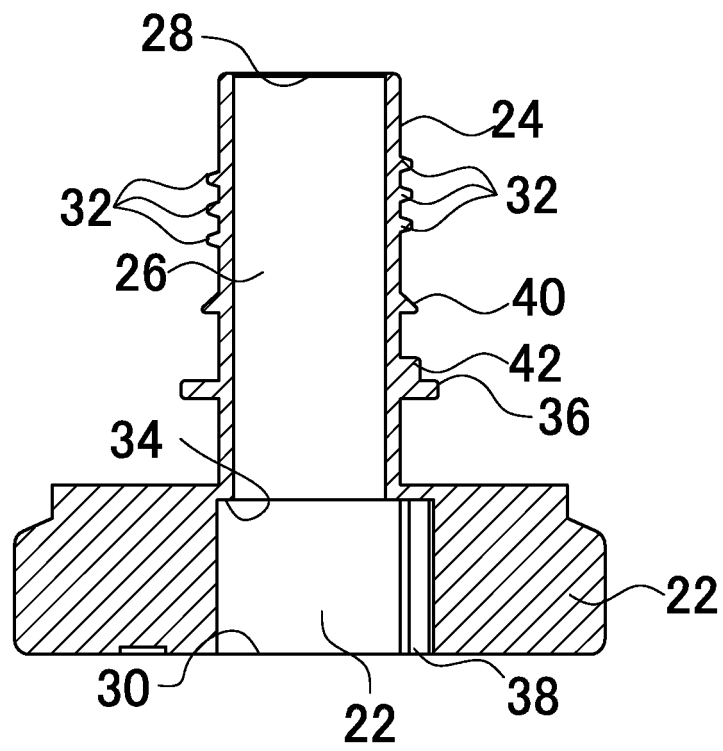


[図5B]

図5B

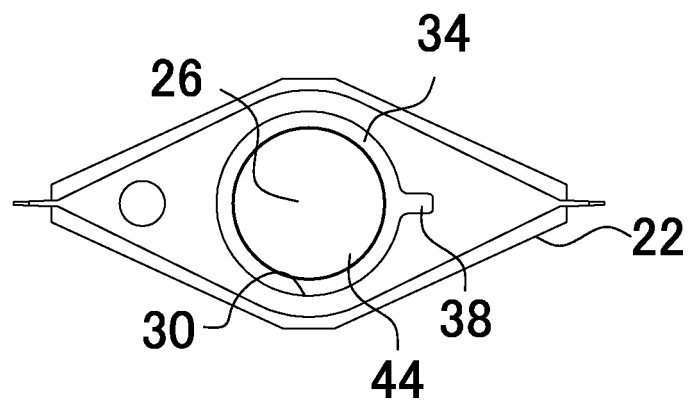
20

(a)



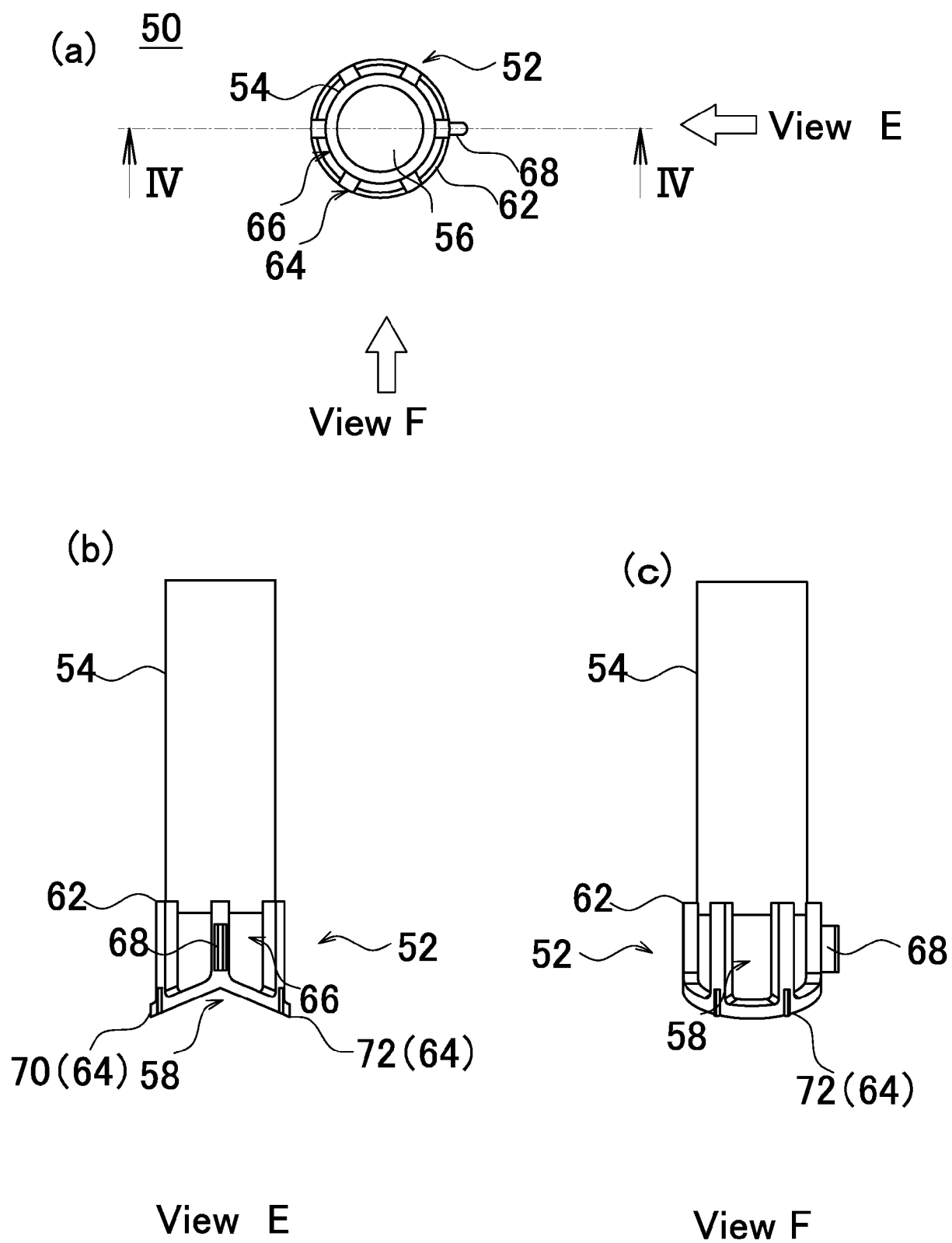
断面Ⅲ-Ⅲ

(b)



[図6A]

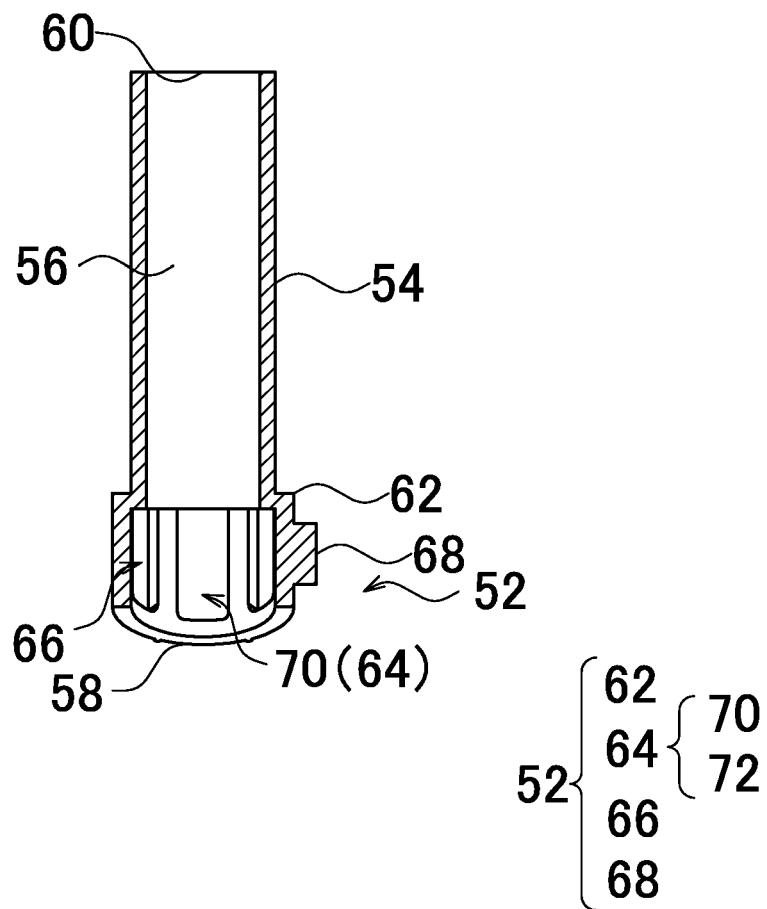
図6A



[図6B]

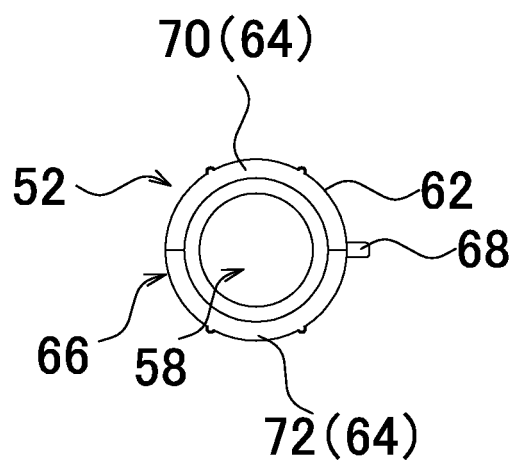
図6B

50
(a)



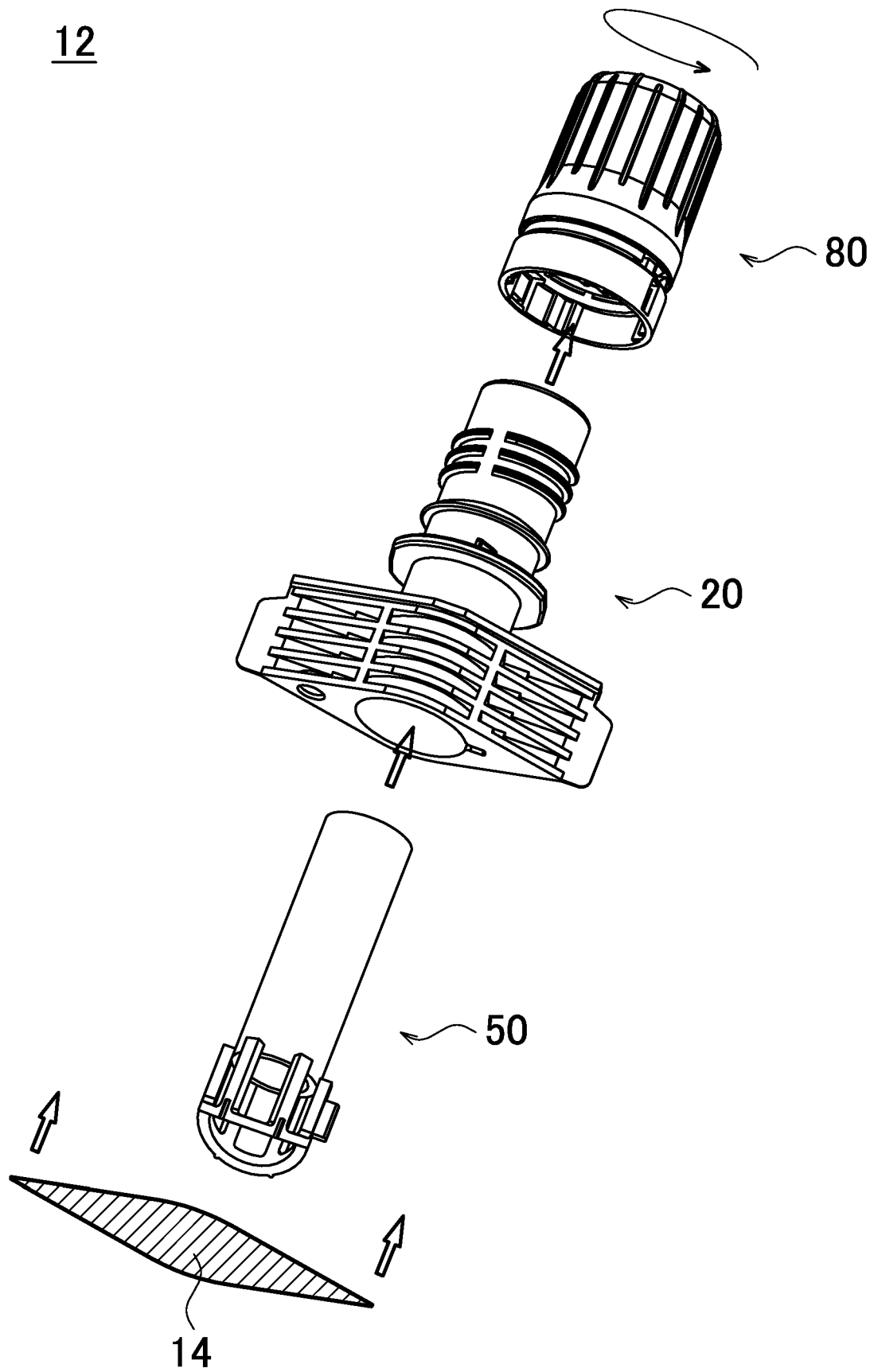
断面IV-IV

(b)



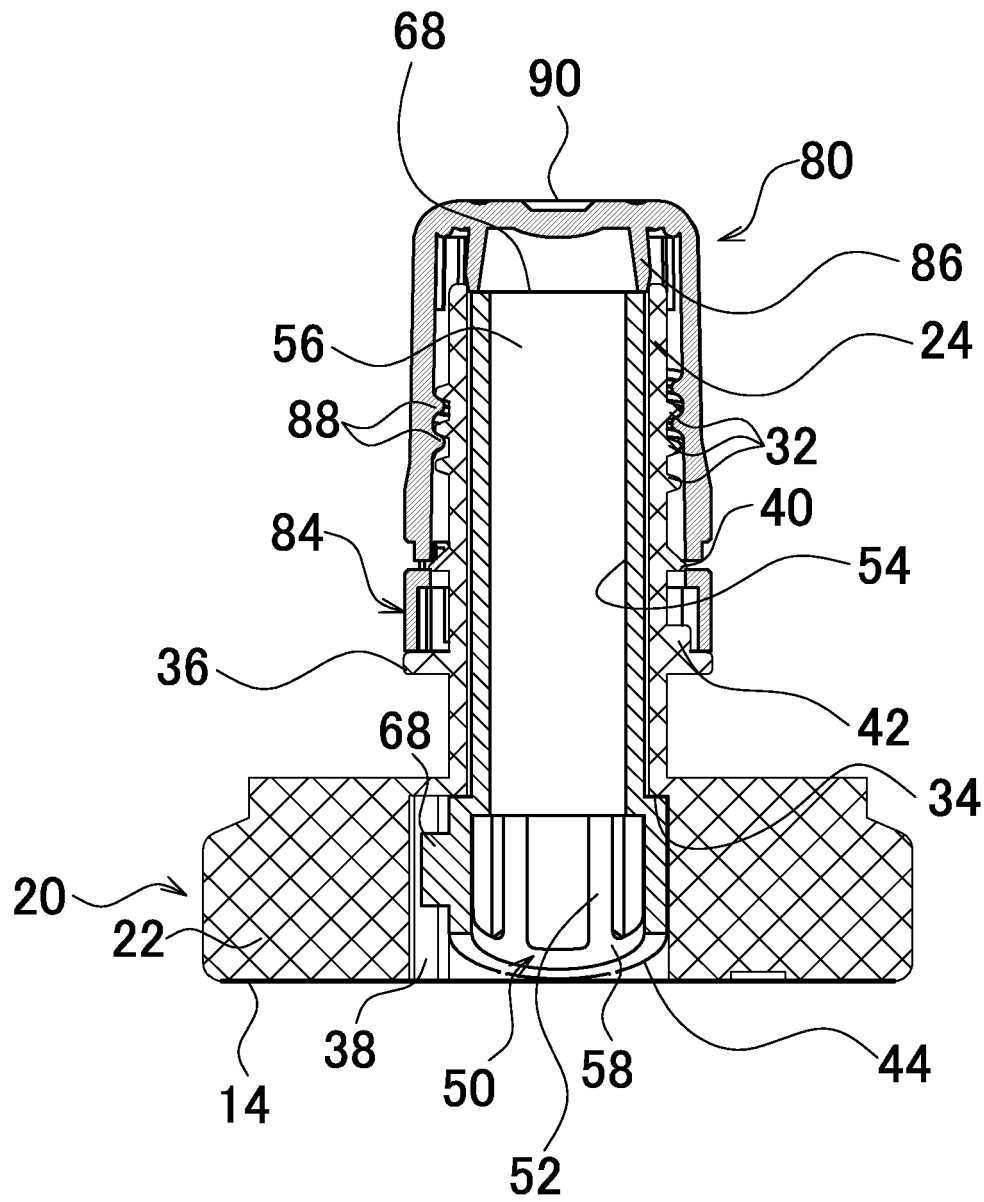
[図7A]

図7A

12

[図7B]

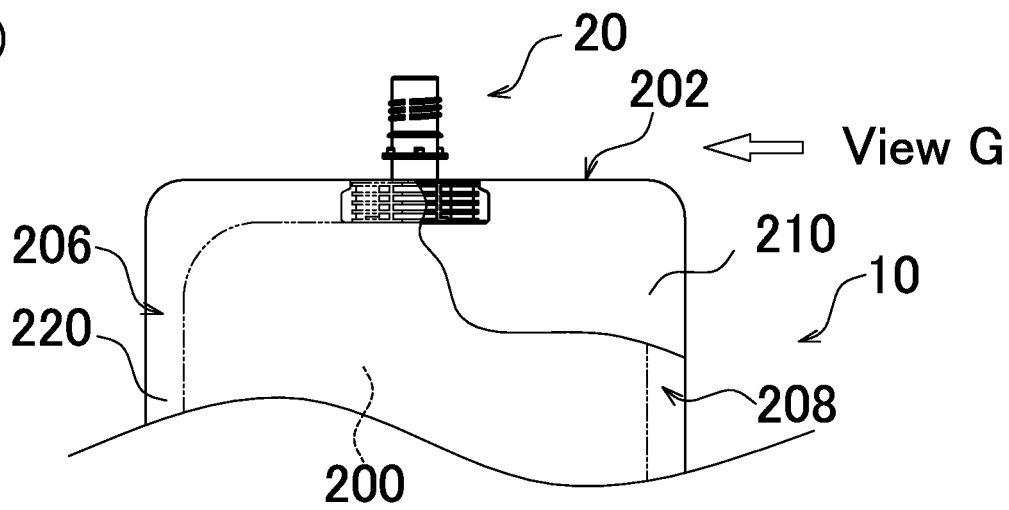
図7B

12

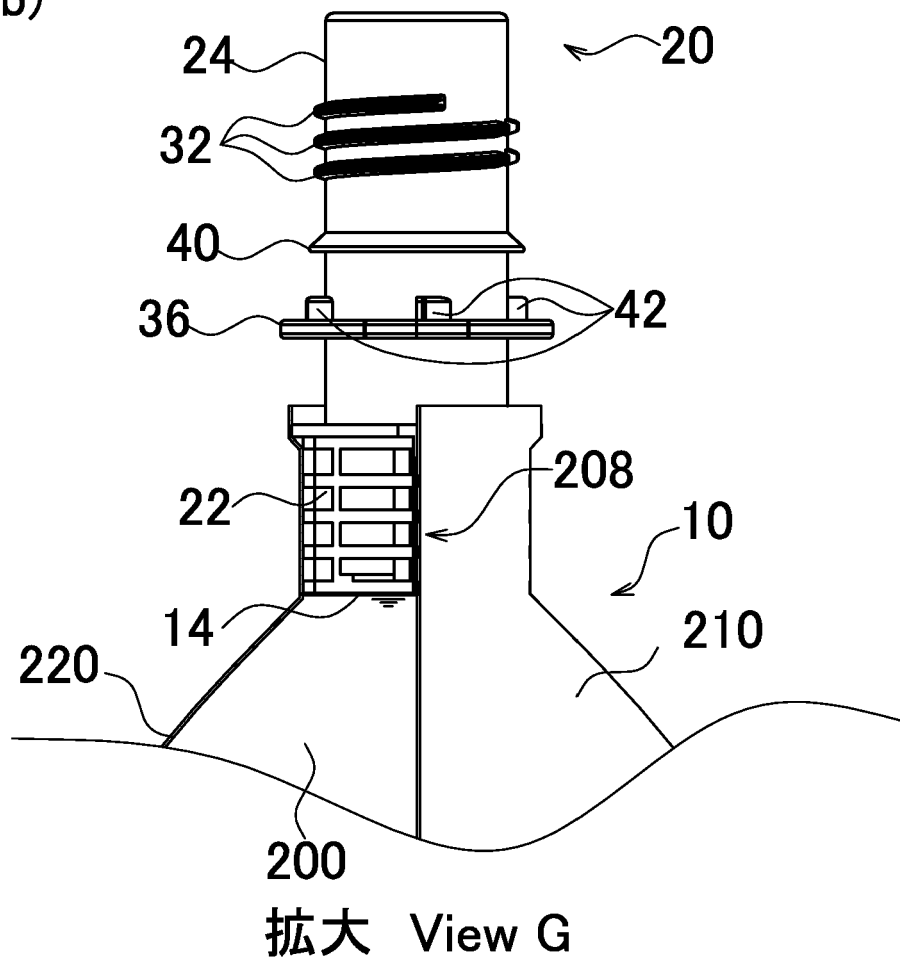
[図8]

図8

(a)



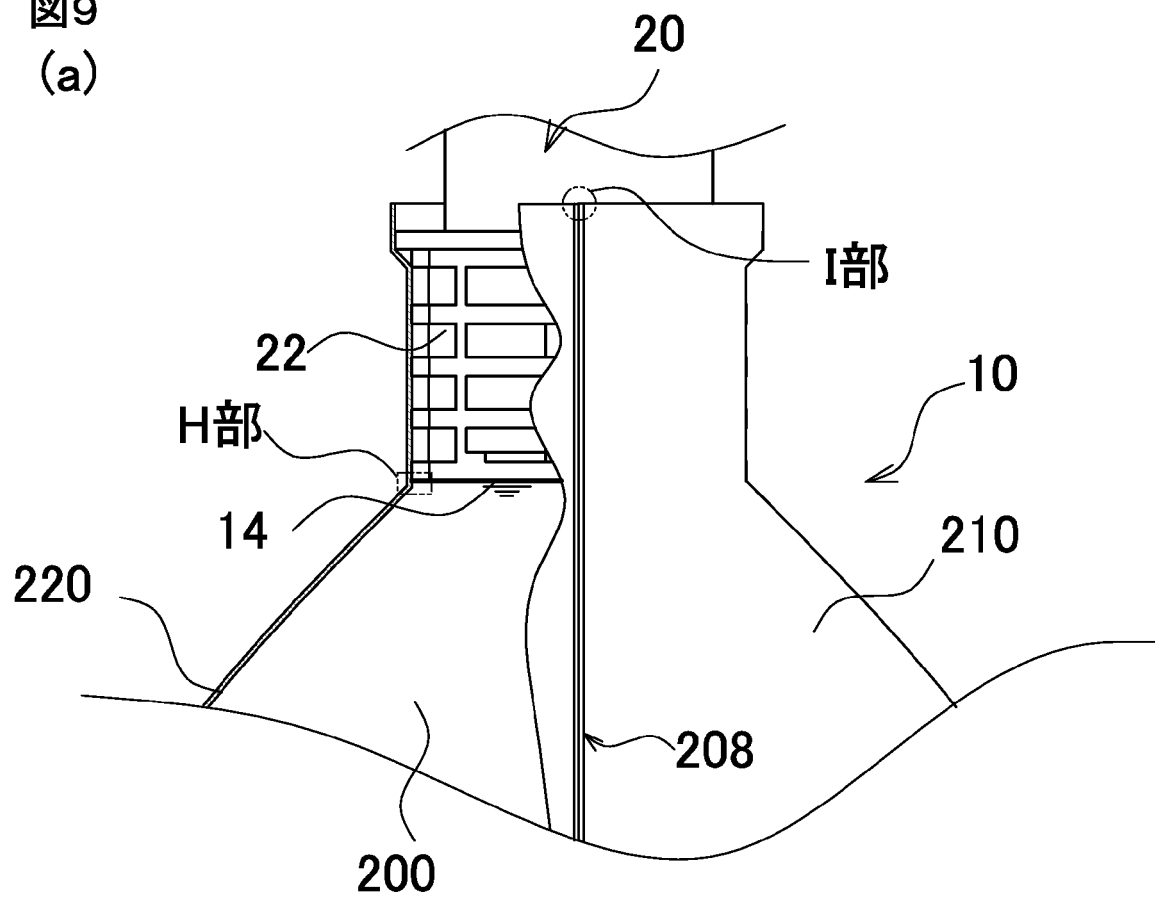
(b)



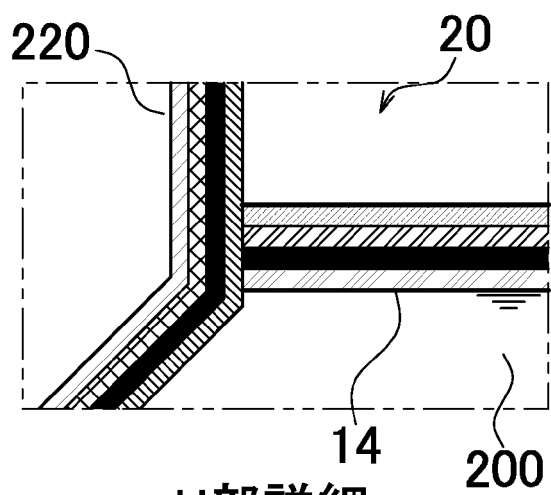
[図9]

図9

(a)

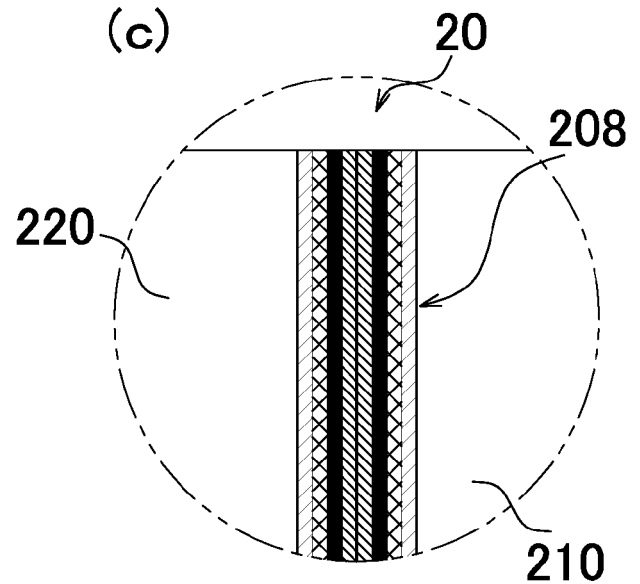


(b)



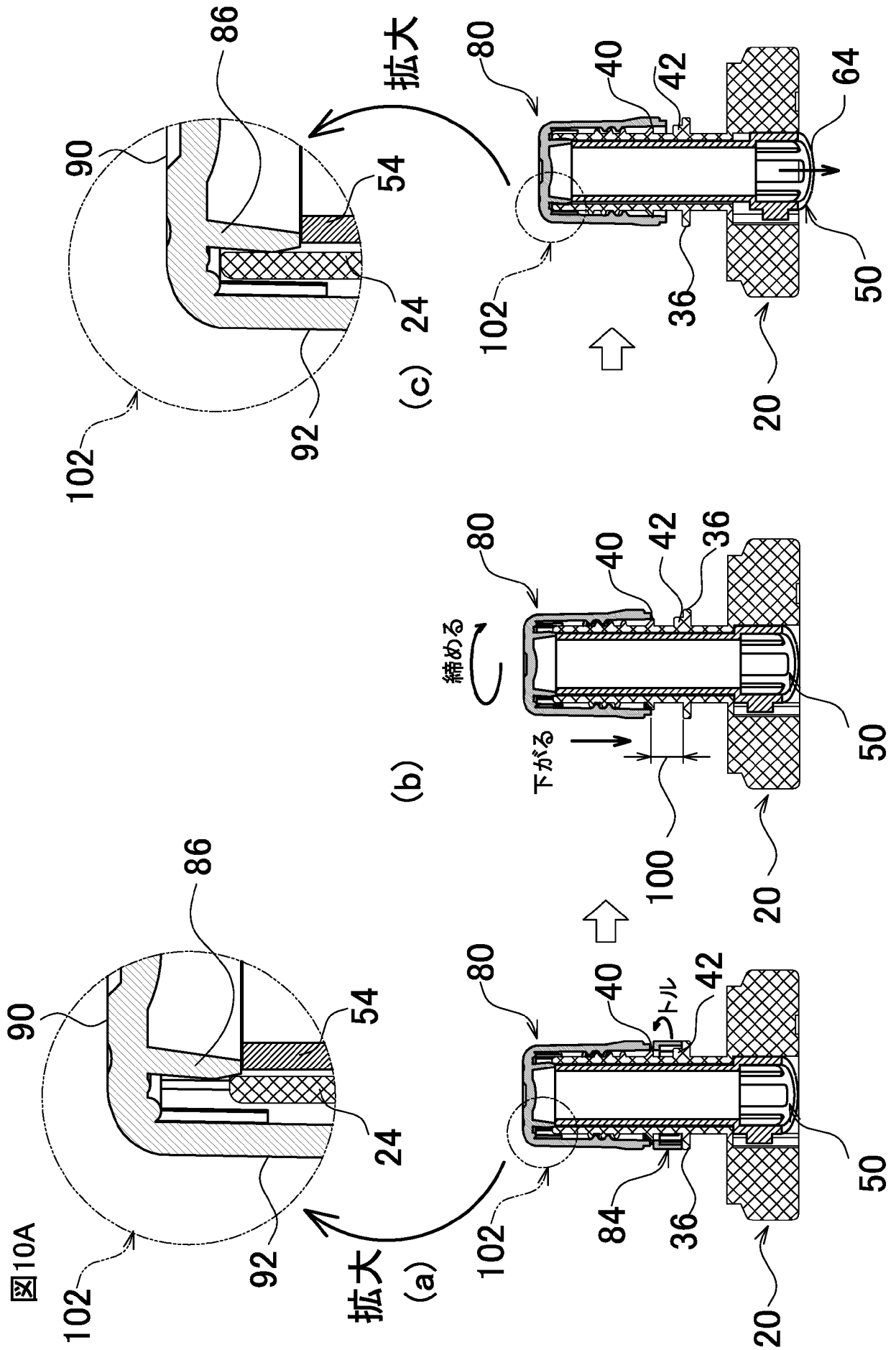
H部詳細

(c)



I部詳細

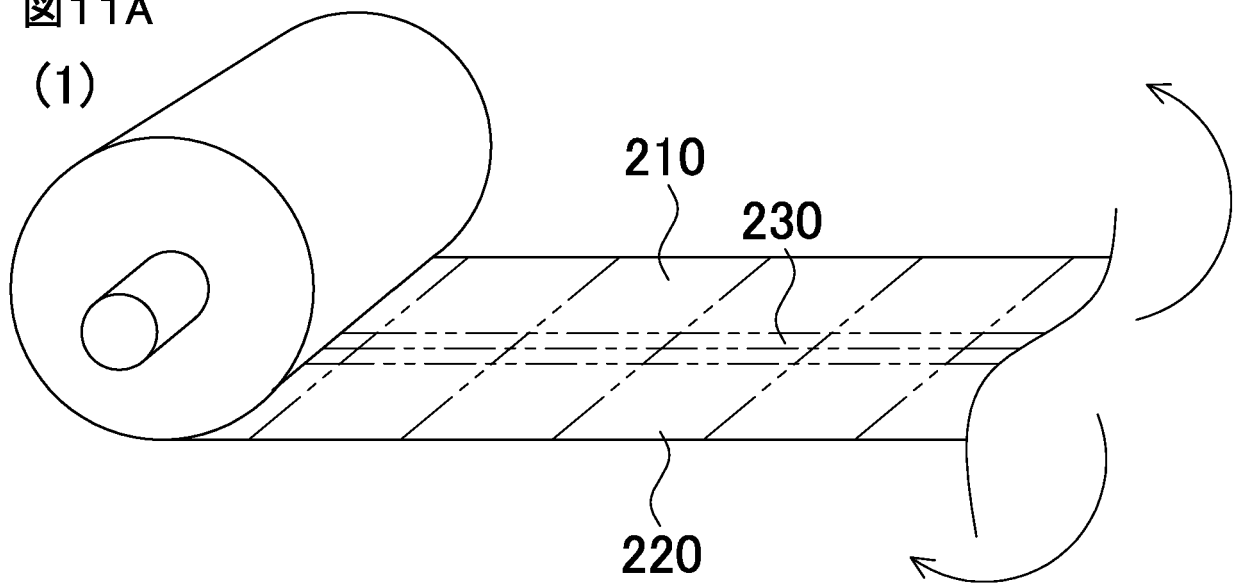
[図10A]



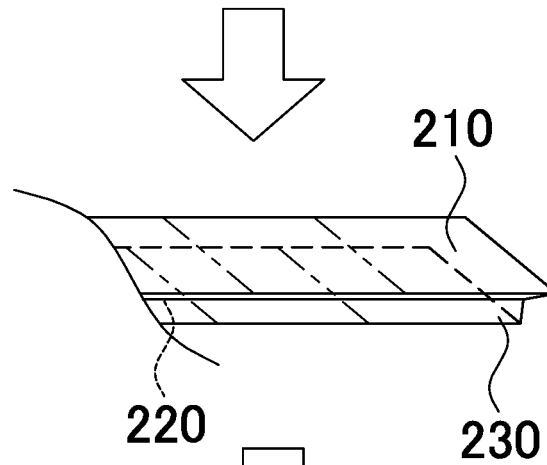
[図11A]

図11A

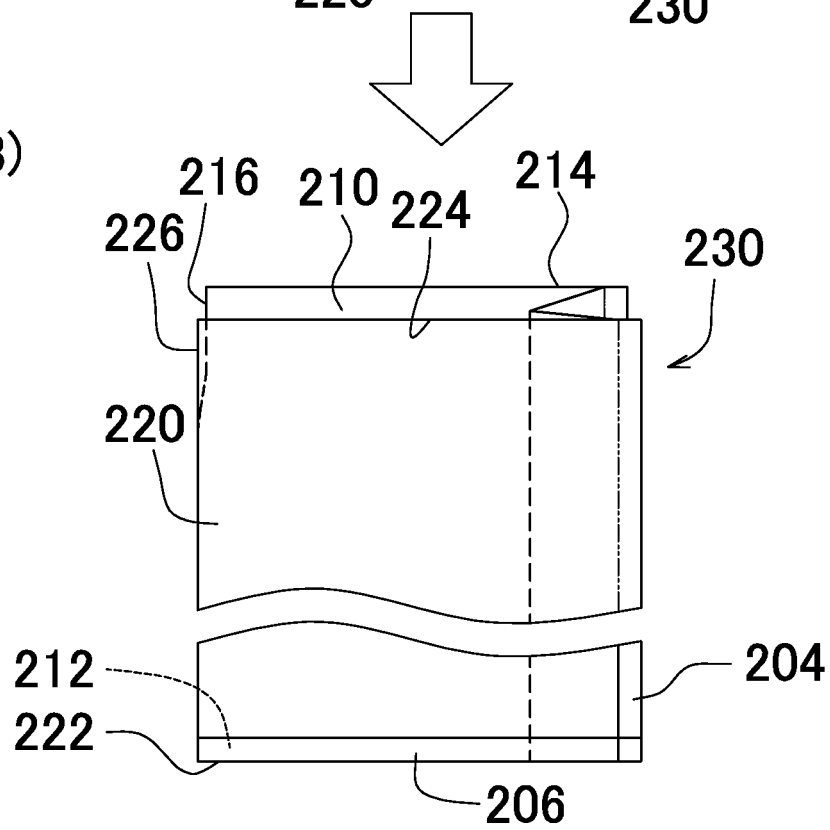
(1)



(2)

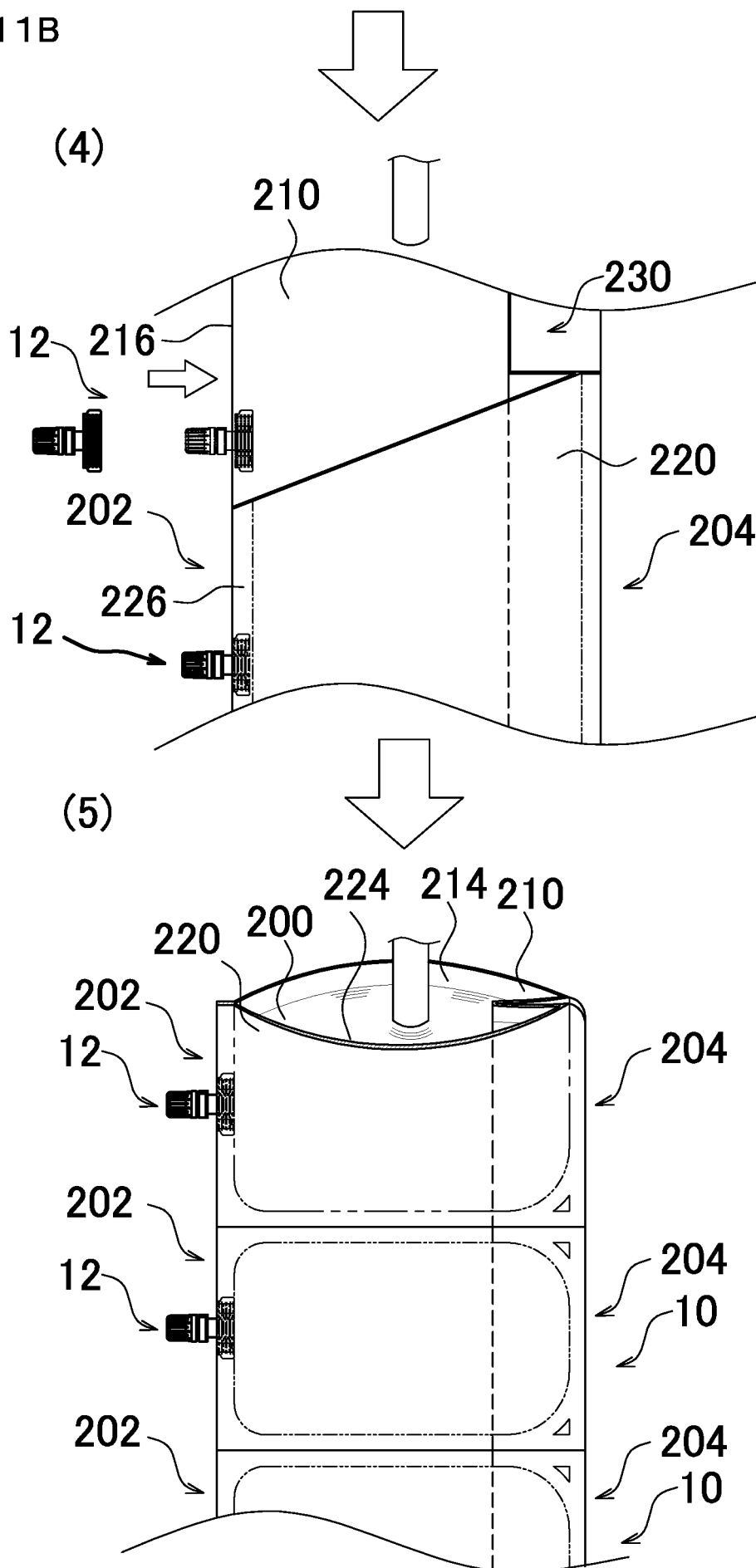


(3)



[図11B]

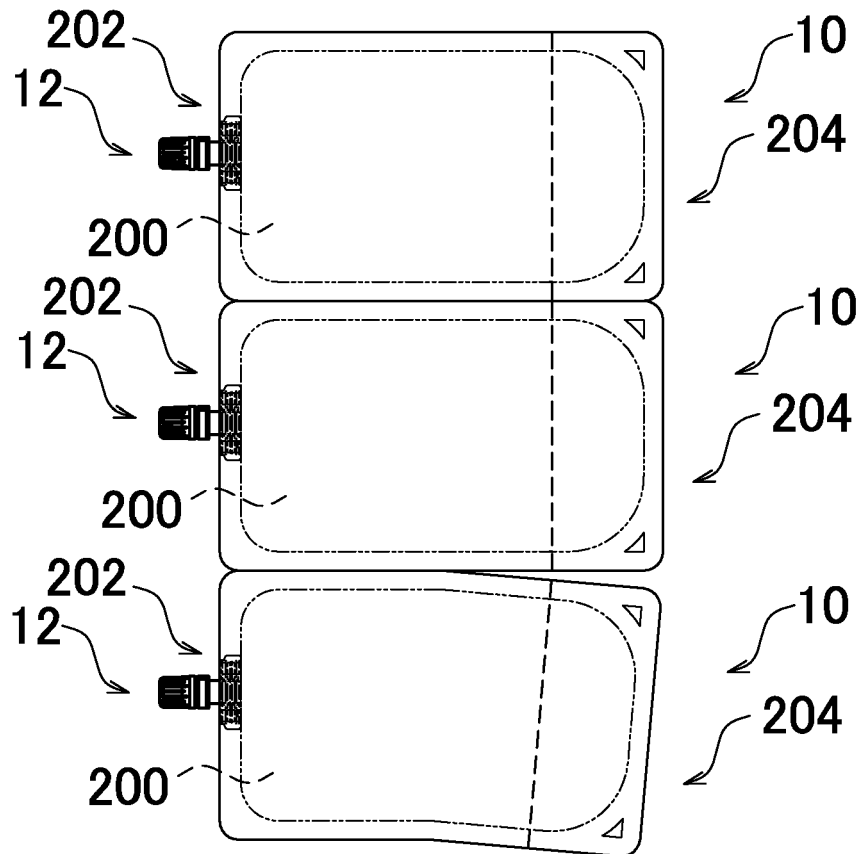
図11B



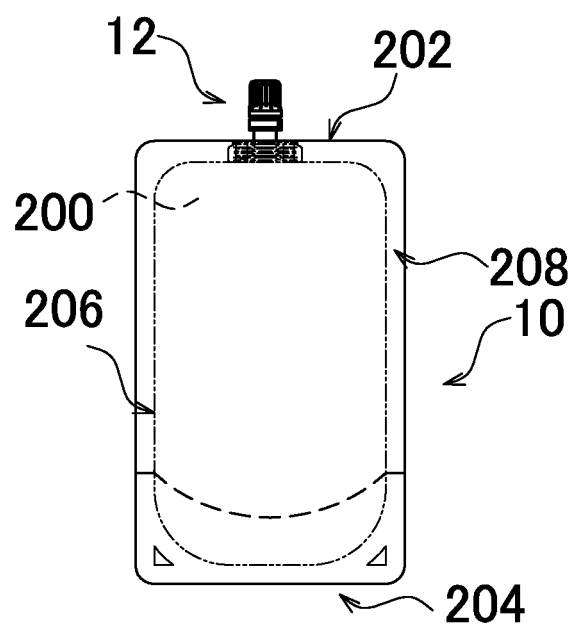
[図11C]

図11C

(6)

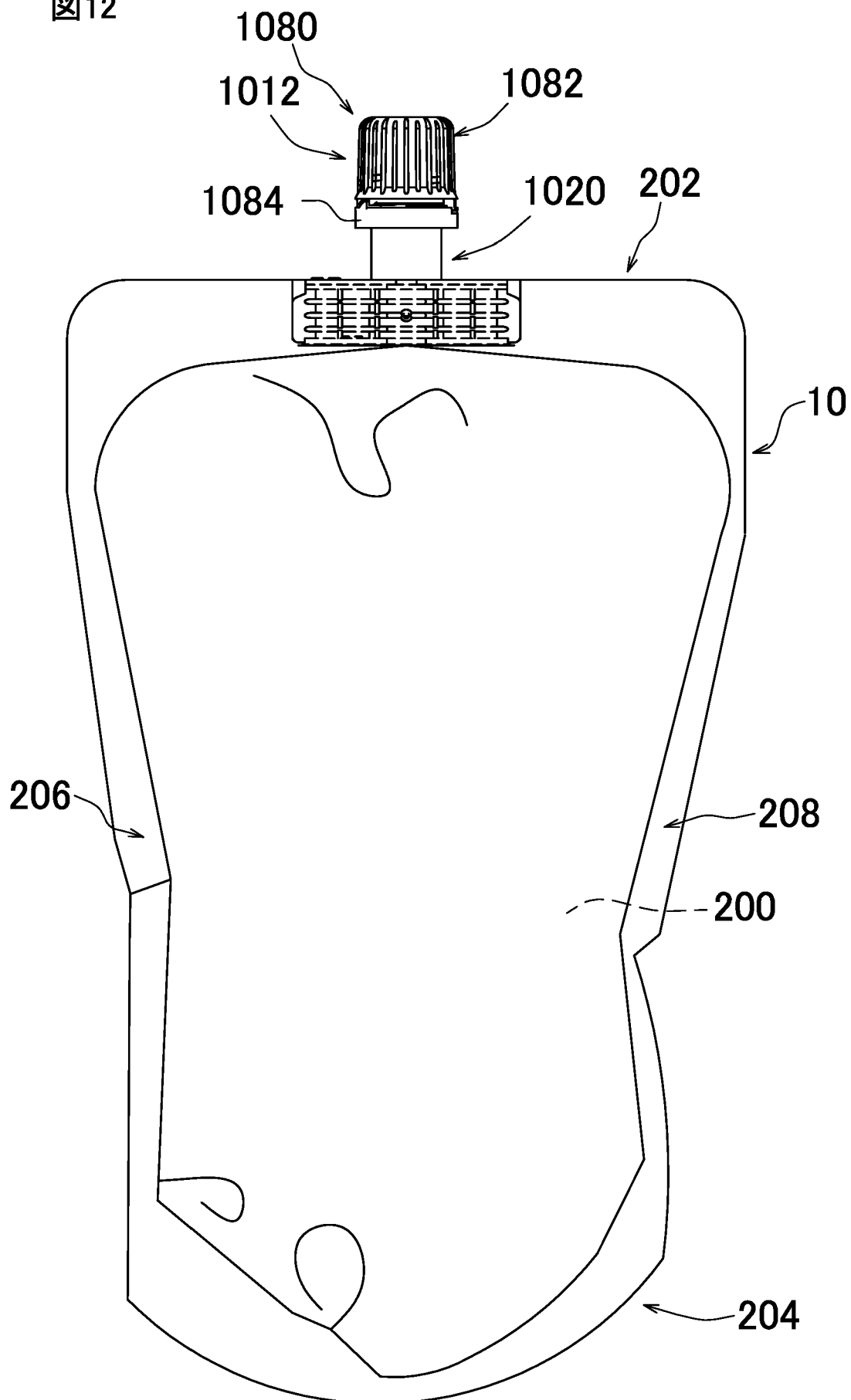


(7)



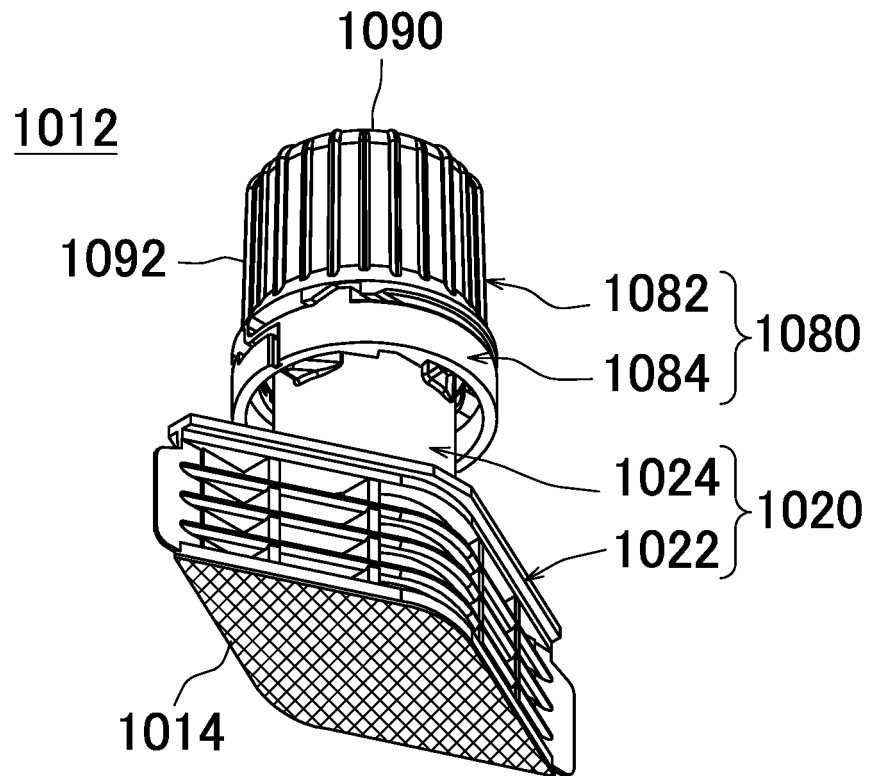
[図12]

図12



[図13]

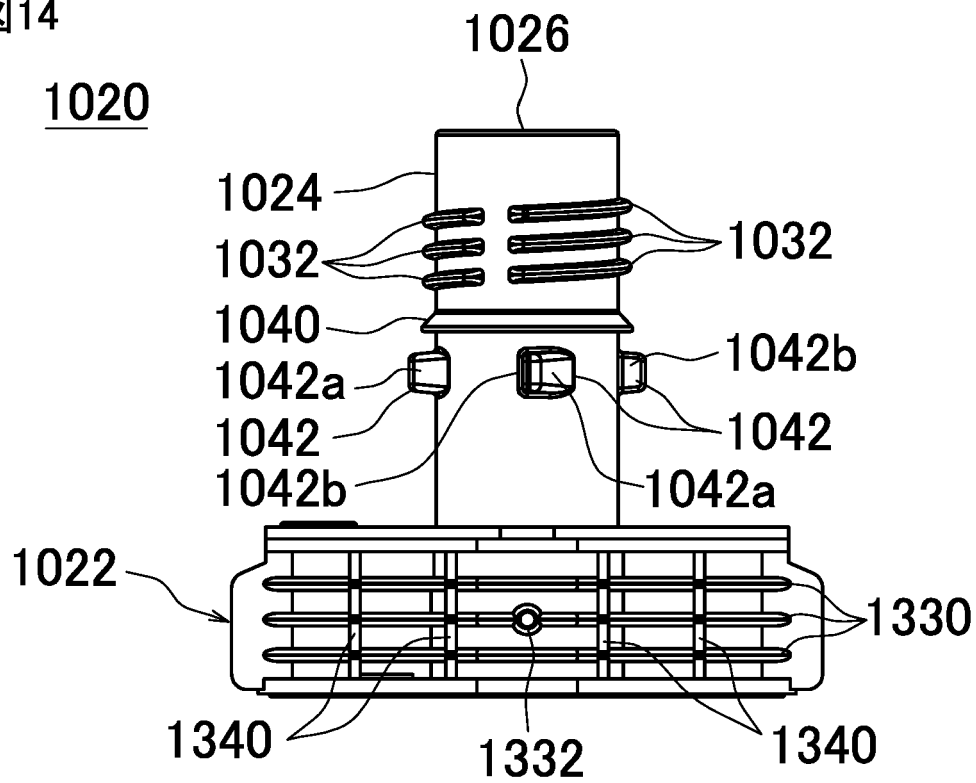
図13



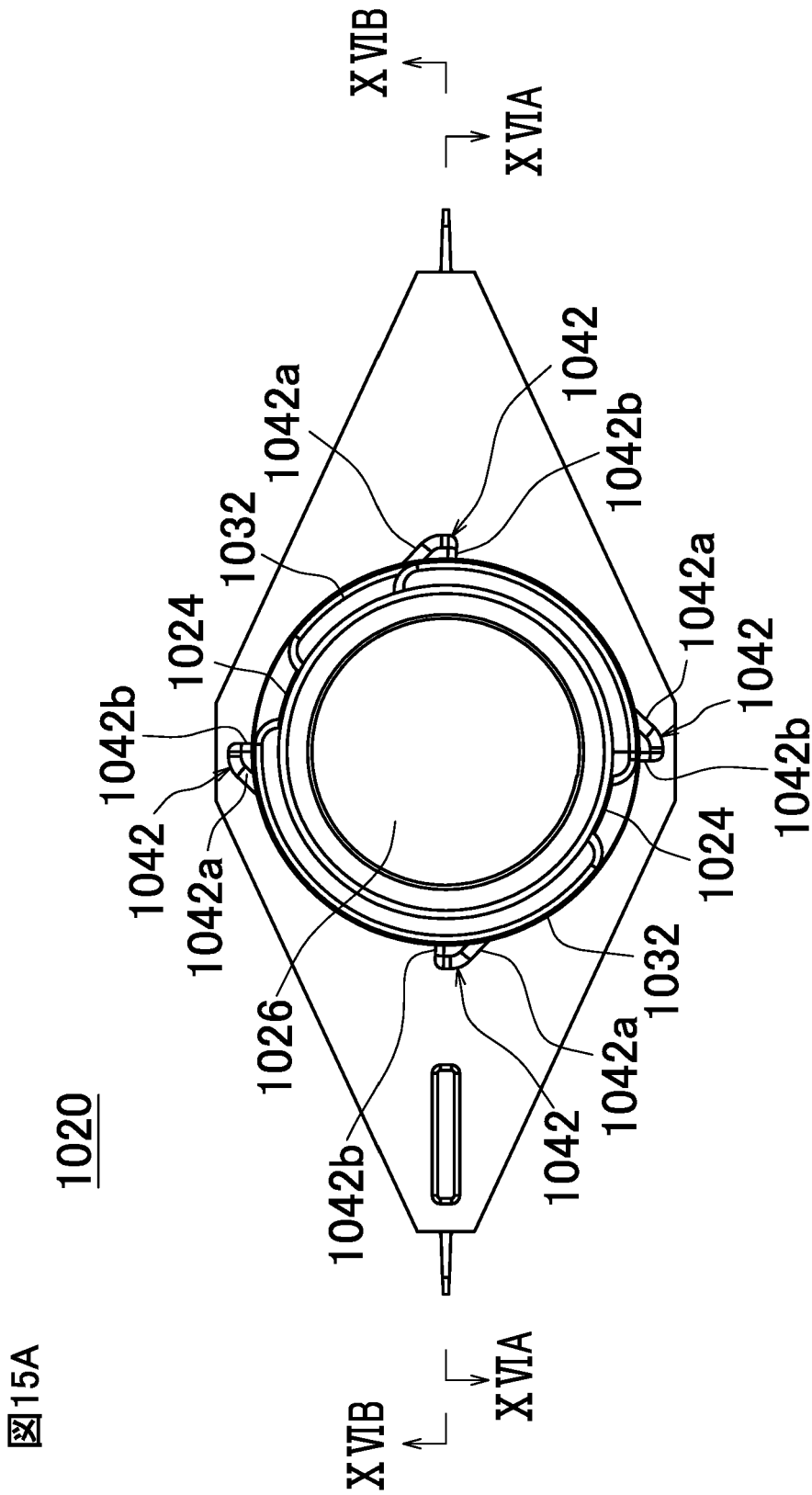
[図14]

図14

1020

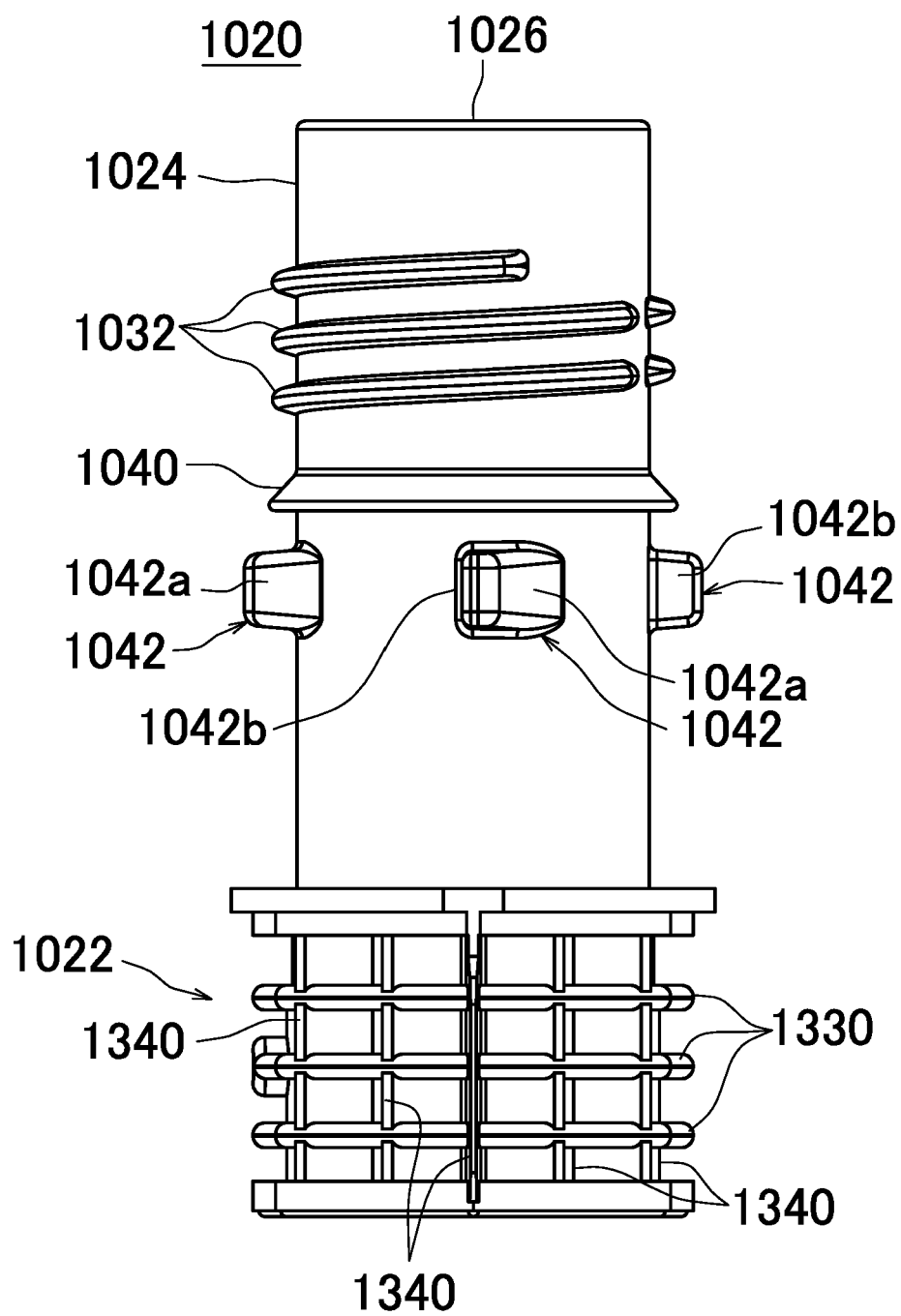


[図15A]



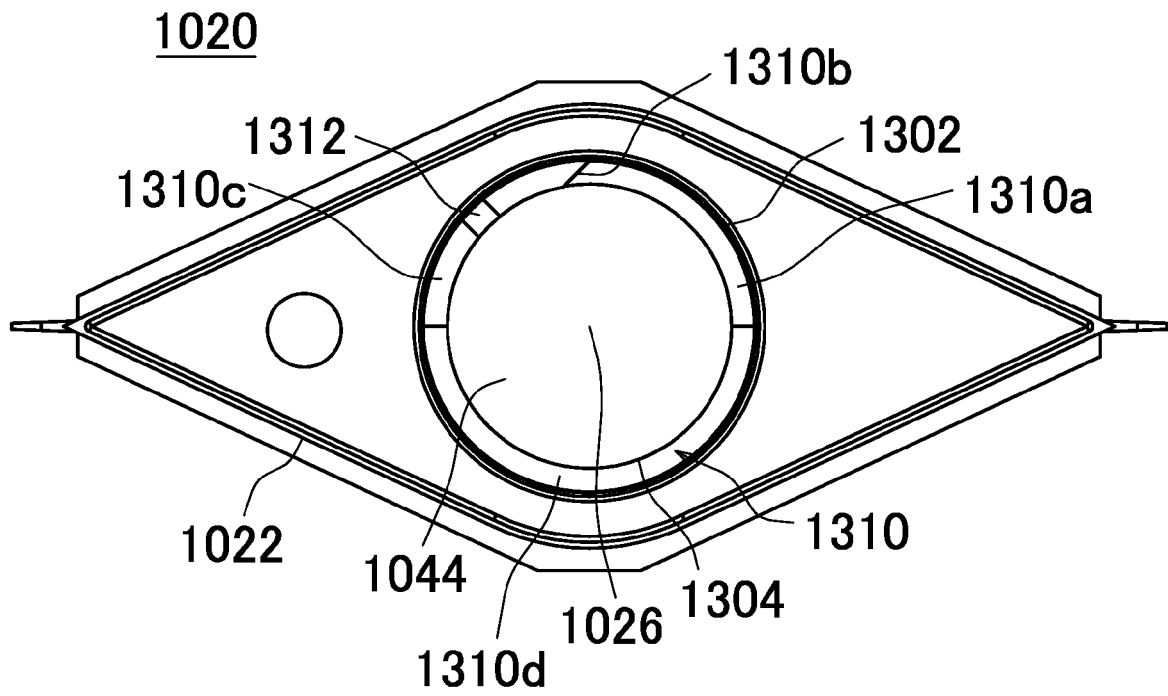
[図15B]

図15B



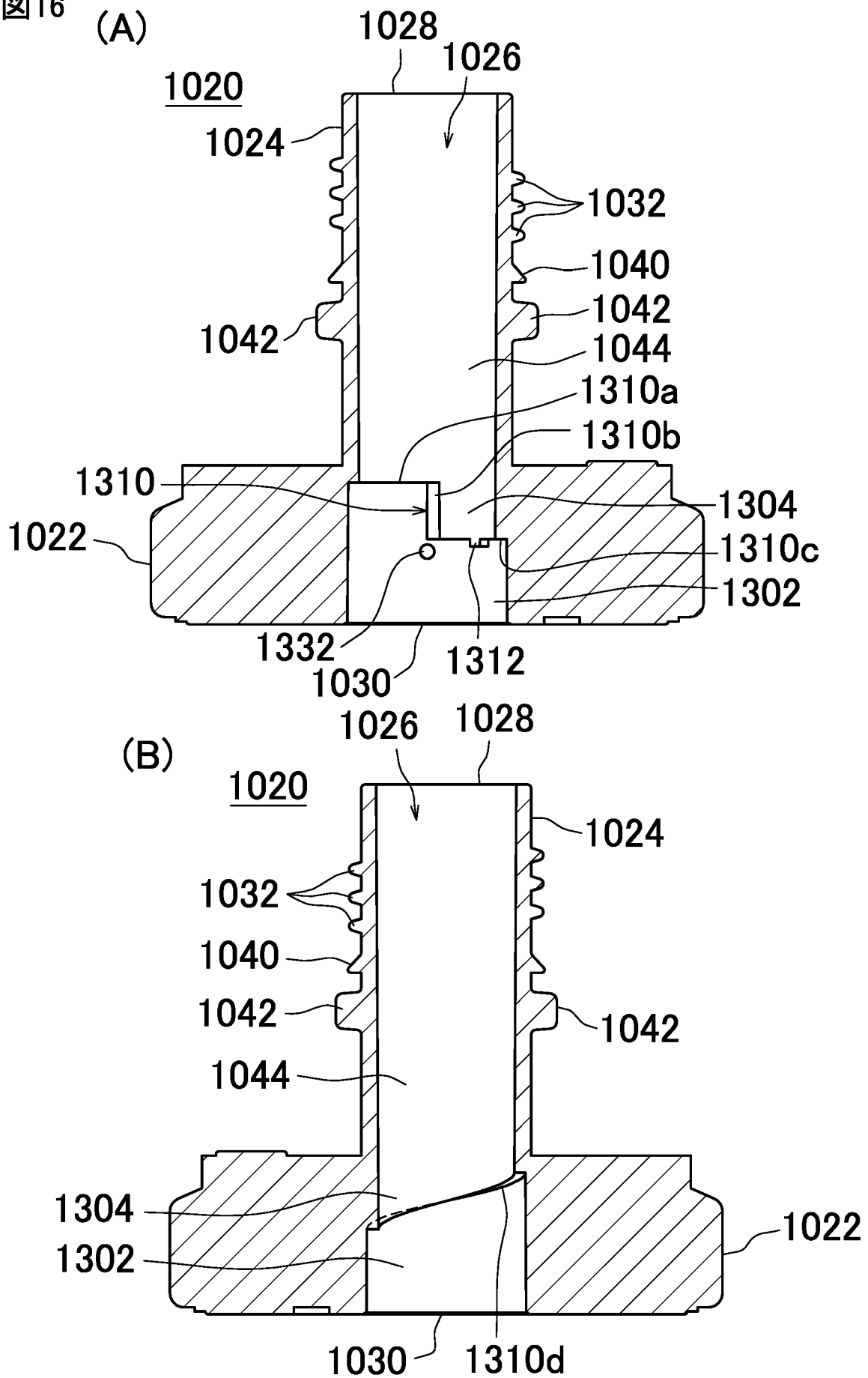
[図15C]

図15C



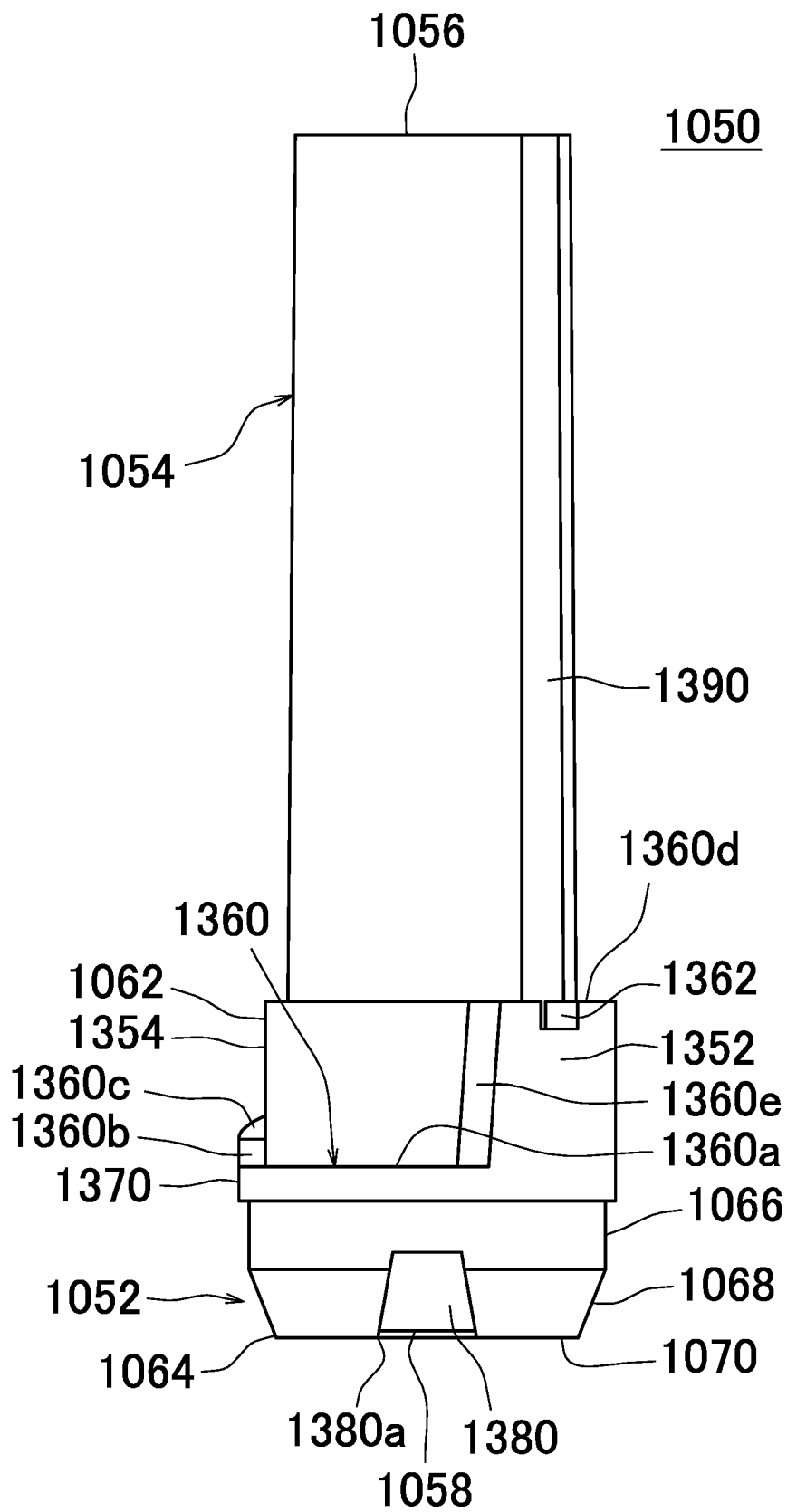
[図16]

図16



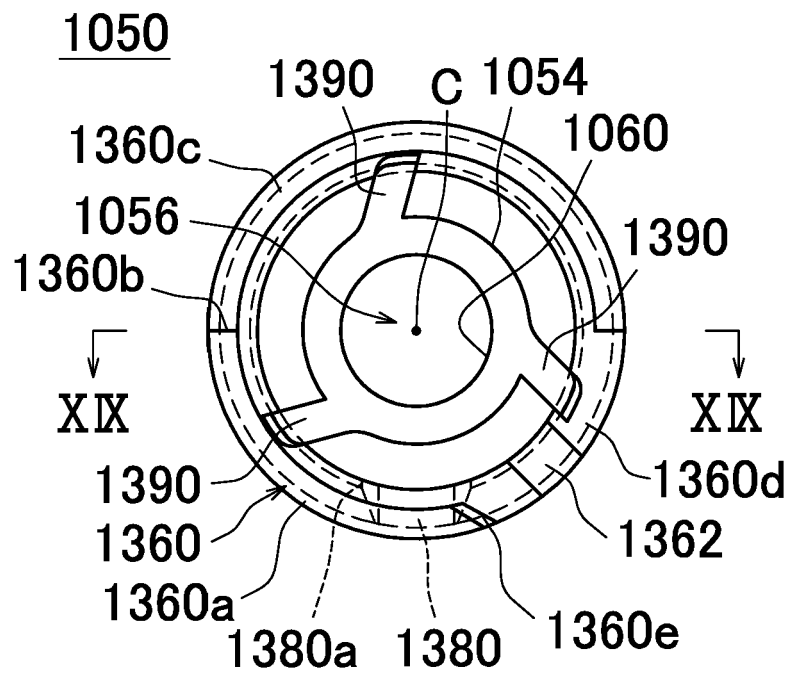
[図17]

図17



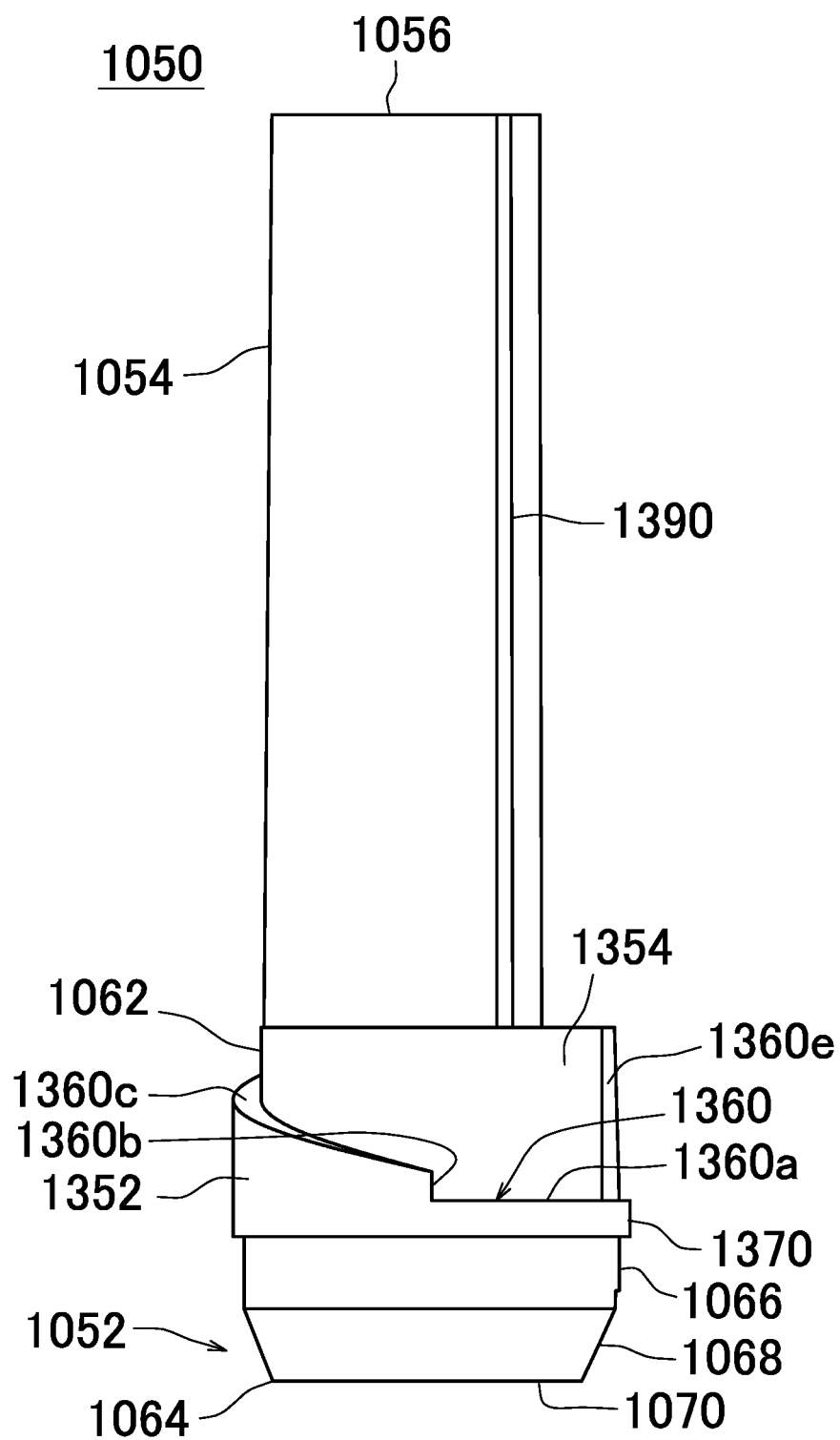
[図18A]

図18A



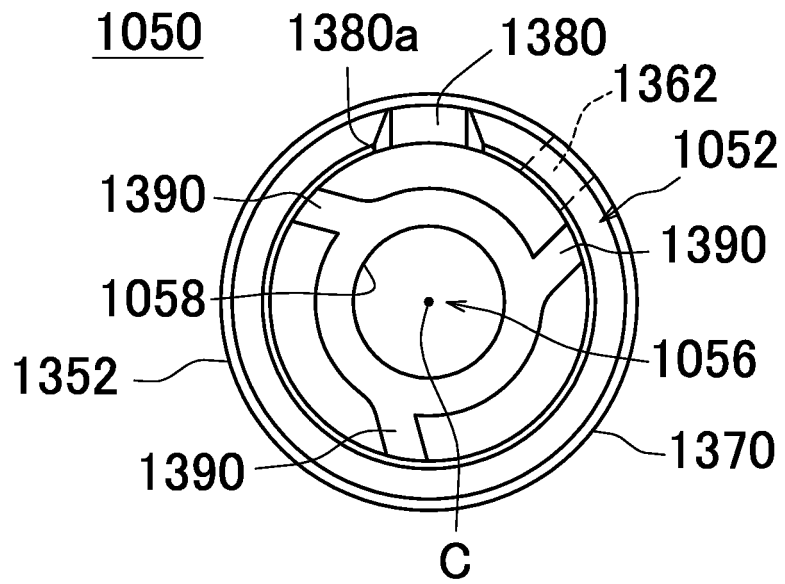
[図18B]

図18B



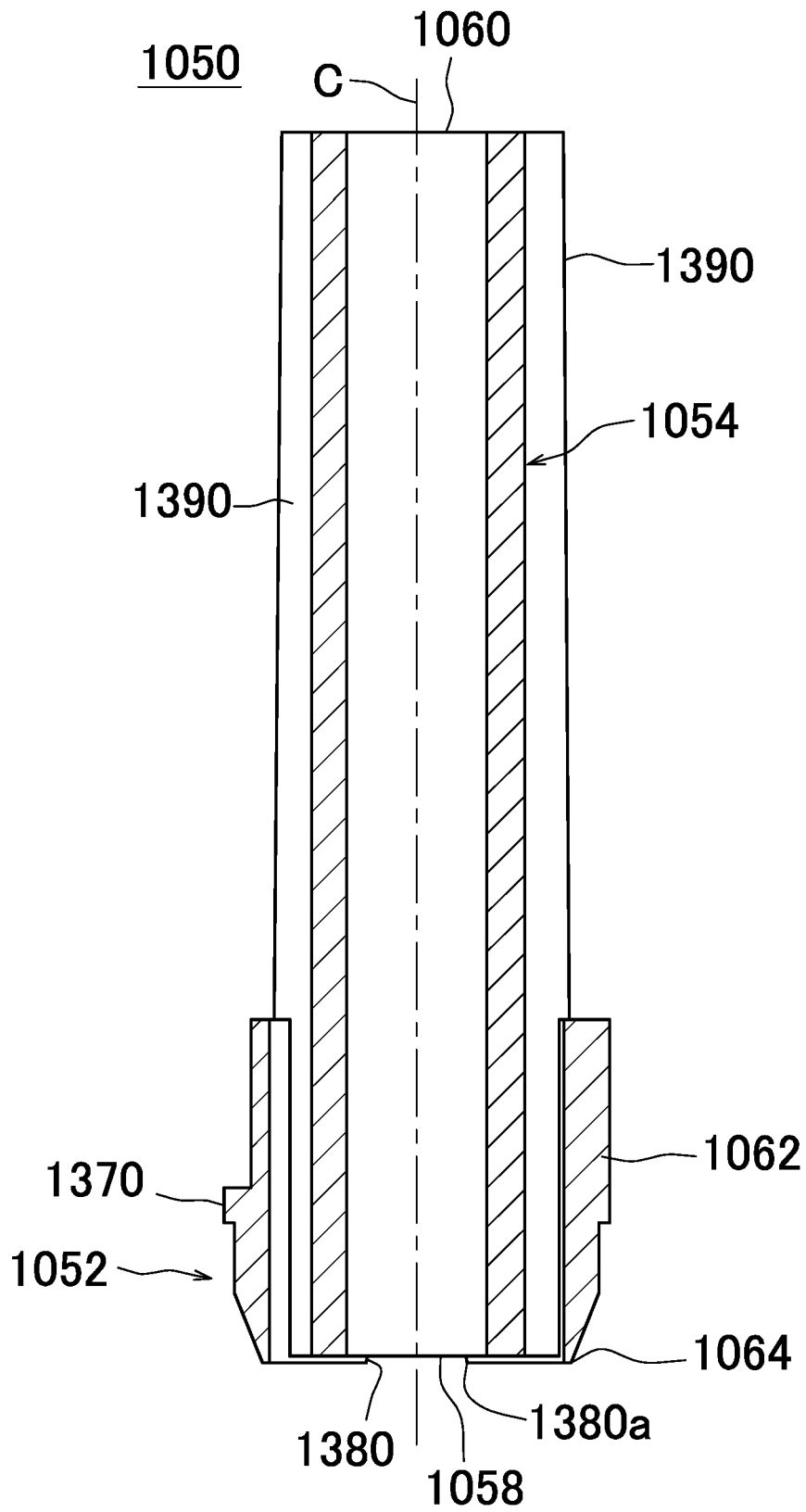
[図18C]

図18C



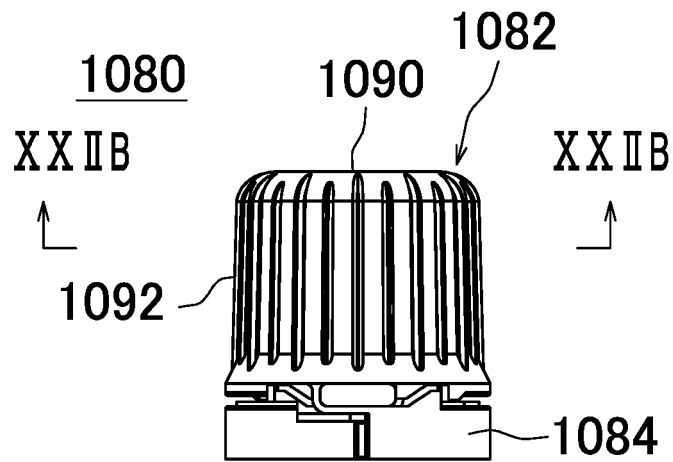
[図19]

図19



[図20]

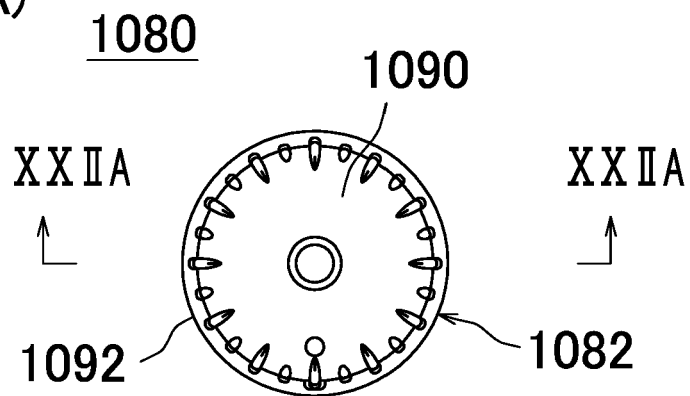
図20



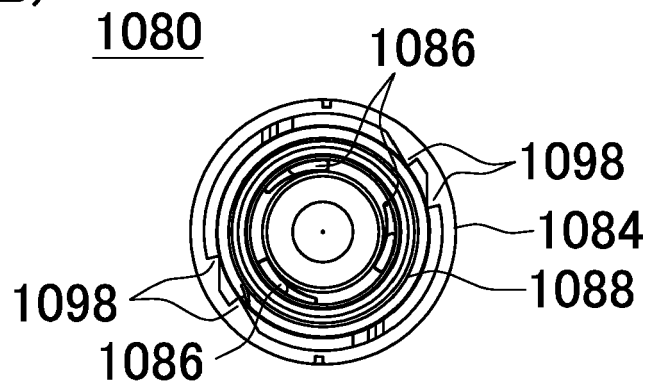
[図21]

図21

(A)

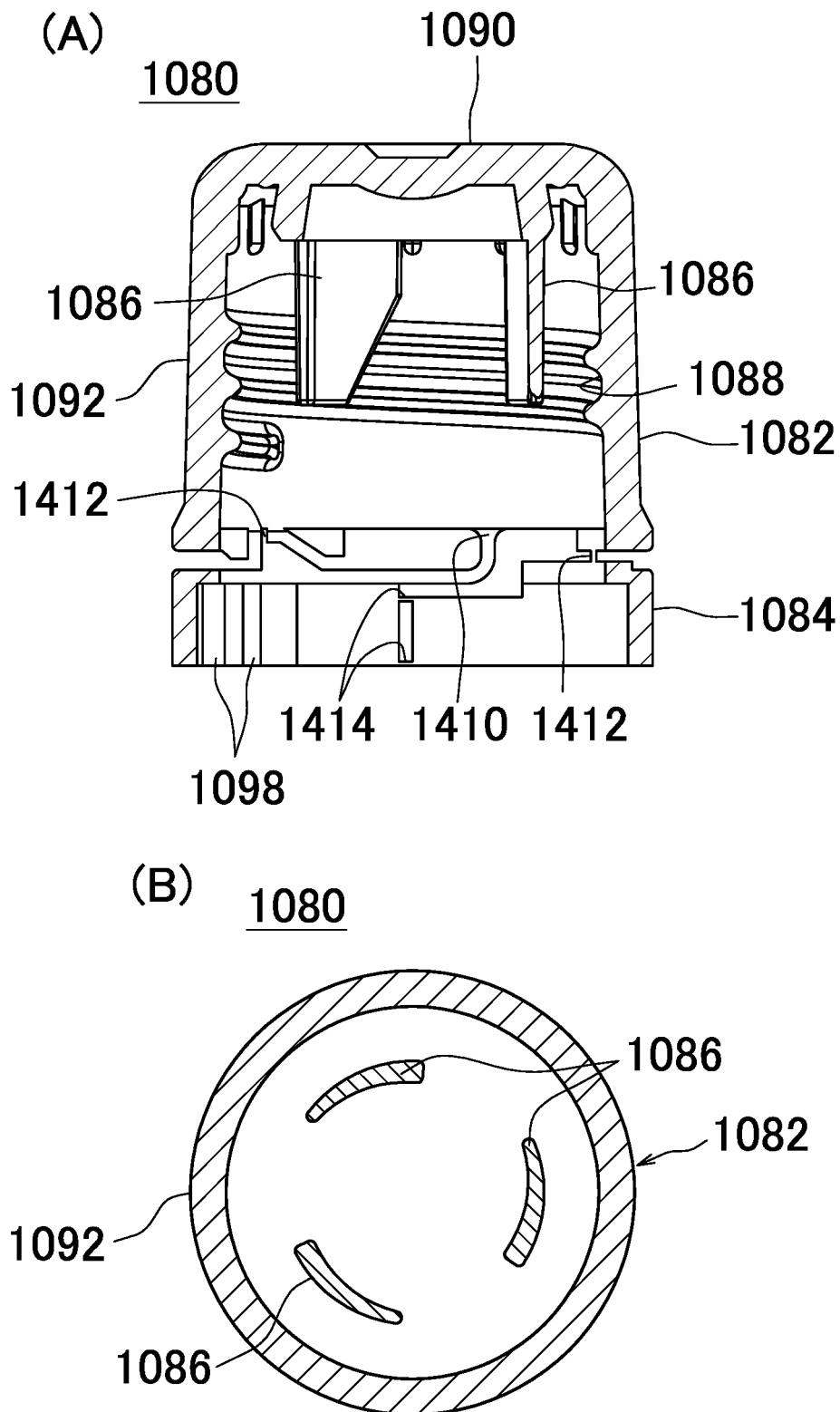


(B)



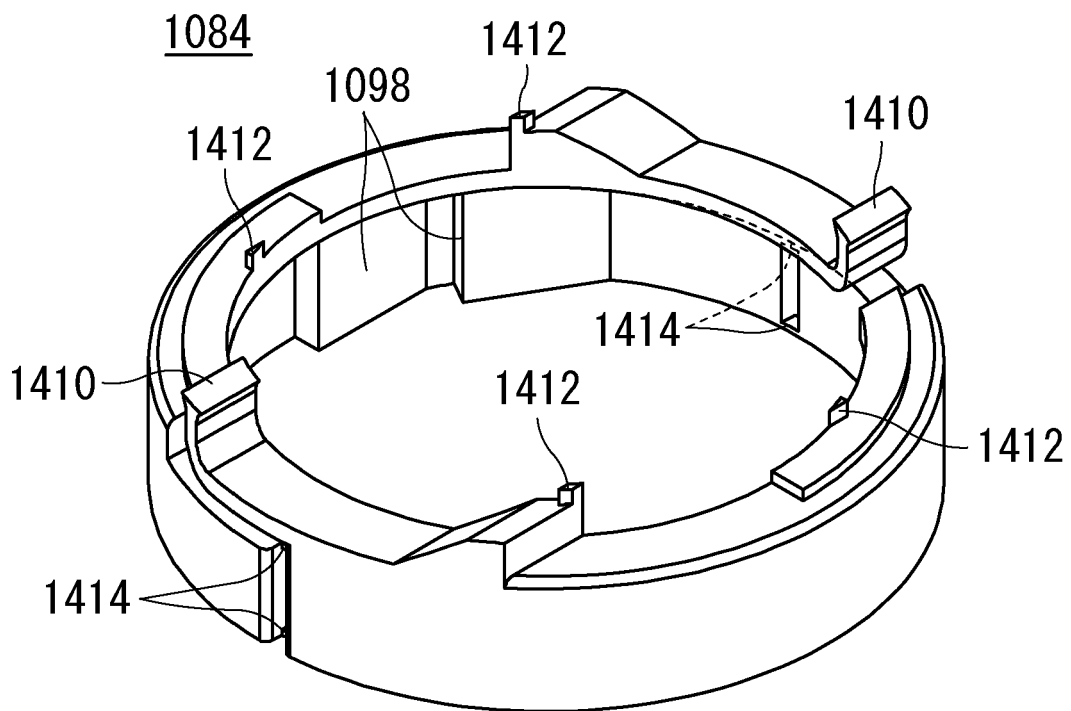
[図22]

図22



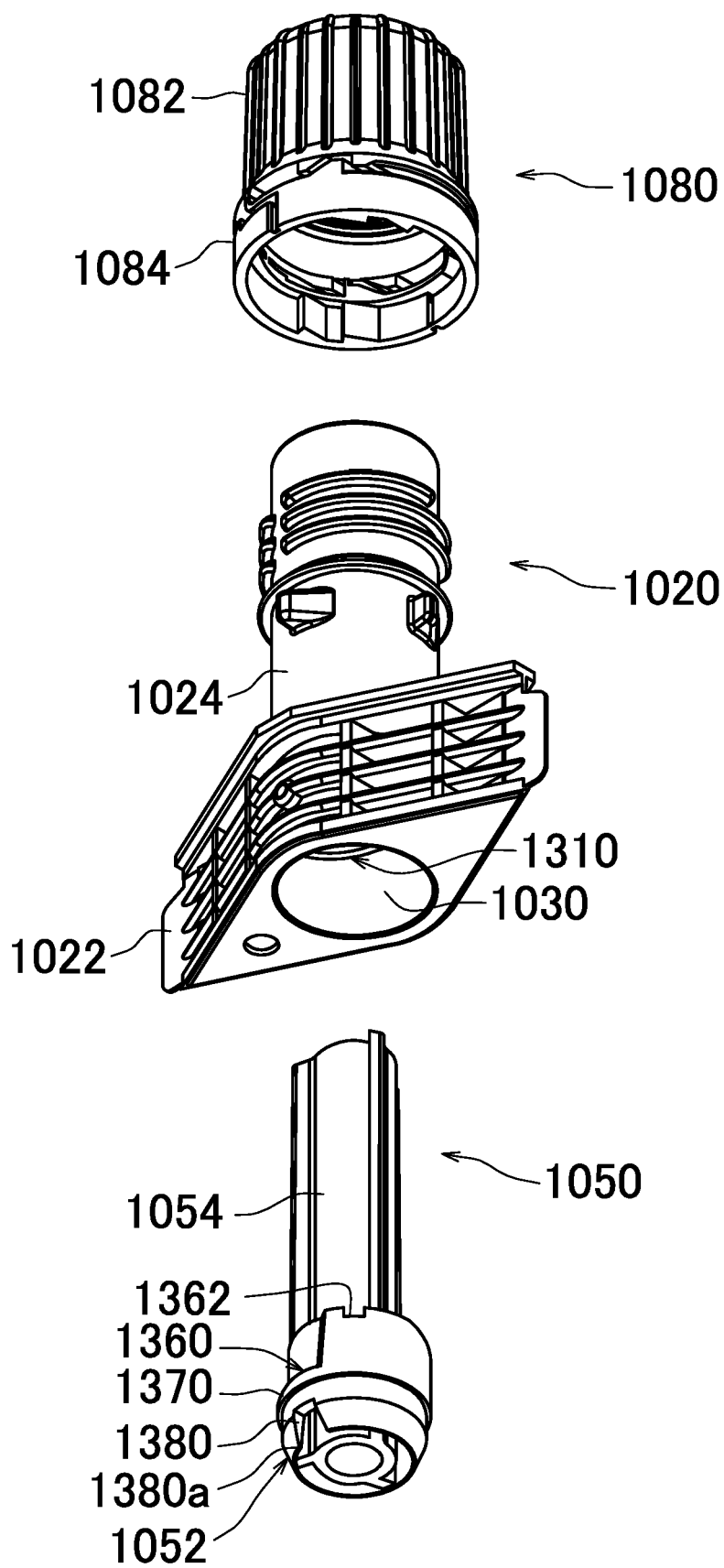
[図23]

図23



[図24]

図24



[図25]

図25

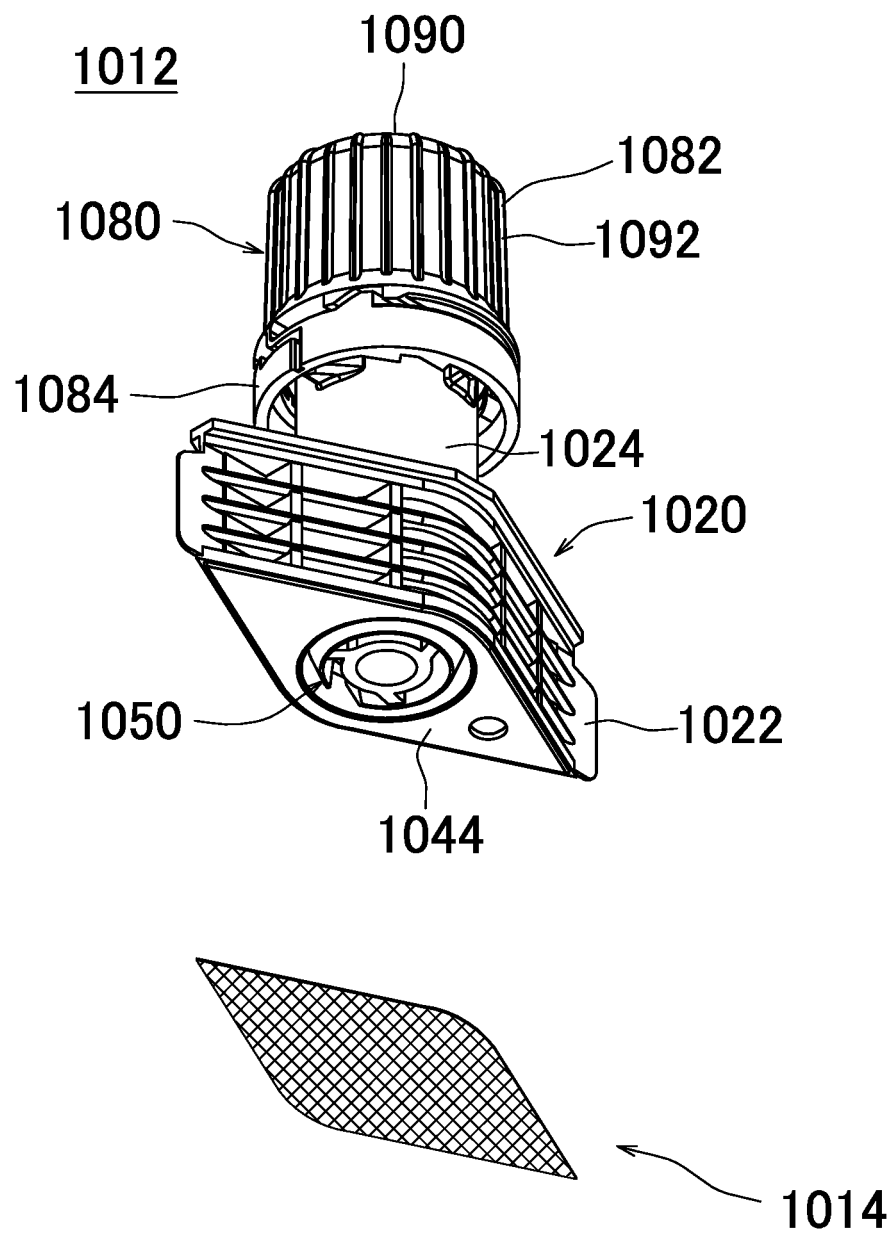
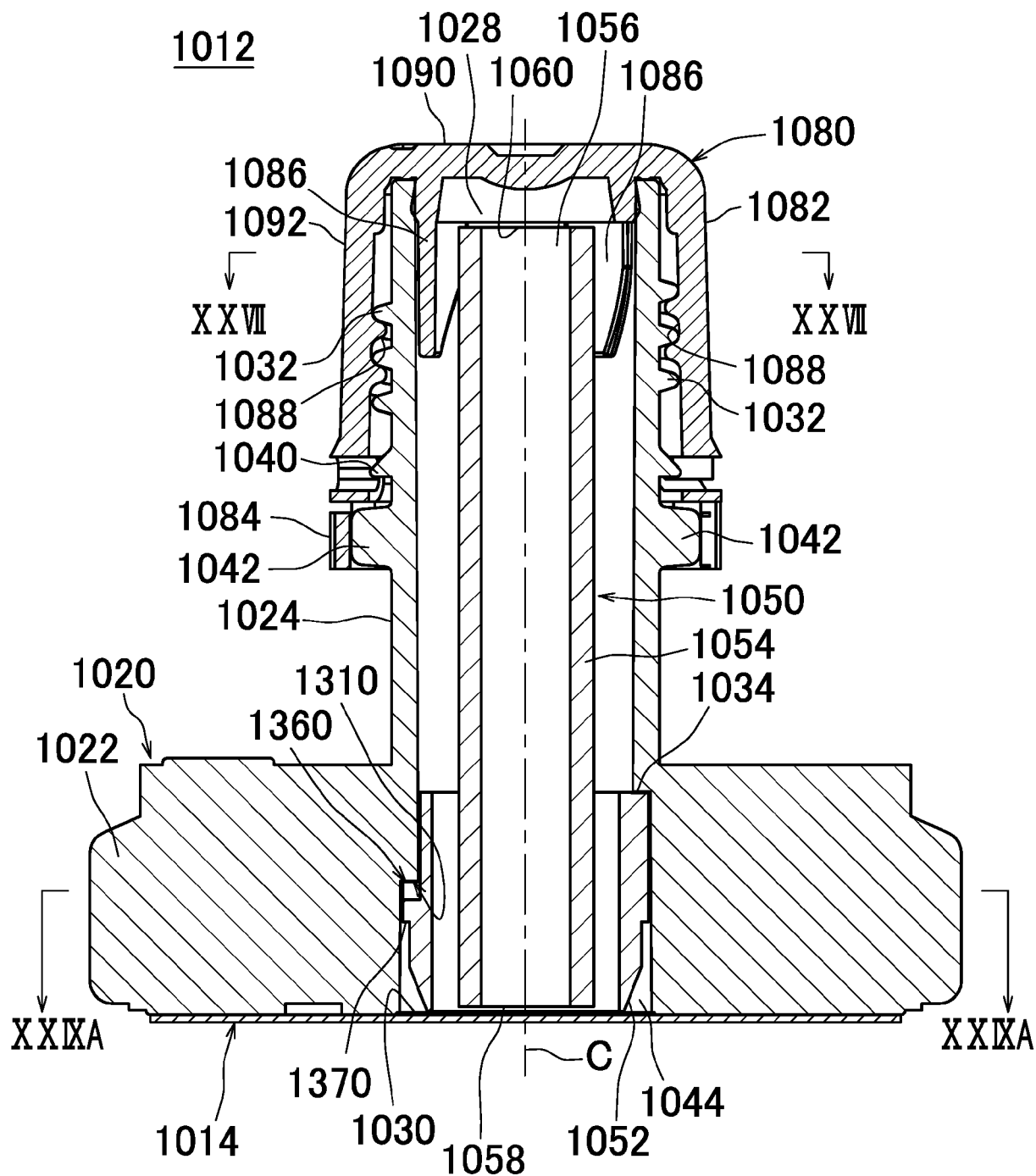


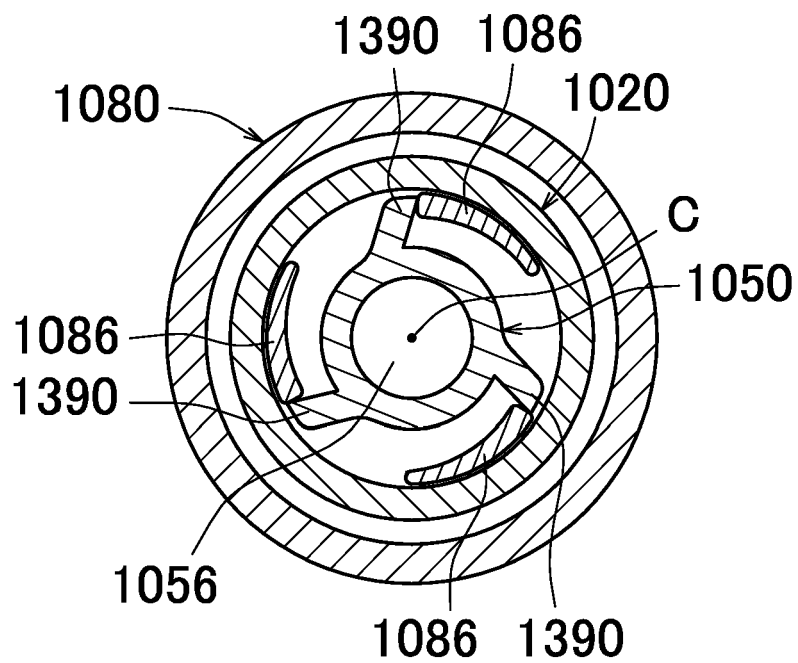
图 26



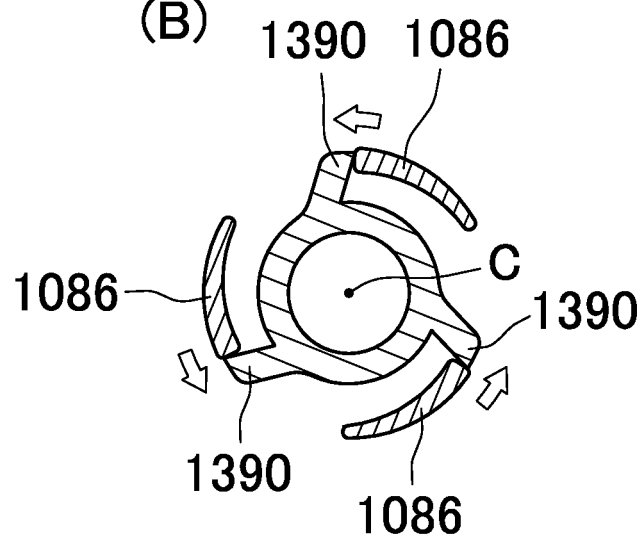
[図27]

図27

(A)

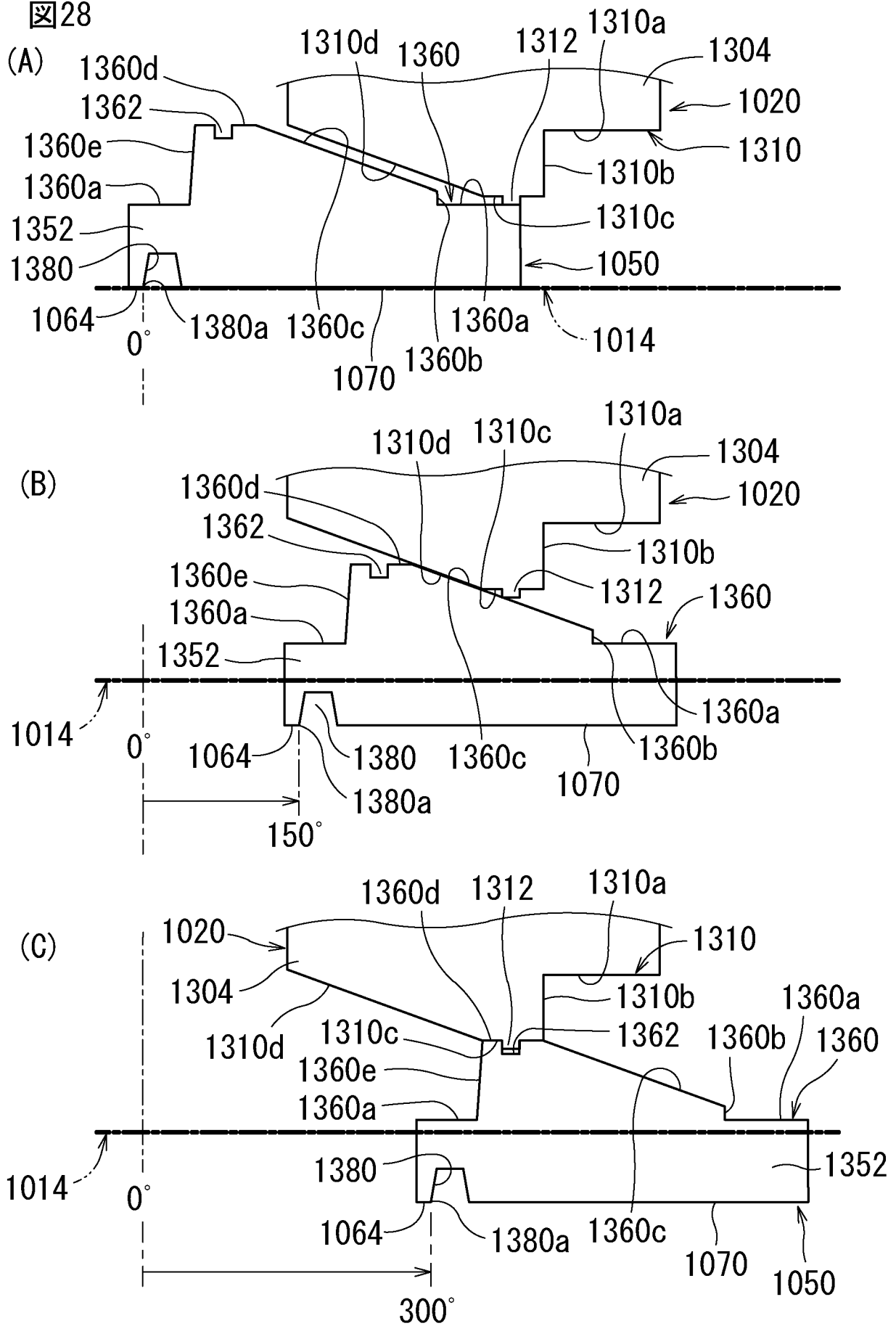
1012

(B)



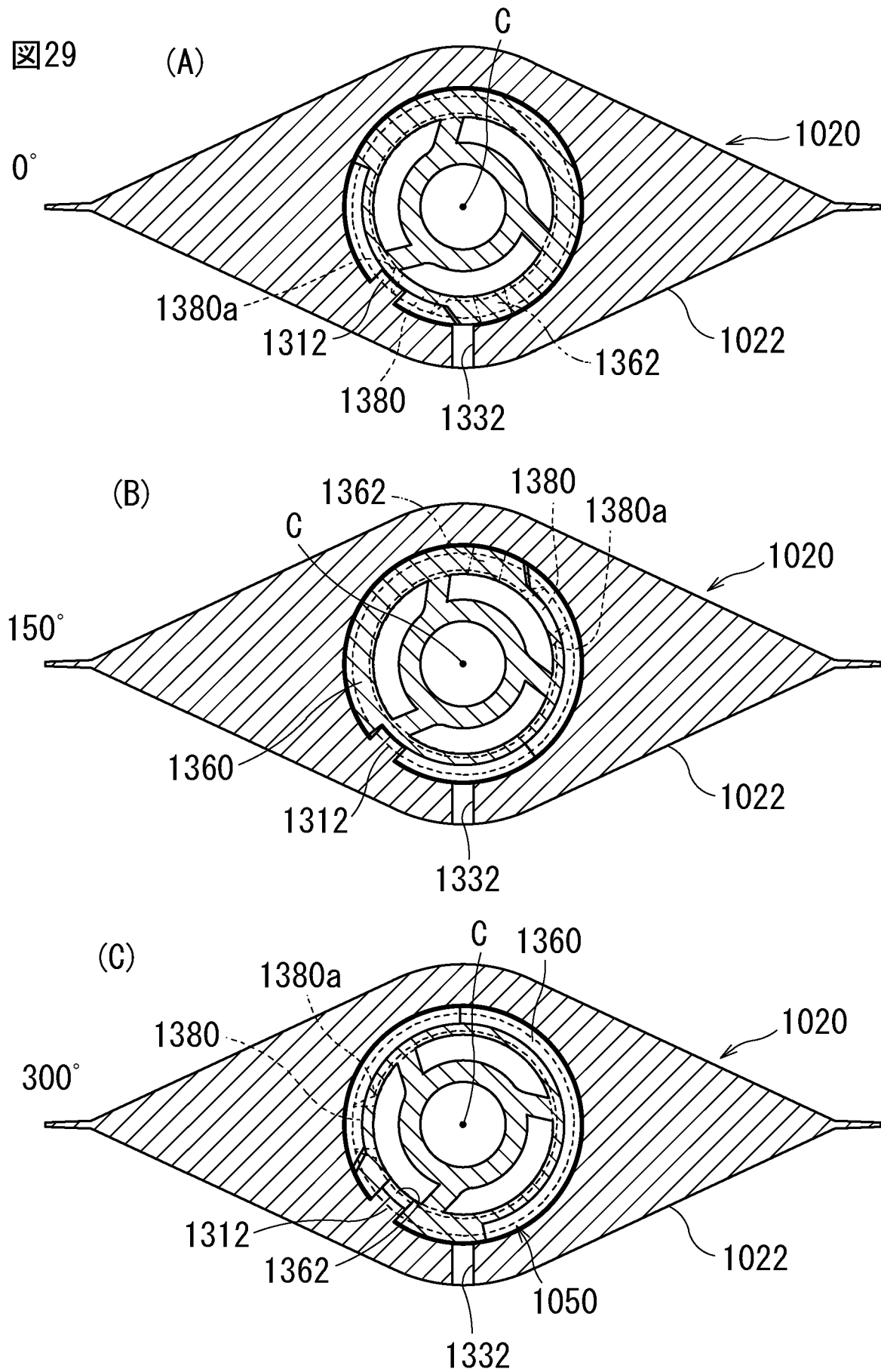
[図28]

図28



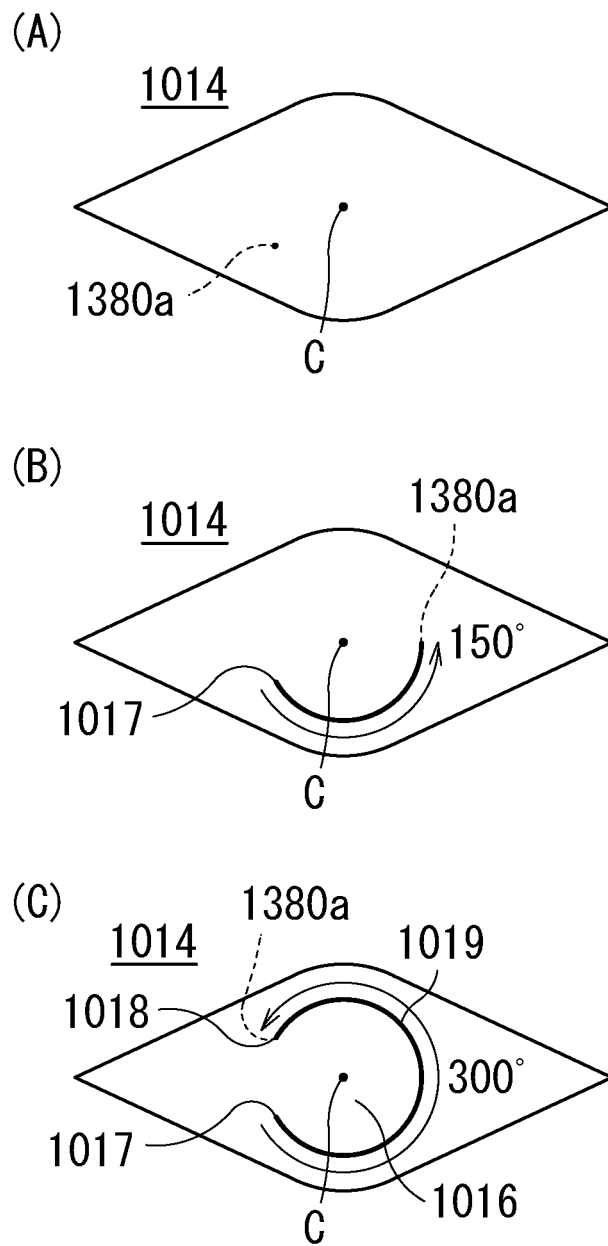
[図29]

図29



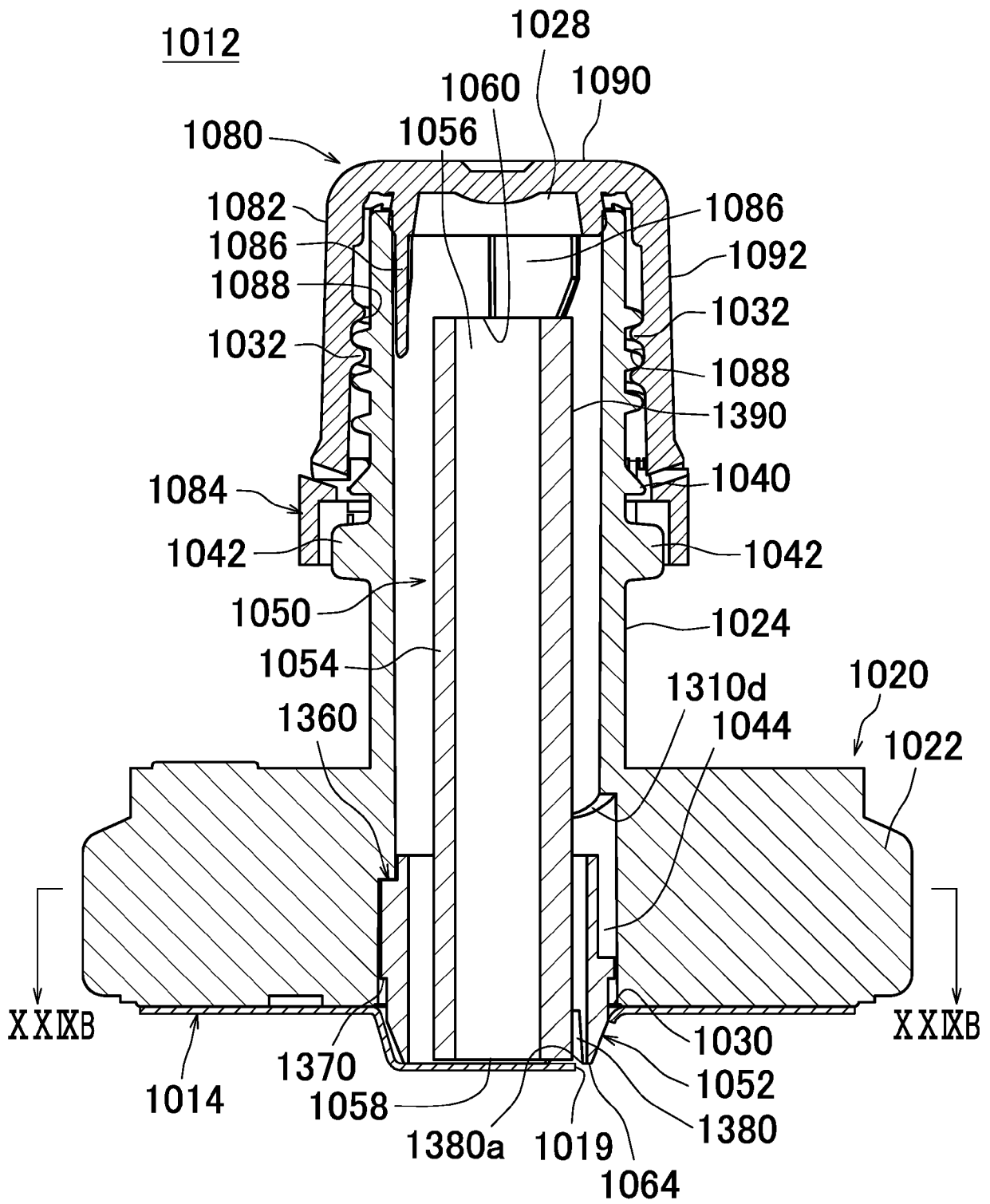
[図30]

図30



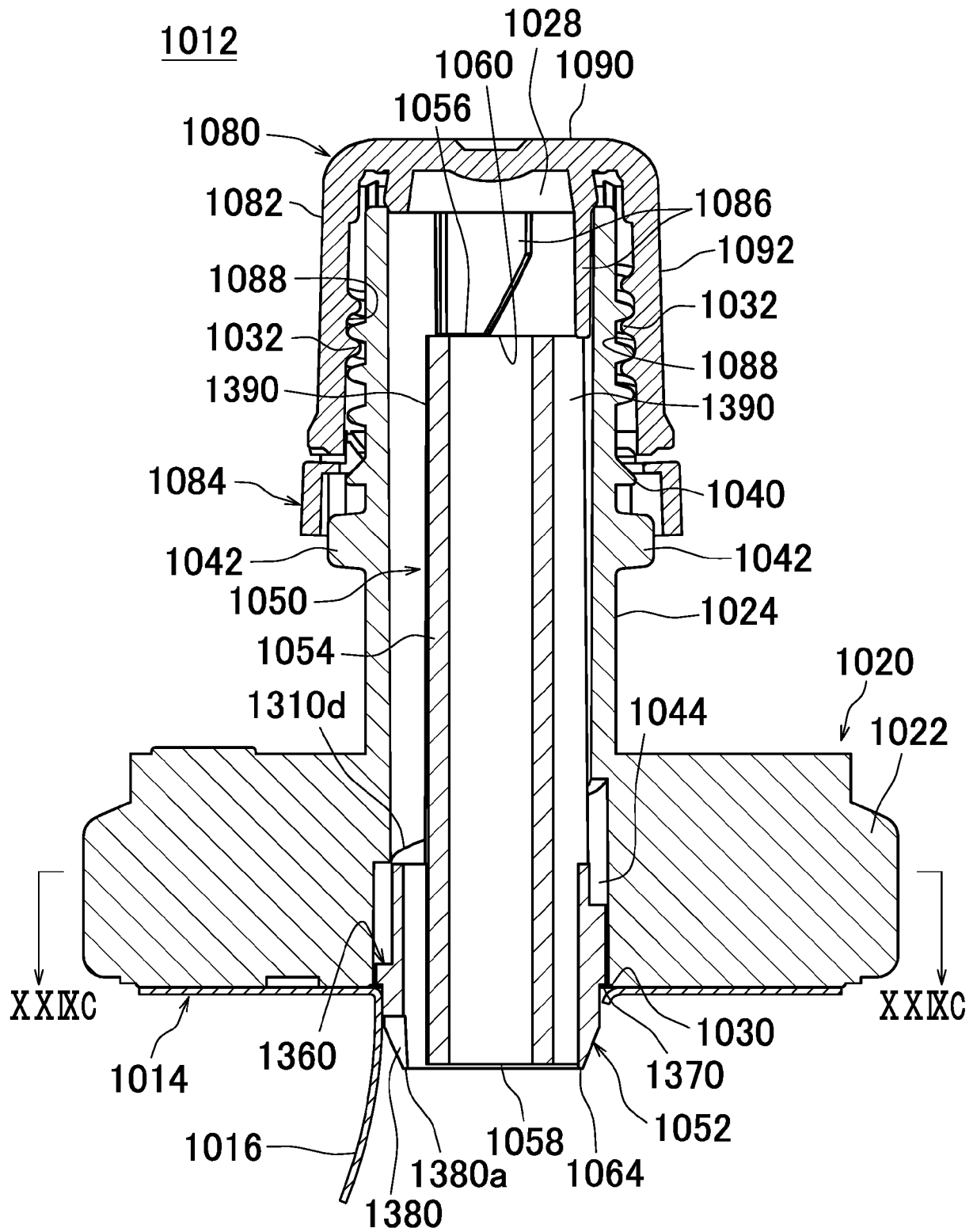
[図31]

図31



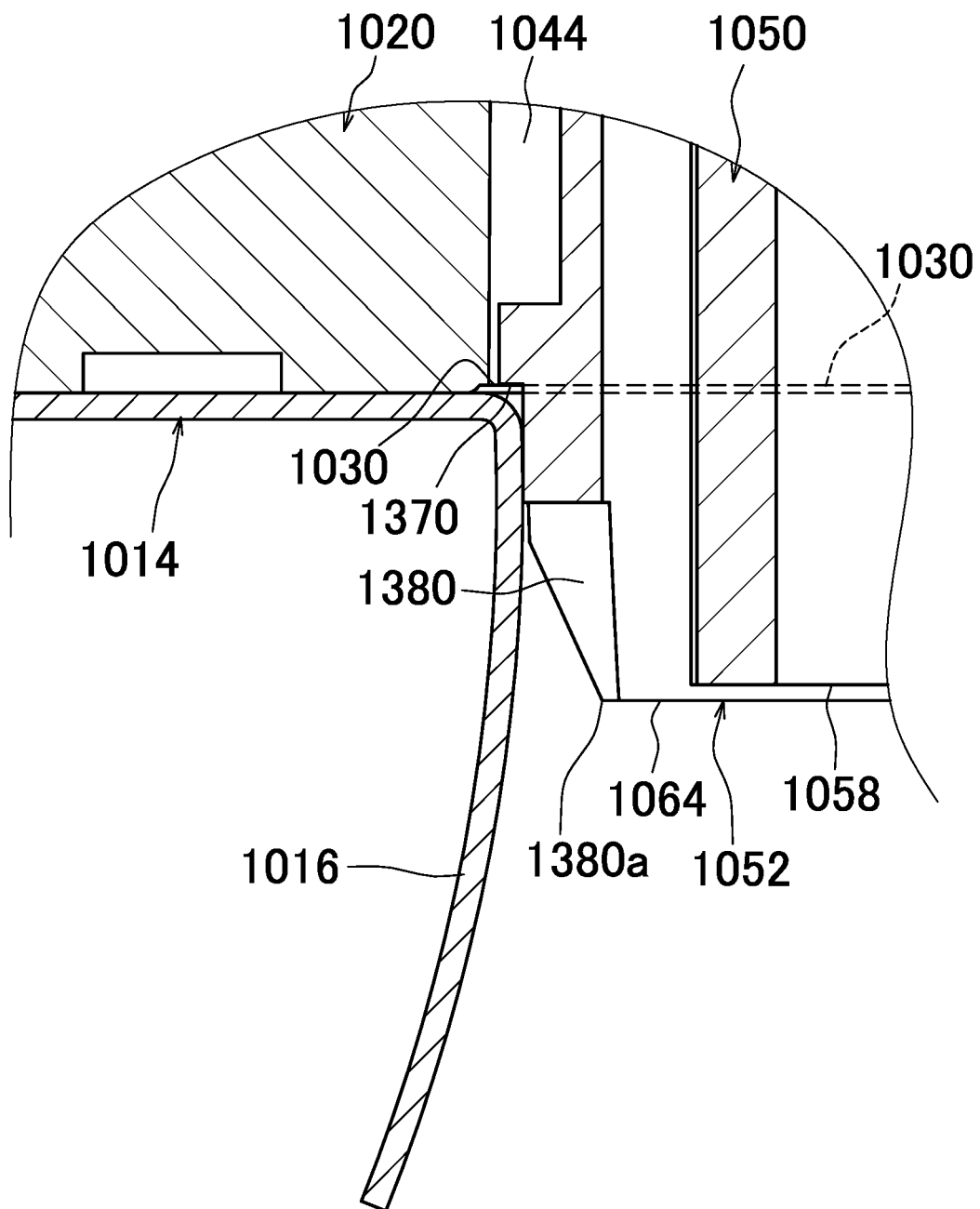
[図32]

図32



[図33]

図33



[図34]

図34

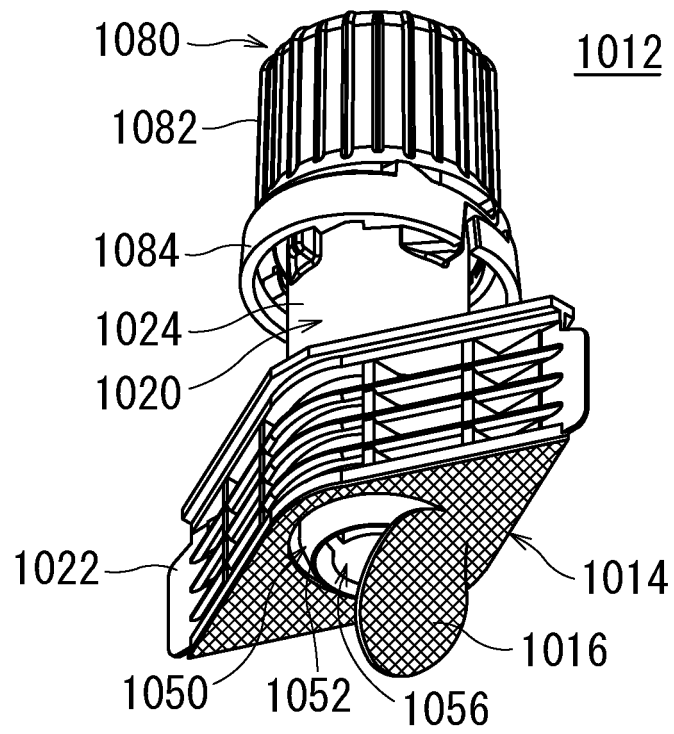


図35

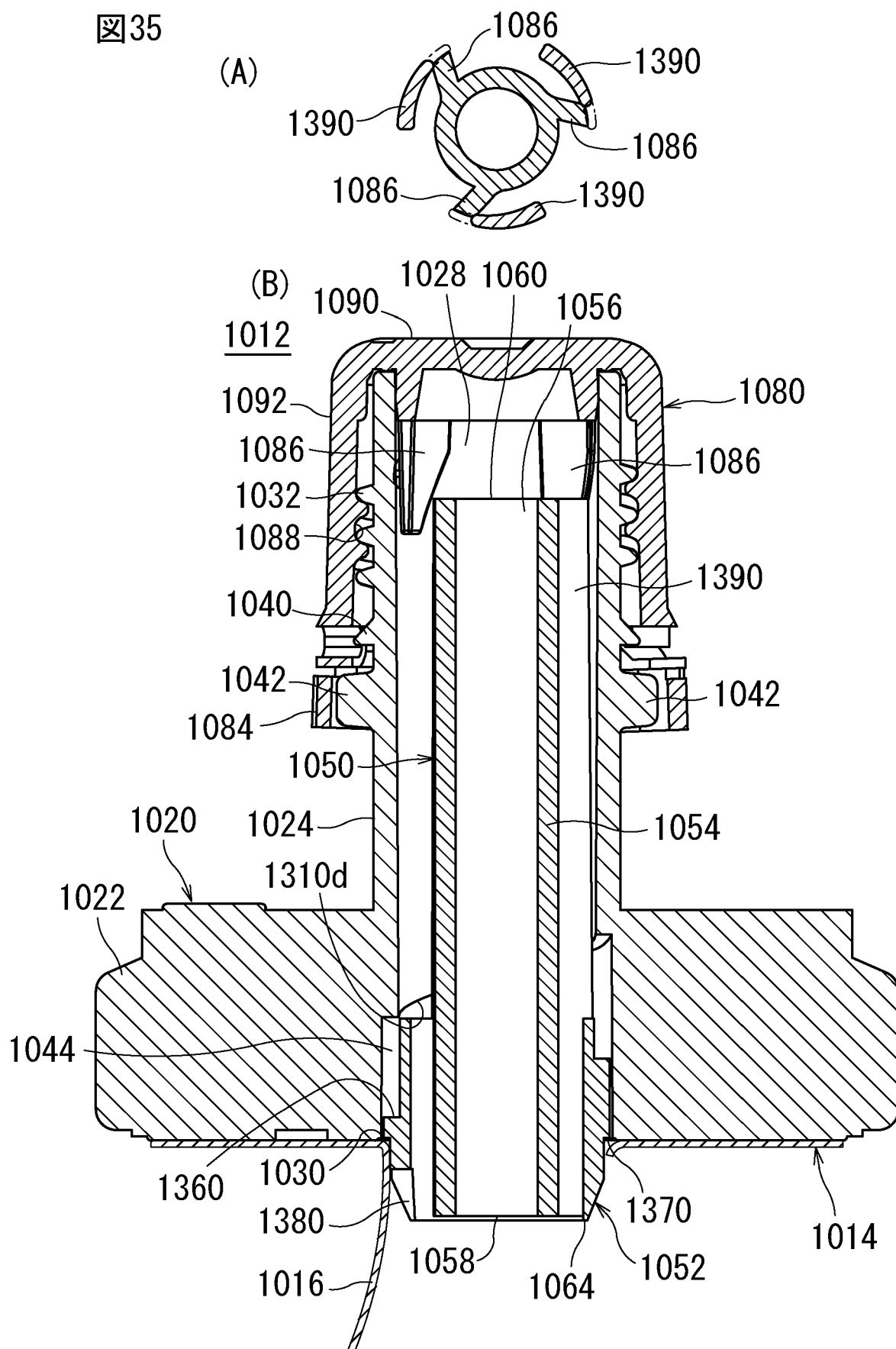
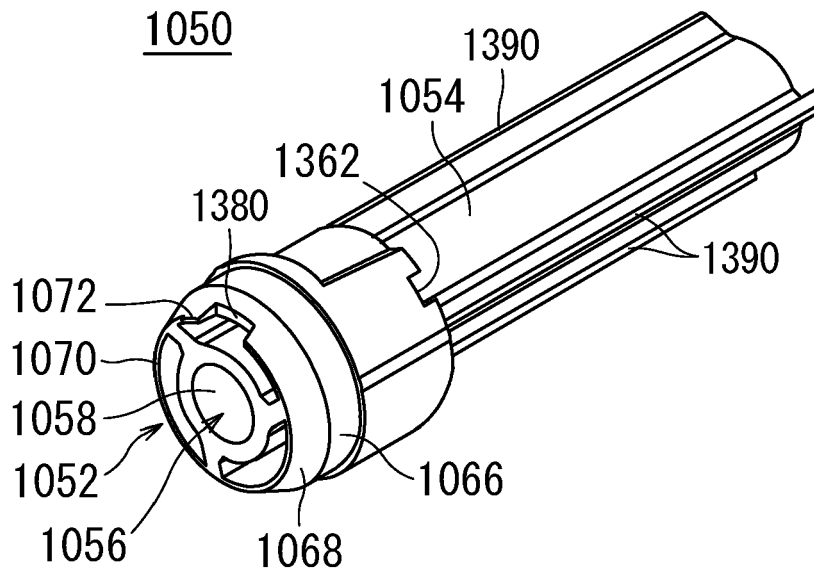


図36

Figure 1 consists of three cross-sectional views of a semiconductor device.
 (A) is a main cross-sectional view showing a substrate 200 with a trench 210. A gate stack 1020 is on the top surface, and a gate 1014 is on the side of the trench. A conductive layer 220 is on the bottom of the trench.
 (B) is a detail view of the H portion (H部詳細) showing the gate stack 1020, gate 1014, and conductive layer 220.
 (C) is a detail view of the I portion (I部詳細) showing the gate stack 1020, gate 1014, and conductive layer 220.

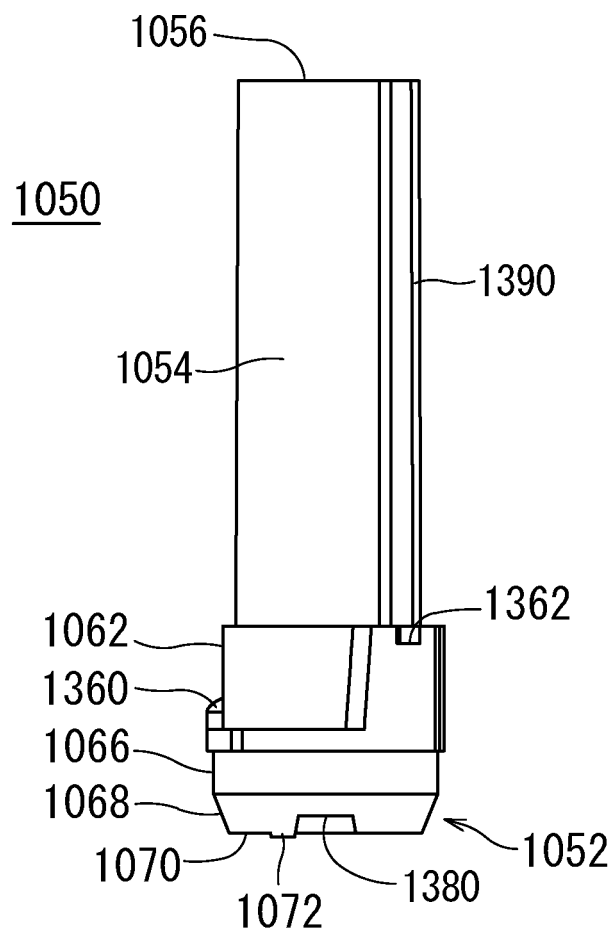
[図37]

図37



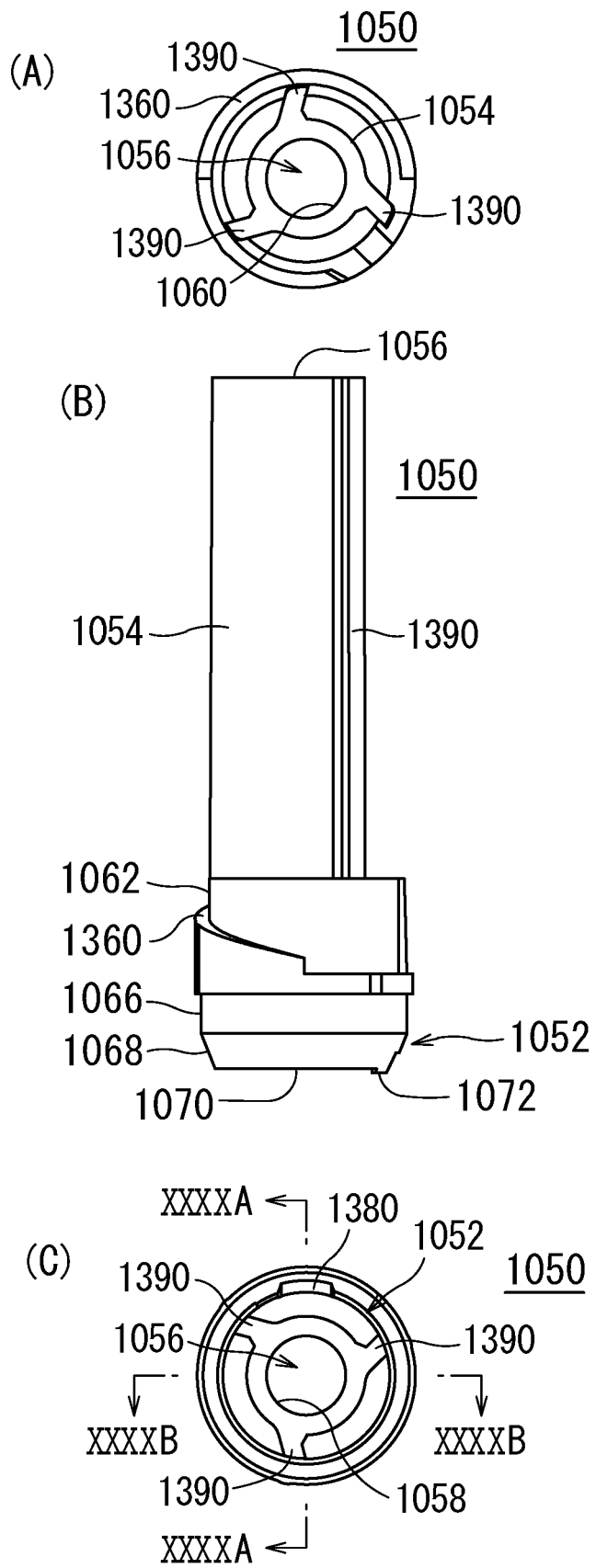
[図38]

図38



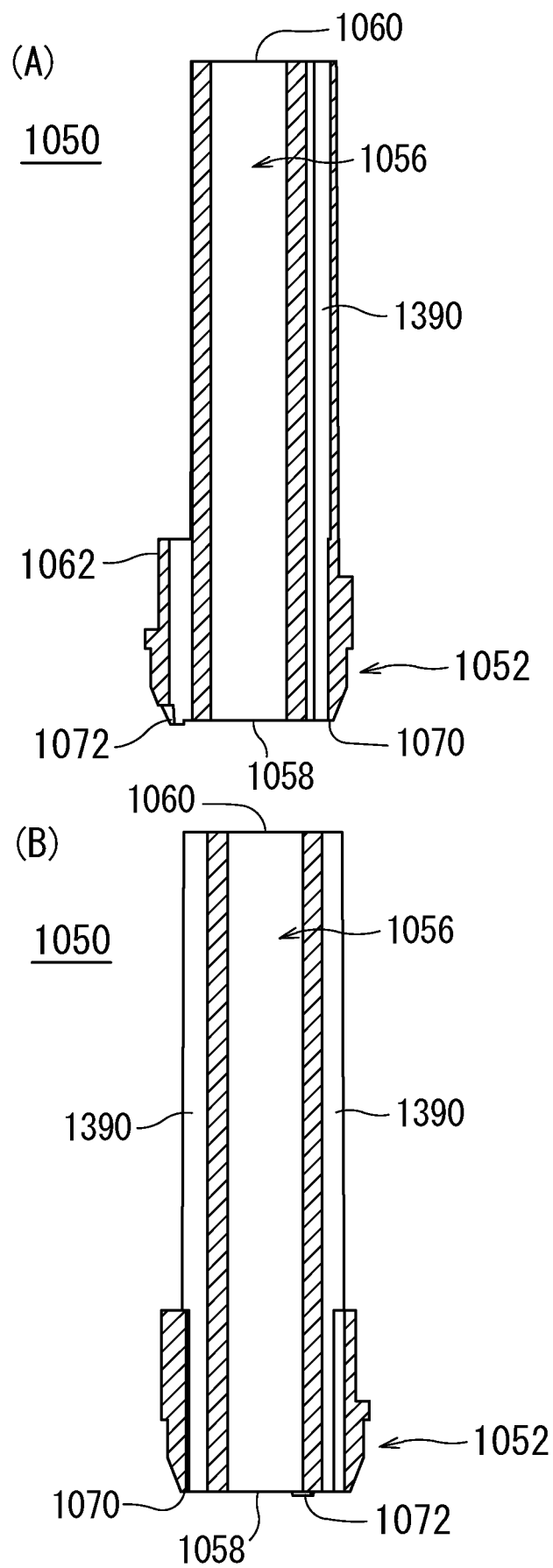
[図39]

図39



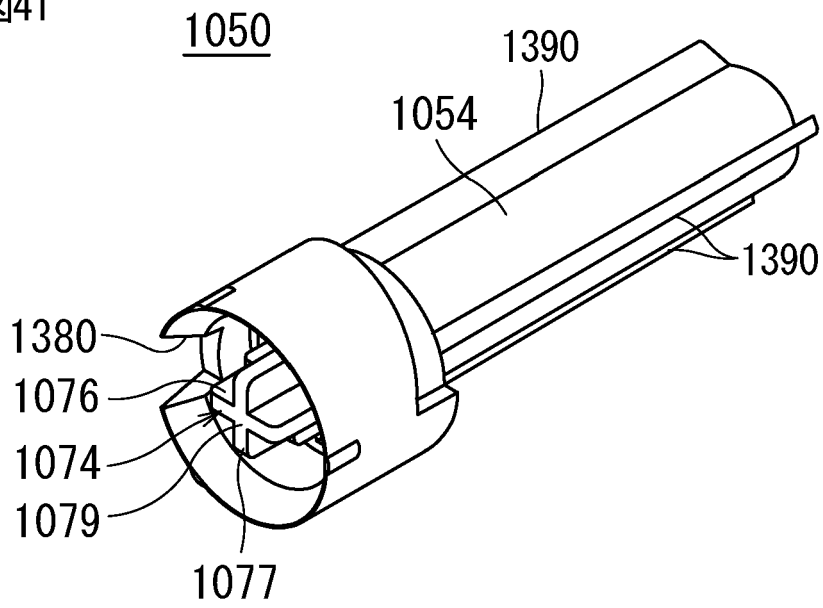
[図40]

図40



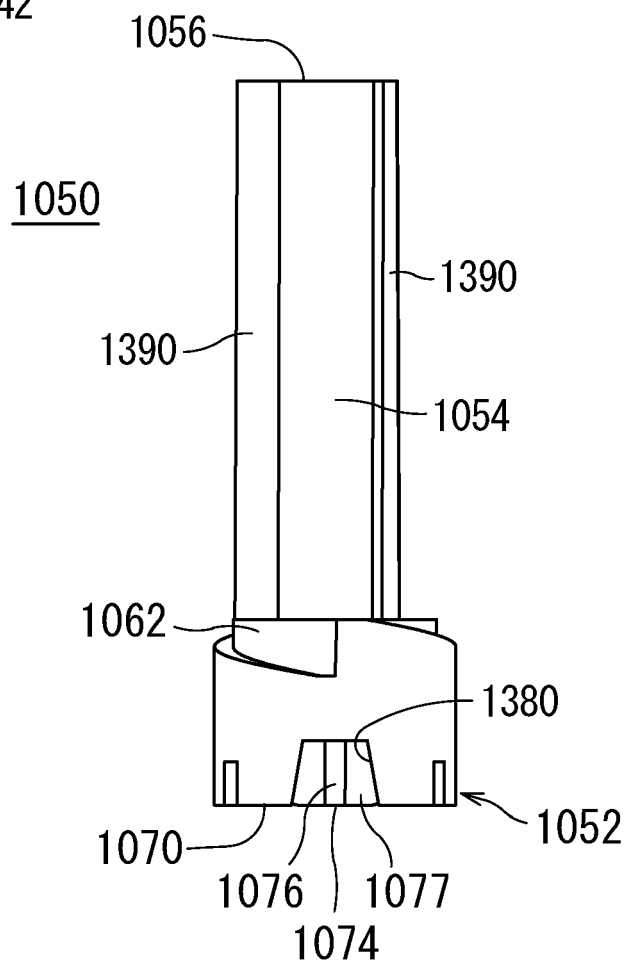
[図41]

図41



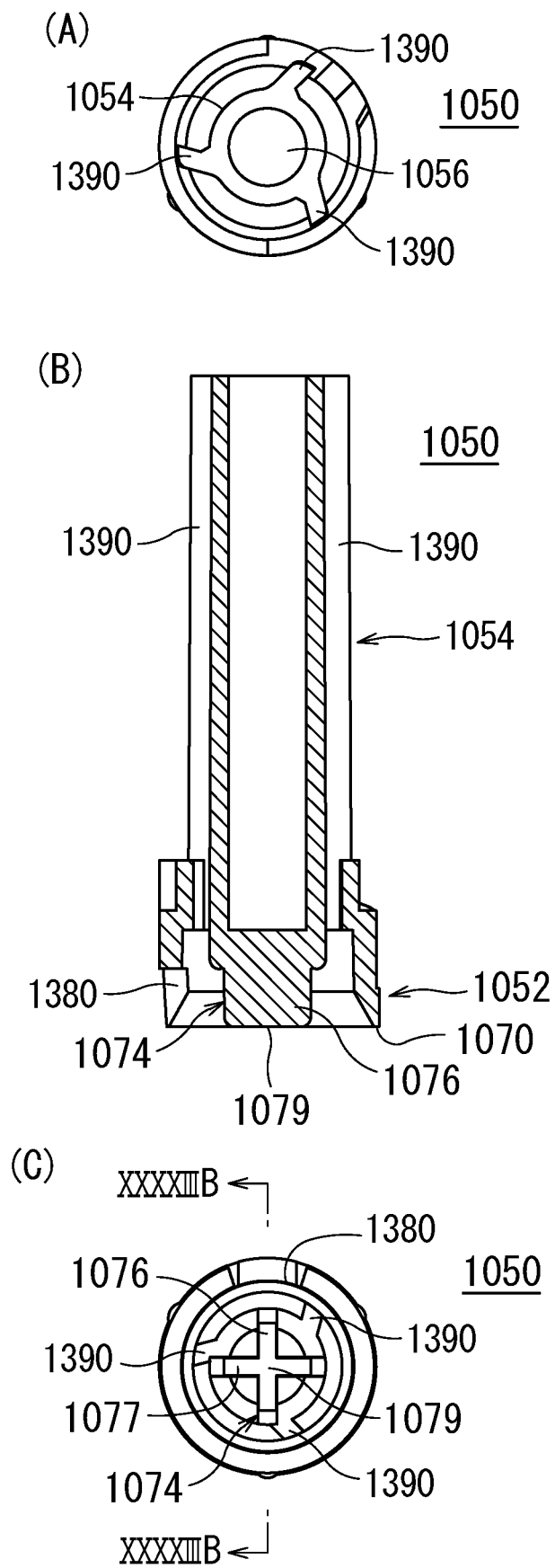
[図42]

図42



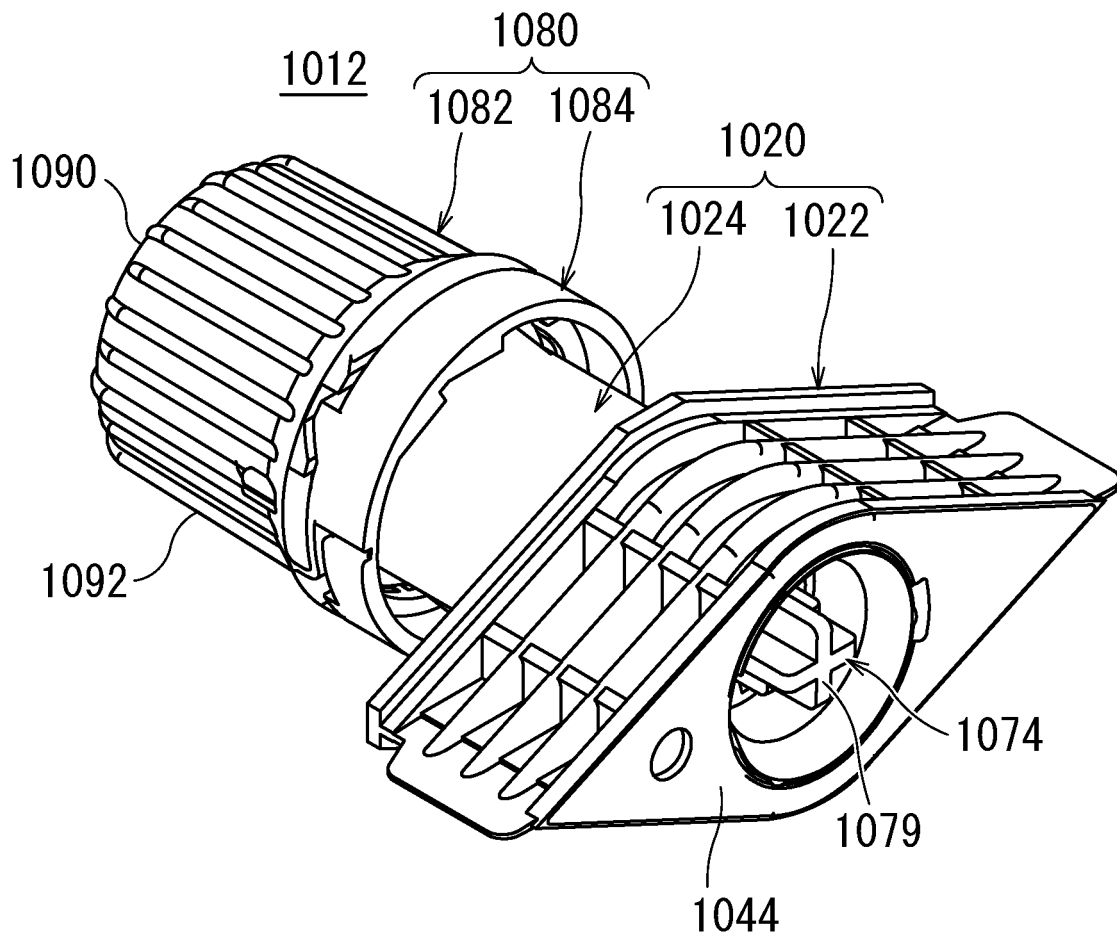
[図43]

図43



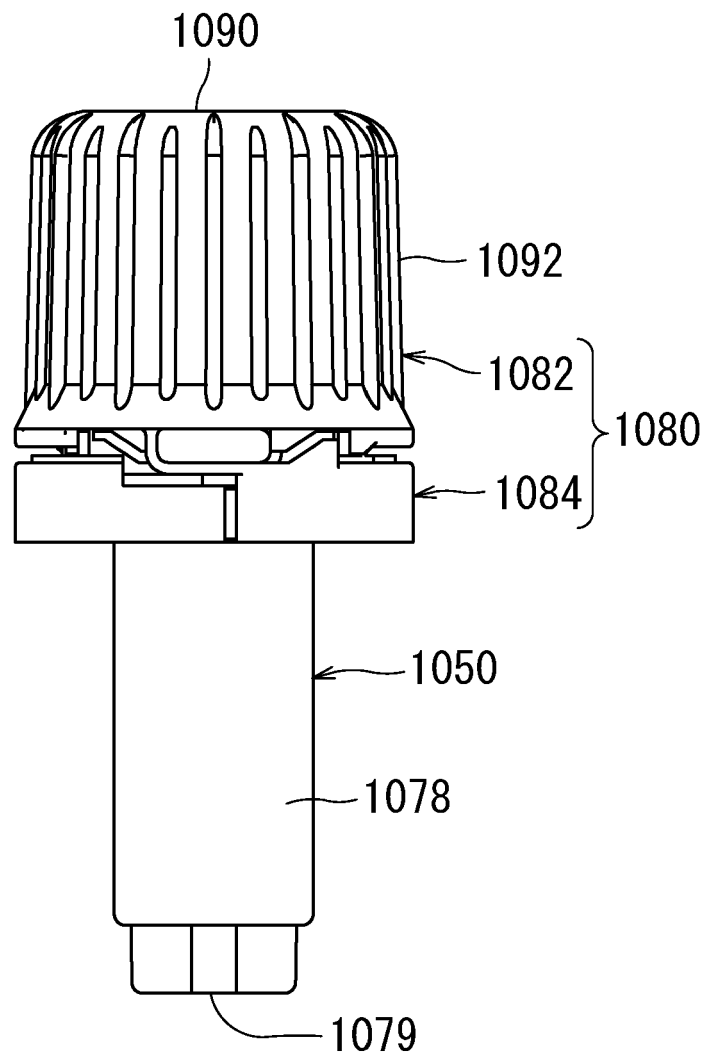
[図44]

図44



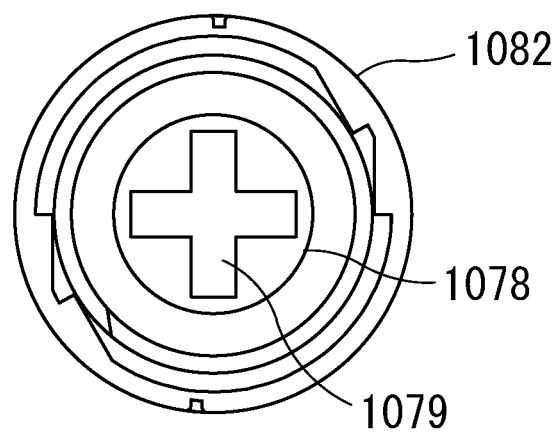
[図45]

図45



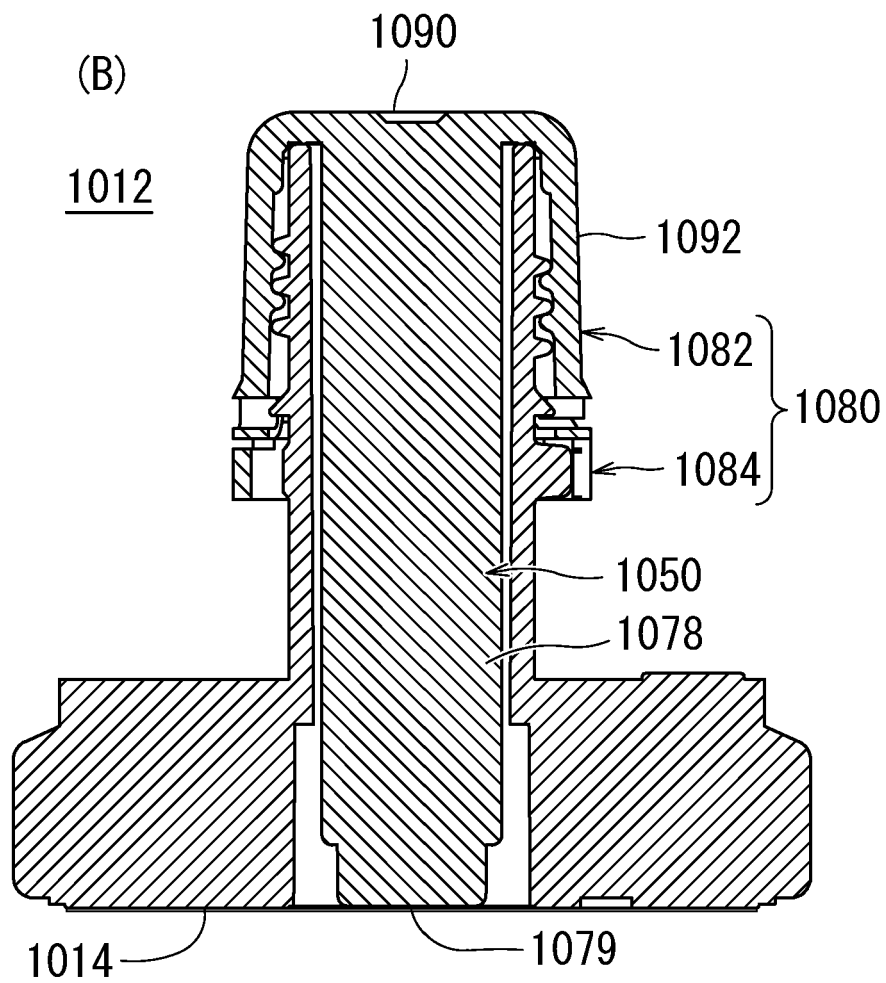
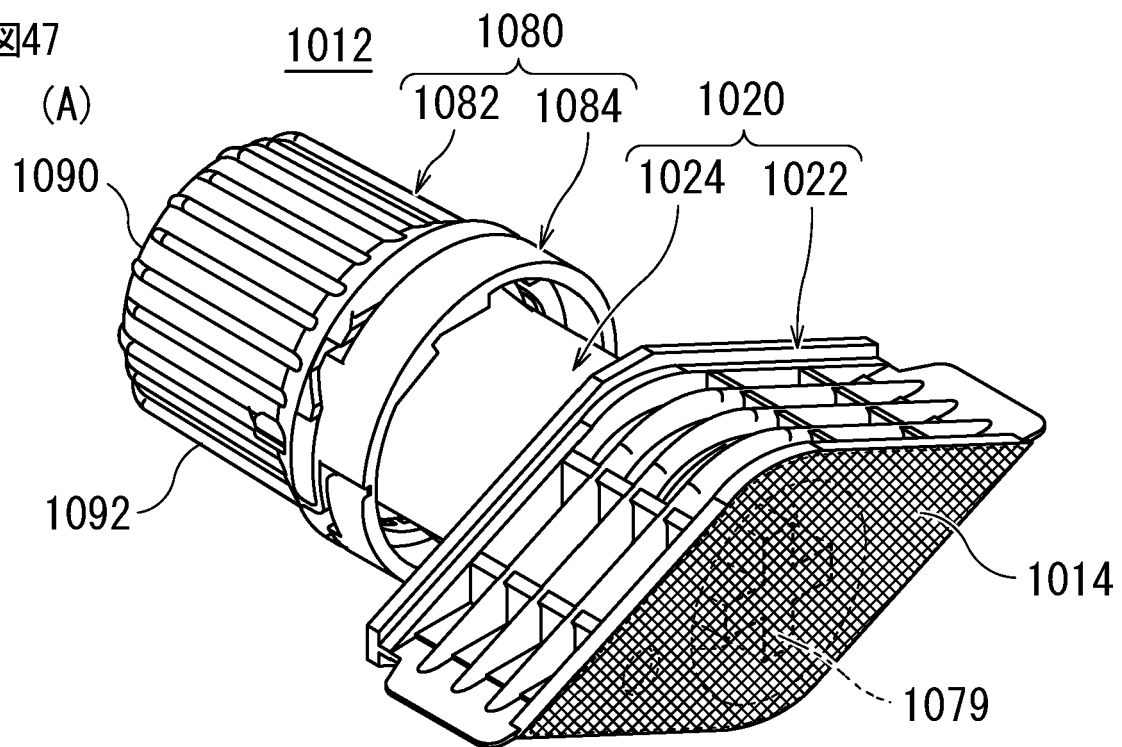
[図46]

図46



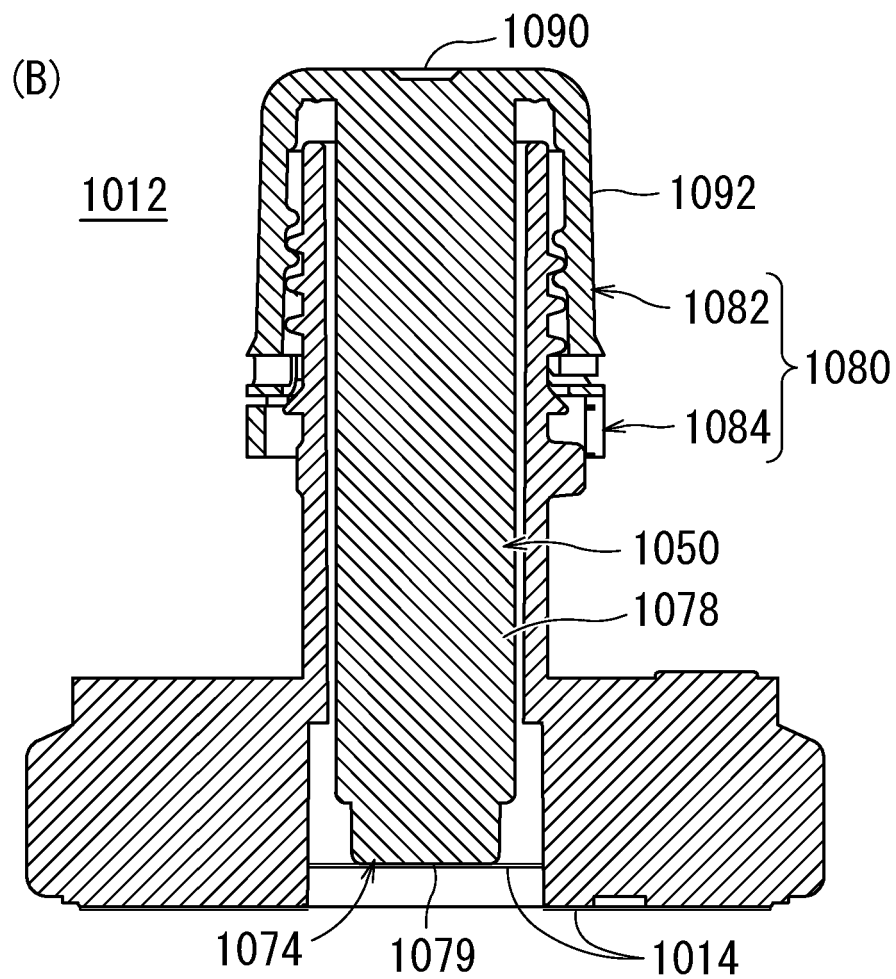
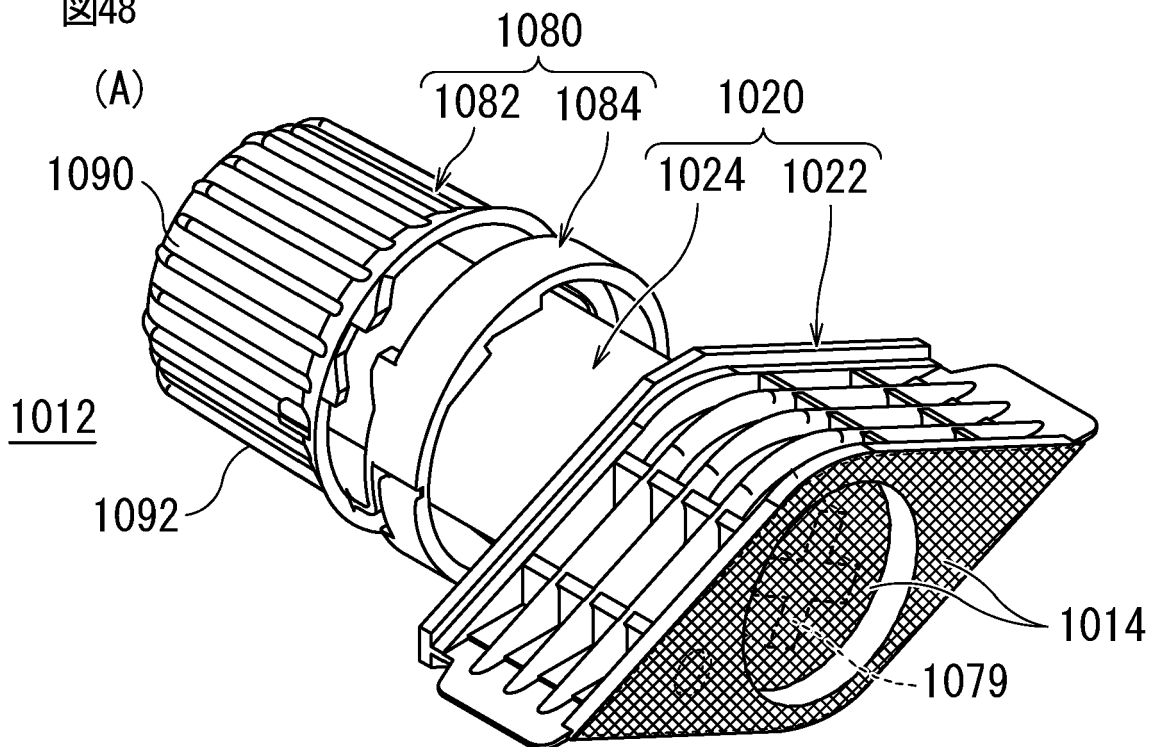
[図47]

図47



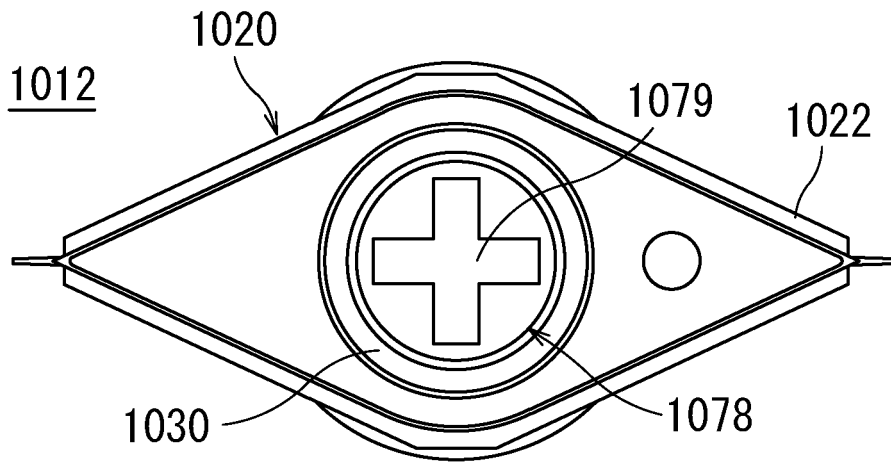
[図48]

図48



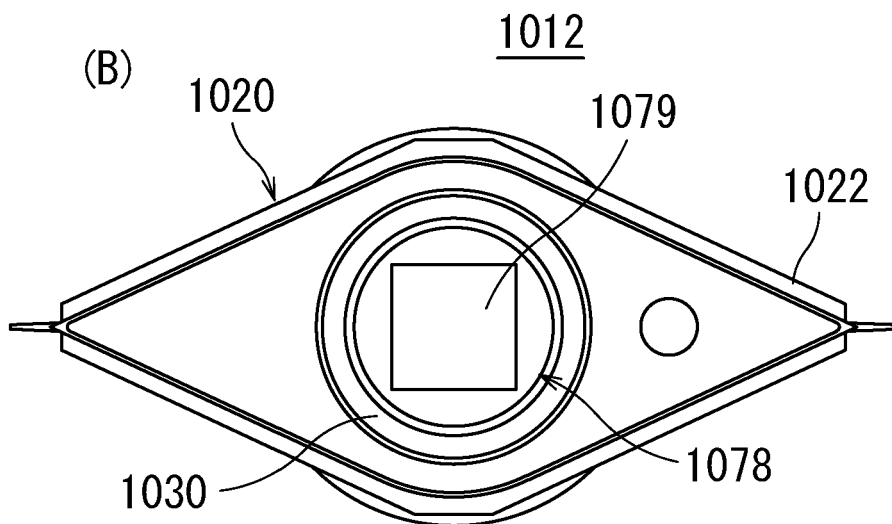
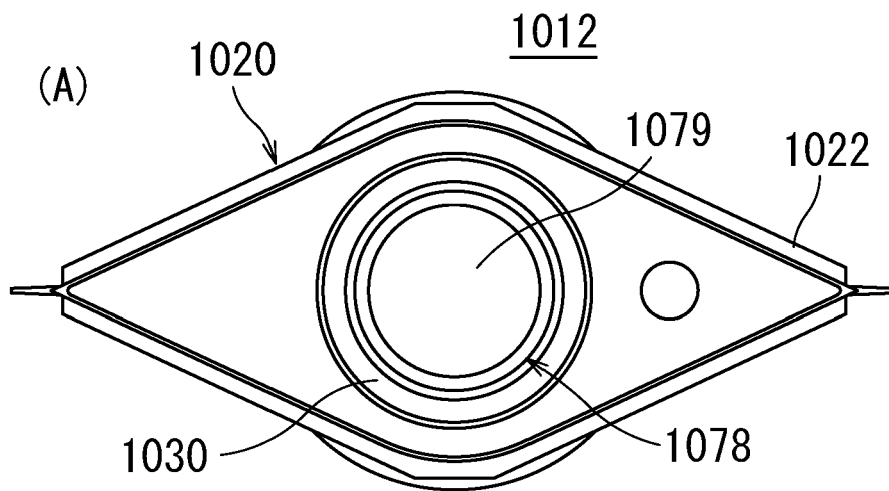
[図49]

図49



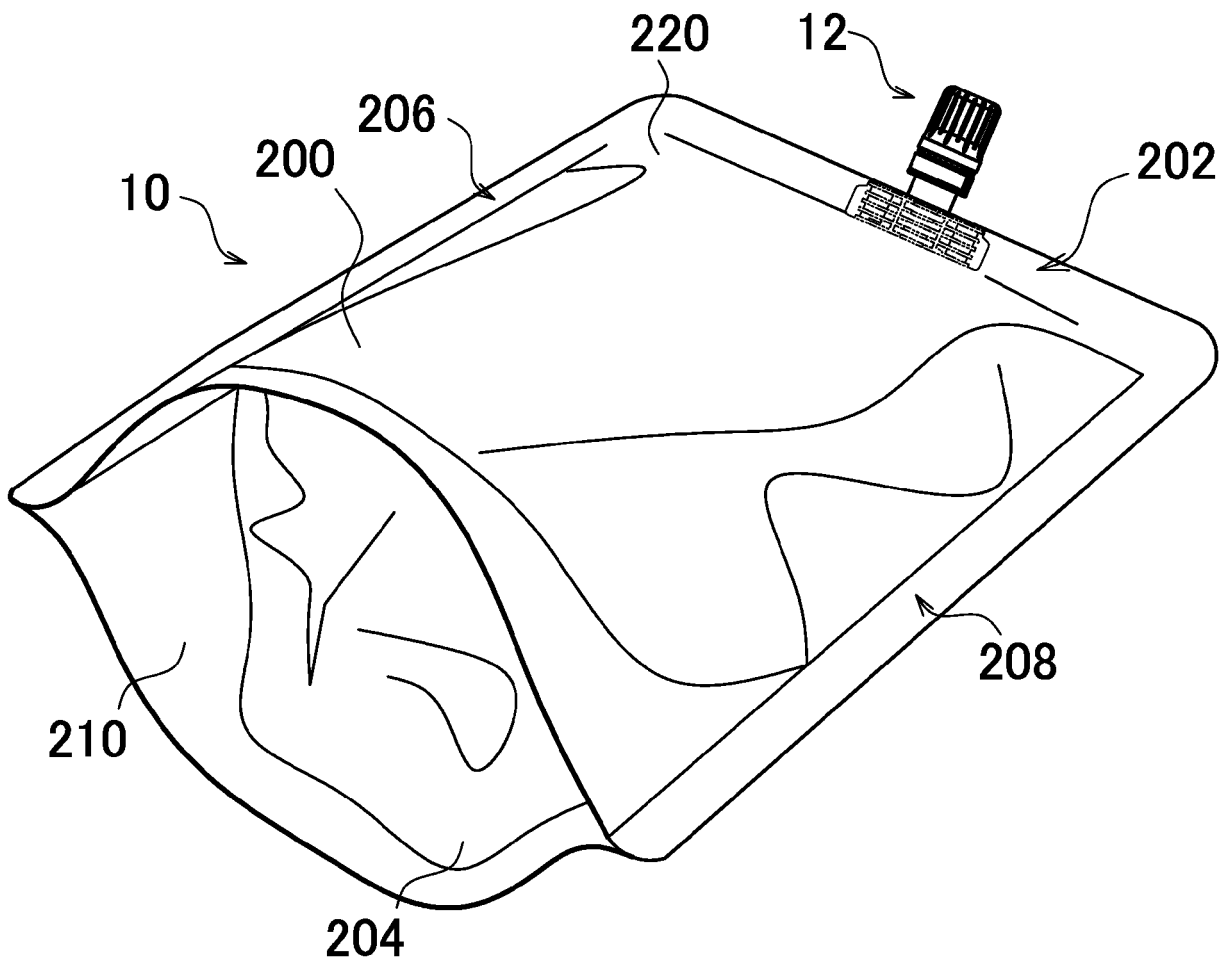
[図50]

図50



[図51]

図51



[図52]

図52

