

CLAIMS:

1. An apparatus comprising:
a substrate;
a first die coupled to the substrate over the substrate, the first die including a power
5 supply circuit coupled to the substrate to receive power;
a second die having a processing core and coupled to the first die over the first die, the
first die being coupled to the power supply circuit to power the processing core; and
a passive device attached to the first die and coupled to the power supply circuit.
2. The apparatus of Claim 1, wherein the first die has a front side including circuitry
10 facing the substrate and a back side facing the second die and wherein the passive device is
positioned on the back side.
3. The apparatus of Claim 2, wherein the front side of the first die is coupled to the
second die using through silicon vias through the first die.
4. The apparatus of Claim 2, wherein the back side of the first die is coupled to the
15 substrate using bonding wires.
5. The apparatus of Claim 1, wherein the first die has a front side including circuitry
facing the second die and a back side facing the substrate and wherein the passive device is
positioned over the front side of the first die.
6. The apparatus of Claim 5, wherein the first die is connected to the second die
20 using solder bumps and wherein the passive device is positioned on the front side of the first die
between the solder bumps.
7. The apparatus of Claim 5, wherein the first die is connected to the second die
using either micro-bump, molded stud, thermosonic, or thermo-compression bonds and wherein
the passive device is positioned on the front side of the first die between the bonds.
8. The apparatus of Claim 6, wherein the front side of the first die has a recess
25 between the solder bumps and wherein the passive device is positioned inside the recess.
9. The apparatus of Claim 8, wherein the recess has a bottom floor and side walls,
wherein the side walls are tapered in towards the bottom floor, and wherein the passive device
has a magnetic layer on the tapered side walls.
10. The apparatus of Claim 1, wherein the first die is a silicon die and wherein the
30 passive device is an inductor with magnetic material formed on a surface of the silicon die.
11. The apparatus of Claim 1, wherein the passive device includes capacitors coupled
to inductors, the capacitors being formed on a surface of the first die.
12. The apparatus of Claim 11, wherein the first die is a silicon die and wherein the
35 capacitors are metal-insulator-metal capacitors.
13. The apparatus of Claim 11, wherein the passive device comprises either 3D
metal-insulator-metal capacitors, planar metal-insulator-metal capacitors, magnetic core
inductors, stripe inductors, spiral inductors, solenoid inductors, or torus inductors.

14. The apparatus of Claim 1, wherein the substrate comprises power decoupling capacitors coupled between an external power supply and the power supply circuit.

15. The apparatus of Claim 1, wherein the power supply circuit comprises either a voltage converter, a switched capacitor voltage converter, a voltage regulator or a fully integrated voltage regulator.

16. A stacked die package comprising:

a cores die having a plurality of processing cores;

an uncore die having a power supply circuit for each processing core, each power supply circuit being independently coupled to each respective processing core to supply power to the respective processing core;

a package substrate coupled to the uncore die to receive power from an external source and to provide power to the power supply circuits of the uncore die;

a plurality of through silicon vias through the uncore die to carry data signals from the cores die to the package substrate; and

a plurality of passive devices attached to the uncore die between the uncore die and the uncore die each coupled to a power supply circuit.

17. The stacked die package wherein the uncore die has a front side facing the cores die and wherein the plurality of passive devices are capacitors attached to the front side of the uncore die.

18. A computing device comprising:

a system board;

a communication package connected to the system board; and

a processor package having a substrate, an uncore die coupled to the substrate over the substrate, the uncore die including a power supply circuit coupled to the substrate to receive power, a cores die having a processing core and coupled to the uncore die over the uncore die, the uncore die being coupled to the power supply circuit to power the processing core, and a passive device attached to the uncore die and coupled to the power supply circuit.

19. The device of Claim 18, wherein the uncore die has a front side including circuitry facing the cores die and a back side facing the substrate, wherein the passive device is positioned in a recess in the front side of the uncore die.

20. The device of Claim 18, wherein the uncore die has a front side facing the substrate and a front side facing the cores die, wherein the passive device is attached to the back side of the die, wherein the power supply circuit is formed on the front side of the uncore die and coupled to the passive device and to the cores die through vias through the back side of the uncore die.