

TRIPLE RAIL LOGIC GATE.BACKGROUND OF THE INVENTION1. FIELD OF THE INVENTION:

The present invention relates to digital logic gates, and more particularly, to improved AND and OR gates having a plurality of inputs, which may be used in a variety of circuit applications.

2. ART BACKGROUND:

In many computer systems, it is necessary to utilize AND or OR gates as part of a digital circuit. Typically, the use of an AND or OR gate within a circuit does not adversely impact the speed of the circuit, since the number of inputs into the particular logic gate is small. However, in the case where a logic gate must detect whether one of tens or hundreds of inputs are either high or low, the digital logic comprising the gate may take hundreds of nanoseconds to make the determination. The use of an AND or OR gate having tens or hundreds of inputs may significantly impact the speed of the digital circuit, and create a bottleneck to efficient circuit operation due to the length of time which the gate takes to generate an output.

As will be described, the present invention provides improved AND and OR gates which may be used in a variety of circuits requiring large numbers of inputs into the logic gate. The present invention's triple rail structure permits the logical AND or OR functions to be completed very quickly using a single logic gate, and significantly improves system performance time.

SUMMARY OF THE INVENTION

According to the present invention there is provided an improved OR gate, comprising:

- a drive rail line;
- a sense rail line;
- a reference rail line;

First transistor means coupled between said drive rail and said sense rail for selectively permitting current to pass between said drive and sense rails;

a plurality of input lines, each of said input lines coupled to a gate of said first transistor means, respectively, such that if an input line is in a first state the transistor to which said input line is coupled passes current;

second transistor means coupled between a known voltage source (V_{dd}) and said sense rail;

third transistor means coupled between said voltage source (V_{dd}) and said reference rail, said third transistor means being sized to pass less current than said second transistor means;

Fourth transistor means coupled between said drive rail and ground;

detection signalling means for generating a detect signal and providing said signal to the gates of said second, third and fourth transistor means, the receipt of said signal resulting in the passage of current through said second, third and fourth transistor means;

sensing means coupled to said sense and

reference rails for sensing the voltage on said rails and generating a predetermined output if the voltage on one of said rails exceeds the voltage on the other.

Also according to the present invention there is provided an improved AND gate comprising:

- a drive rail line;
- a sense rail line;
- a reference rail line;

first transistor means coupled between said drive and sense rails for selectively permitting current to pass between said drive and sense rails;

a plurality of input lines, each of said input lines coupled to a gate of said first transistor means, respectively, such that if an input line is in a first state the transistor to which said input line is coupled passes current;

second transistor means coupled between said drive rail line and a known voltage (V_{dd});

third transistor means coupled between said sense rail and ground,

fourth transistor means coupled between said reference rail and ground, said fourth transistor means being sized to pass less current than said third transistor means;

detection signalling means for generating a detect signal and providing said signal to the gates of said second, third and fourth transistor means, the receipt of said signal resulting in the passage of current through said second, third and fourth transistor means;

sensing means coupled to said sense and reference rail lines for sensing the voltage on said rails and generating a predetermined output if the voltage on one of said rails exceed the voltage on the other.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic illustration of a prior art OR gate having
5 **100 inputs.**

Figure 2 is is a schematic illustration of the present invention's
10 **triple rail OR gate.**

Figure 3 is a timing diagram illustrating the state of various lines
15 **comprising the OR gate of Figure 2 in the event that no input is high.**

Figure 4 is a timing diagram illustrating the state of various lines
20 **of the OR circuit of Figure 2 in the event at least one input is high.**

Figure 5 is a schematic illustration of an AND gate utilizing the
25 **teachings of the present invention.**

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DETAILED DESCRIPTION OF THE INVENTION

An improved multi-input logic gate is disclosed having particular application for use as a OR or AND gate in a digital circuit. In the following
5 description, for purposes of explanation, specific transistors, circuit devices, circuit architectures and components are set forth in order to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known circuits and devices are
10 shown in schematic form in order not to obscure the present invention unnecessarily.

With reference to Figure 1, a prior art OR gate is disclosed which employs multiple inputs denoted as I_n 100 through I_n 199. For purposes of this Specification, the prior art OR circuit of Figure 1 is described with reference to
15 100 inputs, however, the description of the operation of this prior art circuit may be generalized to an OR circuit having N inputs. As illustrated, each input (for example, input 100) is coupled to the gate of a P-channel transistor 300 as well as the gate of an N-channel transistor 302. The output of the prior art circuit of Figure 1 is high if any one of the inputs is high, and will go low only if all of the
20 inputs are low. In operation, the P-channel transistors 300 are turned off, such that no current passes through them, when the input to the gate is high. Conversely, the N-channel transistors 302 are turned off (no current passing therethrough) when the input to the N-channel transistor's gate is low. Accordingly, in the case where all inputs are low, P-channel transistors 300
25 are all turned on, and they permit current to pass therethrough from source V_{dd} . N-channel transistors 302 would then be off and the output of the circuit of Figure 1 due to the presence of inverter 304 is low.

In the event that any one of the inputs (I_n 100 through I_n 199) are high, the P-channel transistor coupled to the high input line is turned off, and
30 the corresponding N-channel transistor for the high input line is turned on. The enabling of an N-channel transistor results in the circuit of Figure 1 pulled low

to ground, and the output of inverter 304 high. It will be appreciated, however, that if all inputs are once again pulled low, a significant amount of time must elapse before enough current is provided through the P-channel transistors 300 from V_{dd} to charge the input to the inverter 304 to a valid high state. It has been
5 estimated that many hundreds of nanoseconds may elapse prior to the OR gate of Figure 1 stabilizing through the 200 transistors (P and N-channel) illustrated in the Figure. Although the circuit may be brought to a low state very quickly because current need only flow through one transistor to get to ground, in order to achieve a high state where all inputs are low, the current must go through all
10 100 transistors illustrated in Figure 1. It has been found that the use of an OR gate as illustrated in Figure 1 significantly impacts the speed of modern digital circuits, and particularly, digital circuits incorporated within high speed data processing equipment. As will be described, the present invention provides improved OR and AND gates which have particular application in high speed
15 digital circuits employed in computer equipment, and overcome the limitations of prior art system illustrated in Figure 1.

Referring now to Figure 2, the present invention's OR gate is illustrated in schematic circuit form. As shown, the OR gate includes a drive rail 310, a sense rail 315 and a reference rail 320. The drive rail 310 and sense rail
20 315 are coupled between the source and drain of N-channel transistors Q_1 through Q_n . Inputs I_1 through I_n are coupled, as shown, to the gates of the N-channel transistors Q_1 through Q_n , respectively. A plurality of dummy transistors Q_d are coupled between the reference rail 320 and ground in order to equalize the capacitances of the rails 310, 315 and 320. Drive rail 310 is
25 coupled to the drain of transistor Q_p 352, sense rail 315 is coupled to the drain of transistor Q_p 354, and reference rail 320 is coupled to the drain of transistor Q_p 356. The source of transistors Q_p 352, Q_p 354 and Q_p 356 are coupled to voltage source V_{dd} . In addition, N-channel transistors Q_{equal} are coupled between the drive rail 310, sense rail 315 and reference rail 320 as shown, and
30 a precharge line 360 is coupled to the gates of Q_p 352, Q_p 354, Q_p 356 and the Q_{equal} transistors.

P-channel transistor Q₃₆₂ is coupled between voltage source V_{dd} and sense rail 315, and P-channel transistor Q₃₆₄ is coupled, as shown between voltage source V_{dd} and reference rail 320. As will be described more fully below, transistor Q₃₆₂ is sized such that it passes more current than transistor Q₃₆₄. A sense amplifier 366 is coupled to the reference rail 320 and sense rail 315. Sense amplifier 366 acts as a differential amplifier such that its output 370 goes to the state which is indicated by the difference between voltages on reference rail 320 and sense rail 315. A detect line 375 is coupled to an inverter 380 which is in turn coupled to the gates of P-channel transistors Q₃₆₂ and Q₃₆₄, and the enable port of sense amp 366. Detect line 375 is further coupled to the gate of N-channel transistor Q₃₈₂ the source of which is coupled to drive rail 310 and the drain of which is coupled to ground.

Referring now to Figures 2, 3, and 4, the operation of the OR circuit of the present invention will be described. Precharge line 360 is driven high such that transistors Q_{p 352}, Q_{p 354}, Q_{p 356}, and the two Q_{equal} transistors are turned on, thereby permitting current to pass therethrough. Accordingly, drive rail 310, sense rail 315, and reference rail 320 are driven high and are equalized to the same voltage. Due to the structure of the circuit illustrated in Figure 2, the voltage of drive rail 310, sense rail 315 and reference rail 320 will stabilize in accordance with the equation $V = V_{dd} - V_{th}$, where V_{th} equals the threshold voltage of the particular MOS transistor devices used. Typically, the value of V_{th} equals approximately .6 volts, and the voltage on the drive rail, sense rail and reference rail approximately equals V_{dd}/2. As illustrated in the timing diagrams of Figures 3 and 4, subsequent to the precharge period, the inputs I₁ through I_n are applied and permitted to stabilize for a predetermined amount of time. A detect signal is provided on line 375 which turns transistor Q₃₈₂ to on, as well as transistors Q₃₆₂ and Q₃₆₄. It will be appreciated that by permitting current to pass through transistor Q₃₈₂, drive rail 310 is immediately pulled low to ground. In the event that all of inputs I₁ through I_n are low, then transistors Q₁ through Q_n remain off. As previously described, transistor Q₃₆₂ is sized such that it passes a greater amount of current than transistor Q₃₆₄. Upon the application of a detect

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signal on line 375, transistors Q362 and Q364 are turned on pulling the sense rail 315 and reference rail 320 toward the V_{DD} voltage. As best shown in Figure 3, the voltage on the sense rail increases slightly faster, due to the sizing of the transistor Q362, then that of the reference rail. Sense amp 366 senses a higher
5 voltage on the sense rail and outputs a low signal indicating that no inputs were high.

Assume for sake of an example that one of the inputs (I₁ through I_n) to the circuit of Figure 2 is high. Subsequent to the precharge of drive rail 310, sense rail 315 and reference rail 320, as described above, the application of the input
10 signals to transistors Q₁ through Q_n would result in one of the inputs (for example, input I₃) to be high. Accordingly, N-channel transistor Q₃ would be turned on. The application of a detect signal on line 375 turning on transistors Q382, Q362 and Q364, results in drive rail 310 being pulled low to ground along with sense rail 315 through transistor Q₃. As illustrated in Figure 4, and as in the case
15 previously described above, transistor Q364 pulls the reference rail 320 toward a higher voltage V_{DD} such that the sense amp 366 senses that the reference rail voltage is higher than the sense rail voltage and outputs a signal on line 370, indicating that at least one of the inputs (I₁ through I_n) is high, and the output for the OR gate is therefore high (or true). It will be appreciated that if more than one of
20 the inputs is high, then the sense rail 315 is pulled toward ground at a faster rate than if only a single input is high. It has been found that the present invention provides a significant increase in speed for determining an OR function, and, as will be described below, an AND function as well.

Referring now to Figure 5, the present invention is illustrated as an AND
25 logic gate, and includes a drive rail 400, a sense rail 410 and a reference rail 415. Inputs to the AND gate of Figure 5 (I₁ through I_n) are coupled to the gates of P-channel transistors Q_{p1} through Q_{pn}, which are in turn coupled between drive rail 400 and the sense rail 410. A plurality of dummy transistors Q_d are coupled between the reference rail 415 and V_{DD} in order to equalize the capacitances of
30 the rails 400, 410 and 415. A P-channel transistor Q_{p 420} is coupled to the drive rail 400 and to V_{DD} as illustrated in Figure 5. A predischARGE circuit is also

provided, and includes an inverter 425 coupled to line 426. P-channel transistors Q_p 428, Q_p 430 and Q_p 432 are coupled to the drive, sense and reference rails, respectively, and to ground. P-channel equalizing transistors Q_{pe} are coupled between the drive rail 400, sense rail 410 and reference rail 415, as shown, with the gates of the transistors Q_{pe}, Q_p 428, Q_p 430 and Q_p 432 coupled to line 426. A detect circuit includes an inverter 440 coupled to line 442. Line 442 is coupled to the gate of transistor Q_p 420 and through inverter 444 to the gates N-channel transistors Q_n 448 and Q_n 450. As illustrated, the transistor Q_n 448 is coupled between the sense rail 410 and ground, and transistor Q_n 450 is coupled between the reference rail 415 and ground. Both the sense rail 410 and reference rail 415 are coupled to a sense amplifier 480 which is enabled by detect line 442.

In operation, driving the predischage line high results in a low signal on line 426 after passing through the inverter 425. The low signal on line 426 acts to turn on transistors Q_p 428, Q_p 430, and Q_p 432, as well as the equalizing transistors Q_{pe}. It will be appreciated, that since transistors are normally off when the gate state is high, that Q_p 420, in the absence of a detect signal, is off. It will further be appreciated that since transistors Q_{pe} are on, during the predischage phase, that the drive rail 400, sense rail 410 and reference 415 are discharged to a threshold voltage above ground. At the end of the predischage phase, line 426 turns off transistors Q_p 428, Q_p 430, Q_p 432 and the equalizing transistors Q_{pe}. The input signals are then applied to inputs I₁ through I_n and permitted it to stabilize.

The driving of the detect line high results in a low signal on line 442 after passing through inverter 440, which results in transistor Q_p 420 being turned on, thereby allowing current to flow from voltage source V_{dd} onto the drive rail 400. In addition, the application of a low signal on line 442 results in N-channel transistors Q_n 448 and Q_n 448 and Q_n 450 to be turned on, thereby pulling sense rail 410 and reference rail 415 low toward ground. In the present invention illustrated in Figure 5, transistor Q_n 448 is sized to pass more current than transistor Q_n 450, such that the voltage on sense rail 410 will move toward a ground state faster than

the voltage on reference rail 415. As is well known, an AND gate requires that the output 480 of sense amp 460 be high only when all the inputs to the AND gate are high, all other input states resulting in a low signal from the sense amp 460. It will be appreciated that in the event that any one of the inputs I_1 through I_n are low, then an AND condition does not exist. The current passing through the drive rail 400 will be passed to the sense rail 410 bringing its voltage to a higher value than the reference rail, which when sensed by the sense amp 460 results in a low output on line 480 indicating that an AND condition does not exist.

Accordingly, an improved OR and AND gate has been disclosed which permits high speed logic functions to be completed. The present invention has particular application for use in high speed digital computer environments, and may be incorporated into a variety of digital circuitry. Although the present invention has been described with reference to Figures 1 through 5, it will be appreciated by one skilled in the art that the figures are for illustration only, and do not serve as limitations on the invention.



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CLAIMS

5 1. An improved OR gate, comprising:
 a drive rail line;
 a sense rail line;
 a reference rail line;
 first transistor means coupled between said drive rail and said sense
10 rail for selectively permitting current to pass between said drive and sense rails;
 a plurality of input lines, each of said input lines coupled to a gate of
 said first transistor means, respectively, such that if an input line is in a first state
 the transistor to which said input line is coupled passes current;
 second transistor means coupled between a known voltage source
15 (V_{dd}) and said sense rail;
 third transistor means coupled between said voltage source (V_{dd})
 and said reference rail, said third transistor means being sized to pass less current
 than said second transistor means;
 fourth transistor means coupled between said drive rail and ground;
20 detection signaling means for generating a detect signal and
 providing said signal to the gates of said second, third and fourth transistor means,
 the receipt of said signal resulting in the passage of current through said second,
 third and fourth transistor means;
 sensing means coupled to said sense and reference rails for
25 sensing the voltage on said rails and generating a predetermined output if the
 voltage on one of said rails exceeds the voltage on the other.

 2. The OR gate as defined by claim 1, further including
30 precharge means coupled to said drive, sense and reference rails for selectively
 charging said rails to a known state prior to the generation of said detect signal.

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3. The OR gate as defined by claim 2, wherein said first transistor means comprises transistors, at least one transistor for each of said
5 input lines.

4. The OR gate as defined by claim 3, further including fifth transistor means coupled to said reference rail for equalizing the capacitance of
10 said reference rail and said sense rail.

5. The OR gate as defined by claim 3, wherein said sensing means comprises a sense amplifier.
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6. The OR gate as defined by claim 5, wherein said precharge means includes sixth transistor means coupled between said drive rail, sense rail and reference rail to equalize the voltage on said rails.
20

7. The OR gate as defined by claim 6, wherein said precharge means further includes:

seventh transistor means coupled between said voltage source
25 V_{dd} and said drive rail, sense rail and reference rail, respectively;

a precharge line coupled to said sixth and seventh transistor means, such that if a precharge signal is provided on said precharge line, said sixth and seventh transistor means turn on and pass current therethrough.



8. The OR gate as defined by claim 7, wherein said sixth and seventh transistor means comprises N-channel transistors.

5 9. The OR gate as defined by claim 6, wherein said first transistor means comprise N-channel transistors.

10 10. The OR gate as defined by claim 6, wherein said fourth transistor means comprises an N-channel transistor.

11. The OR gate as defined by claim 6, wherein said second and third transistor means comprises P-channel transistors.

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12. The OR gate as defined by claim 6, further including an inverter coupled between said detection signalling means and the gates of said second and third transistor means.

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13. The OR gate as defined by claim 2, wherein said known state is approximately $V_{dd} - V_{th}$, where V_{th} equals the threshold voltages of said sixth and seventh transistor means.

25



14. An improved AND gate comprising:

a drive rail line;

a sense rail line;

a reference rail line;

5 first transistor means coupled between said drive and sense rails for selectively permitting current to pass between said drive and sense rails;

a plurality of input lines, each of said input lines coupled to a gate of said first transistor means, respectively, such that if an input line is in a first state the transistor to which said input line is coupled passes current;

10 second transistor means coupled between said drive rail line and a known voltage (V_{dd});

third transistor means coupled between said sense rail and ground;

fourth transistor means coupled between said reference rail and ground, said fourth transistor means being sized to pass less current than said
15 third transistor means;

detection signalling means for generating a detect signal and providing said signal to the gates of said second, third and fourth transistor means, the receipt of said signal resulting in the passage of current through said
second, third and fourth transistor means;

20 sensing means coupled to said sense and reference rail lines for sensing the voltage on said rails and generating a predetermined output if the voltage on one of said rails exceed the voltage on the other.

25 15. The AND gate as defined by claim 14, further including predischARGE means coupled to said drive, sense and reference rails for selectively discharging said rails to a threshold level above ground prior to the generation of said detect signal.



16. The AND gate as defined by claim 15, wherein said first transistor means comprises transistors, at least one transistor for each of said input lines.

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17. The AND gate as defined by claim 16, wherein said sensing means comprises a sense amplifier.

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18. The AND gate as defined by claim 17, wherein said predischage means includes fifth transistor means coupled between said drive rail, sense rail and reference rail to equalize the voltage on said rails.

15

19. The AND gate as defined by claim 18, wherein said predischage means further includes:

sixth transistor means coupled between said drive, sense and reference rails and ground;

20 such that if a predischage signal is provided on said predischage line, said fifth and sixth transistor means turn on and bring said drive, sense and reference rails to a threshold state above ground.

25

20. The AND gate as defined by claim 19, wherein said first transistor means comprises P-channel transistors.

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21. The AND gate as defined by claim 20, wherein said second transistor means comprises at least one P-channel transistor.



22. The AND gate as defined by claim 21, wherein said third and fourth transistor means comprise N-channel transistors.

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23. The AND gate as defined by claim 22, further including seventh transistor means coupled to said reference rail for equalizing the capacitance of said reference rail and said sense rail.

10

24. The AND gate as defined by claim 23, wherein said fifth and sixth transistor means comprise P-channel transistors.

25. An improved logic gate substantially as hereinbefore described with reference to the accompanying drawings except figure 1.

