CLAIMS

1. An apparatus, comprising: a memory device, comprising: a plurality of memory cells; and a partial array refresh (PAR) mask register, wherein when the memory device is in a self-refresh (SR) mode and a partial array self-refresh (PASR) is enabled, the memory device is configured to internally refresh a subset of the plurality of memory cells selected in accordance with the PAR mask register without receiving a refresh (REF) command, and wherein a value of the PAR mask register is externally settable through a mode register write (MRW) command.

2. The apparatus of claim 1, further comprising a system-on-chip (SOC) configured to provide commands to the memory device over a link, wherein the memory device is configured to enter the SR mode upon receiving a self-refresh-enter (SRE) command from the SOC and exit the SR mode upon receiving a self-refresh-exit (SRX) command.

3. The apparatus of claim 2, wherein the apparatus comprises a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop computer, a server, and a device in an automotive vehicle, and wherein the device incorporates the memory device and the SOC configured to communicate with each other over the link.

4. The apparatus of claim 2, wherein the memory device further comprises an input/output (I/O) circuit configured to interface with the SOC over the link, and write data to and read data from the plurality of memory cells, wherein memory device is configured to refresh the subset of the memory cells selected in accordance with the PAR mask register without the I/O circuit receiving refresh (REF) commands from the SOC when the memory device is in the SR mode and the PASR is enabled, and wherein the memory device is configured to refresh the subset of the plurality of memory cells selected in accordance with the PAR mask register upon the I/O circuit receiving the REF command from the SOC when the memory device is not in the SR mode.

5. The apparatus of claim 4, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register comprises a plurality of segment mask bits, each segment mask bit corresponding to a segment indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the memory device is in the SR mode and the PASR is enabled, the memory device is configured to, for each bank, skip the internal refreshing of each segment whose corresponding segment mask bit indicates that the refresh is disabled.

6. The apparatus of claim 4, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask

register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the memory device is in the SR mode and the PASR is enabled, the memory device is configured to skip the internal refreshing of each segment of each bank whose corresponding bank and segment mask bits respectively indicate that the refresh is disabled for that bank and for that segment.

7. The apparatus of claim 4, wherein the plurality of memory cells is partitioned into a plurality of banks, wherein the PAR mask register comprises a plurality of bank mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and wherein when the memory device is in the SR mode and the PASR is enabled, the memory device is configured to skip the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled.

8. The apparatus of claim 4, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the memory device is in the SR mode and the PASR is enabled, the memory device is configured to skip the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled for that bank, and for each bank whose corresponding bank mask bit indicates that the refresh is enabled for that bank, skip the internal refreshing each segment whose corresponding segment mask bit indicates that the refresh is disabled.

9. An apparatus, comprising: a system-on-chip (SOC) configured to communicate with a memory device over a link, wherein the memory device comprises: a plurality of memory cells; and a partial array refresh (PAR) mask register, and wherein the SOC is configured to issue a self-refresh-enter (SRE) and self-refresh-exit (SRX) commands to instruct the memory device to enter into and exit from a self-refresh (SR) mode, and wherein when the memory device is in the SR mode and a partial array self-refresh (PASR) is enabled, the memory device is configured to internally refresh a subset of the memory cells selected in accordance with the PAR mask register without receiving refresh (REF) commands from the SOC.

10. The apparatus of claim 9, wherein the memory device comprises a plurality of mode registers (MR) comprising the PAR mask register and a plurality of enable bits including a PASR enable bit indicating whether the PASR is enabled or disabled.

11. The apparatus of claim 10, wherein the SOC is configured to issue a mode register write

(MRW) command with a corresponding mode value of the PASR enable bit to the memory device, and for each mode register used to implement the PAR mask register, issue the MRW command with the corresponding mode value to the memory device so as to cause a mask value to be written to the PAR mask register, the mask value indicating a refresh skip region comprising one or more portions of the plurality of memory cells that do not require refreshing.

12. The apparatus of claim 11, wherein the SOC is configured to receive the refresh skip region from a memory driver of a computing system, and issue the MRW commands to set the PASR enable bit and to set the mask value indicating the refresh skip region subsequent to receiving the refresh skip region from the memory driver.

13. The apparatus of claim 9, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register comprises a plurality of segment mask bits, each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and when the PASR is enabled, the SRE command issued by the SOC causes the memory device to, for each bank, skip the internal refreshing of each segment whose corresponding segment mask bit indicates that the refresh is disabled upon entering the SR mode.

14. The apparatus of claim 9, wherein the plurality of memory cells is partitioned into a plurality of banks, wherein the PAR mask register comprises a plurality of bank mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and wherein when the PASR is enabled, the SRE command issued by the SOC causes the memory device to skip the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled.

15. The apparatus of claim 9, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the PASR is enabled, the SRE command issued by the SCO causes the memory device to skip the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled for that bank, and for each bank whose corresponding bank mask bit indicates that the refresh is enabled for that bank, skip the internal refreshing each segment whose corresponding segment mask bit indicates that the refresh is disabled.

16. The apparatus of claim 9, wherein the apparatus comprises a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop

computer, a server, and a device in an automotive vehicle, and wherein the device incorporates the memory device and the SOC configured to communicate with each other over the link.

17. A method for reducing memory power consumption in an apparatus of a computing system, wherein the apparatus comprises a system-on-chip (SOC) and a memory device configured to communicate with each other over a link, wherein the memory device comprises: a plurality of memory cells; and a plurality of mode registers (MR) comprising a PAR mask register, a partial array self-refresh (PASR) enable bit indicating whether PASR is enabled or disabled, and wherein the method comprises: issuing, by the SOC, a mode register write (MRW) command with a corresponding mode value of the PASR enable bit to the memory device; issuing, by the SOC, for each mode register used to implement the PAR mask register, a mode register write (MRW) command with a corresponding mode value to the memory device so as to cause a mask value to be written to the PAR mask register, the mask value corresponding to a refresh skip region; issuing, by the SOC, a self-refresh-enter (SRE) command to the memory device; and skipping, by the memory device, an internal refreshing of the refresh skip region based on the PAR mask register when the SRE command is received from the SOC and the PASR enable bit is set.

18. The method of claim 17, wherein the plurality of memory cells is partitioned into a plurality of banks, wherein the PAR mask register comprises a plurality of bank mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and wherein the skipping the internal refreshing comprises skipping the internal refreshing of each bank whose corresponding segment mask bit indicates that the refresh is disabled when the SRE command is received and the PASR enable bit is set.

19. The method of claim 17, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register comprises a plurality of segment mask bits, each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein the skipping the internal refreshing comprises, for each bank, skipping the internal refreshing of each segment whose corresponding segment mask bit indicates that the refresh is disabled when the SRE command is received and the PASR enable bit is set.

20. The method of claim 17, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the SRE command is received and the PASR enable bit is set, the skipping the internal refreshing comprises: skipping the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled for that bank, and for each

bank whose corresponding bank mask bit indicates that the refresh is enabled for that bank, skipping the internal refreshing each segment whose corresponding segment mask bit indicates that the refresh is disabled.

21. An apparatus, comprising: a system-on-chip (SOC) configured to communicate with a memory device over a link, wherein the SOC is configured to provide commands to the memory device over the link including a self-refresh-enter (SRE) and self-refresh-exit (SRX) commands to instruct the memory device to enter into and exit from a self-refresh (SR) mode, wherein the memory device comprises: a plurality of memory cells; a partial array refresh (PAR) mask register; and a built-in timer configured to generate refresh pulses, wherein when the memory device receives the SRE command and a partial array self-refresh (PASR) is enabled, the memory device is configured to internally refresh a subset of the memory cells selected in accordance with the PAR mask register and in accordance with the refresh pulses generated by the built-in timer without receiving refresh (REF) commands from the SOC.

22. The apparatus of claim 21, wherein the plurality of memory cells is partitioned into a plurality of banks, wherein the PAR mask register comprises a plurality of bank mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and wherein the memory device is configured to skip the internal refreshing of each bank whose corresponding segment mask bit indicates that the refresh is disabled when the SRE command is received and the PASR enable bit is set.

23. The apparatus of claim 21, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register comprises a plurality of segment mask bits, each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein the memory device is configured to skip, for each bank, the internal refreshing of each segment whose corresponding segment mask bit indicates that the refresh is disabled when the SRE command is received and the PASR enable bit is set.

24. The apparatus of claim 21, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the SRE command is received and the PASR enable bit is set, the memory device is configured to skip the internal refreshing of each bank whose corresponding bank mask bit indicates that the refresh is disabled for that bank, and for each bank whose corresponding bank mask bit indicates that the refresh is enabled for that bank, skip the internal refreshing each segment whose corresponding segment mask bit indicates that the refresh is disabled.

25. The apparatus of claim 9, wherein the plurality of memory cells is partitioned into a

plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the PASR is enabled, the SRE command issued by the SCO causes the memory device to skip the internal refreshing of each segment of each bank whose corresponding bank and segment mask bits respectively indicate that the refresh is disabled for that bank and for that segment.

26. The method of claim 17, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the SRE command is received and the PASR enable bit is set, the skipping the internal refreshing comprises skipping the internal refreshing of each segment of each bank whose corresponding bank and segment mask bits respectively indicate that the refresh is disabled for that bank and for that segment.

27. The apparatus of claim 21, wherein the plurality of memory cells is partitioned into a plurality of banks, each bank comprising a plurality of segments, wherein the PAR mask register includes a plurality of bank mask bits and a plurality of segment mask bits, each bank mask bit corresponding to a bank and indicating whether a refresh is enabled or disabled for the corresponding bank, and each segment mask bit corresponding to a segment and indicating whether a refresh is enabled or disabled for the corresponding segment, and wherein when the SRE command is received and the PASR enable bit is set, the memory device is configured to skip the internal refreshing of each segment of each bank whose corresponding bank and segment mask bits respectively indicate that the refresh is disabled for that bank and for that segment.