CLAIMS

WHAT IS CLAIMED IS:

1. An apparatus, comprising:

a transistor region of an integrated circuit, the transistor region being above a substrate in a vertical dimension perpendicular to the substrate;

a first metal layer located above the transistor region in the vertical dimension;

a second metal layer located above first metal layer in the vertical dimension;

wherein at least one of the first metal layer and the second metal layer includes power supply routing, ground supply routing, and signal routing; and

a transistor circuit positioned between the first metal layer and the second metal layer in the vertical dimension, wherein the transistor circuit includes:

an active region;

a gate;

a signal input coupled to the gate and a portion of the signal routing;

a voltage supply input for the active region coupled to the power supply routing;

a ground supply input for the active region coupled to the ground supply routing; and

a signal output coupled to an additional portion of the signal routing.

2. The apparatus of claim 1, wherein the transistor circuit is a buffer transistor circuit configured to increase a strength of a signal received at the signal input.

3. The apparatus of claim 1, wherein the transistor circuit is an inverter transistor circuit, the active region including a p-type active region and an n-type active region.

4. The apparatus of claim 3, wherein the transistor circuit further includes local vias between one or more of the gate, the voltage supply input, the ground supply input, and the signal output and one or both of the first and second metal layers.

5. The apparatus of claim 3, wherein the transistor circuit further includes a local interconnect wire between drain regions and gate regions of the active region.

6. The apparatus of claim 1, wherein the power supply routing, the ground supply routing, and the signal routing are oriented in parallel in a horizontal dimension parallel to the substrate, and wherein the active region is positioned between the power supply routing and the ground supply routing in the horizontal dimension.

7. The apparatus of claim 1, further comprising an additional transistor circuit positioned between the first metal layer and the second metal layer in the vertical dimension, wherein the additional transistor circuit includes an additional active region.

8. The apparatus of claim 7, wherein the additional active region is oriented orthogonally to the active region in a horizontal dimension parallel to the substrate.

9. The apparatus of claim 1, wherein the transistor circuit is positioned in a dielectric layer between the first metal layer and the second metal layer.

10. The apparatus of claim 1, wherein the active region is formed by a thin channel material positioned in between the first metal layer and the second metal layer.

11. An apparatus, comprising:

a transistor circuit positioned within a transistor region of an integrated circuit, the transistor circuit being above a substrate in a vertical dimension perpendicular to the substrate;

a first metal layer located above the transistor region in the vertical dimension;

a second metal layer located above the transistor region in the vertical dimension;

wherein at least one of the first metal layer and the second metal layer includes power supply routing, ground supply routing, and signal routing, wherein a portion of the signal routing is coupled to the transistor circuit; and

a buffer transistor circuit positioned between the first metal layer and the second metal layer in the vertical dimension, wherein the buffer transistor circuit includes:

a p-type active region;

an n-type active region;

a gate input coupled to the portion of the signal routing that is coupled to the transistor circuit;

a voltage supply input coupled to a source region in the p-type active region and the power supply routing;

a ground supply input coupled to a source region in the n-type active region and the ground supply routing; and

a gate output coupled to an additional portion of the signal routing.

12. The apparatus of claim 11, wherein the power supply routing, the ground supply routing, and the signal routing are oriented in parallel along a first direction in a horizontal dimension parallel to the substrate.

13. The apparatus of claim 12, wherein the p-type active region and the n-type active region are oriented in parallel along the first direction in the horizontal dimension.

14. The apparatus of claim 12, wherein the buffer transistor circuit includes a gate wire oriented along a second direction in the horizontal dimension, the second direction being perpendicular to the first direction, and wherein the gate wire extends over both the p-type active region and the n-type active region in the vertical dimension.

15. The apparatus of claim 11, wherein the voltage supply input includes:

a metal wire positioned at least partially above the source region in the p-type active region; and

a via coupled between the metal wire and the power supply routing.

16. The apparatus of claim 11, wherein the ground supply input includes:

a metal wire positioned at least partially above the source region in the n-type active region; and

a via coupled between the metal wire and the ground supply routing.

17. The apparatus of claim 11, wherein the buffer transistor circuit includes:

a first gate wire oriented along a direction in a horizontal dimension, wherein the gate wire is positioned at least partially above channel regions of both the p-type active region and the n-type active region in the vertical dimension;

a first stage output wire oriented along the direction, wherein the first stage output wire is

positioned at least partially above drain regions of both the p-type active region and the n-type active region in the vertical dimension; and

a local interconnect wire connected to both ends of the first stage output wire, wherein at least a portion of the local interconnect wire is positioned above the channel regions of both the p-type active region and the n-type active region in the vertical dimension.

18. The apparatus of claim 17, wherein the gate output includes a second stage output wire oriented along a second direction in the horizontal dimension, the second direction being perpendicular to the first direction, wherein the second stage output wire is positioned at least partially above the drain regions of both the p-type active region and the n-type active region in the vertical dimension.

19. The apparatus of claim 11, wherein the buffer transistor circuit is positioned in a dielectric layer between the first metal layer and the second metal layer.

20. An apparatus, comprising:

a transistor region of an integrated circuit, the transistor region being above a substrate in a vertical dimension perpendicular to the substrate;

a first metal layer located above the transistor region in the vertical dimension, wherein the first metal layer includes first power supply routing, first ground supply routing, and first signal routing;

a second metal layer located above the first metal layer in the vertical dimension, wherein the second metal layer includes second power supply routing, second ground supply routing, and second signal routing; and

a first buffer transistor circuit positioned between the first metal layer and the second metal layer in the vertical dimension, wherein the first buffer transistor circuit includes:

a first p-type active region;

a first n-type active region;

a first gate input coupled to a portion of the first signal routing;

a first voltage supply input coupled to a first source region in the first p-type active region and the first power supply routing;

a first ground supply input coupled to a first source region in the first n-type active region and the first ground supply routing; and

a first gate output coupled to an additional portion of the first signal routing; and

a second buffer transistor circuit positioned between the first metal layer and the second metal layer in the vertical dimension, wherein the second buffer transistor circuit includes:

a second p-type active region;

a second n-type active region;

a second gate input coupled to a portion of the second signal routing;

a second voltage supply input coupled to a second source region in the second p-type active region and the second power supply routing;

a second ground supply input coupled to a second source region in the second n-type active region and the second ground supply routing; and

a second gate output coupled to an additional portion of the second signal routing.