English translation of the PCT specification

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF SAME

TECHNICAL FIELD

BACKGROUND OF THE INVENTION

The present invention relates generally to semiconductor devices and manufacturing methodology of the same as well as semiconductor modules, and more particularly to architectures or techniques for fabricating semiconductor elements in the form of being mountable in units of wafers and for subdividing this into necessary sizes to thereby obtain the intended semiconductor devices.

In recent years, as electrical and electronic parts or components are increasing more and more in performance, semiconductor elements have likewise increased in integration density and functionality in a way such that the IC complexity has advanced from large-scale integration (LSI) to very-large-scale integration (VLSI), and finally to ultralarge-scale integration (ULSI). Such technological growth results in further increases in dimension and pin number plus operating rate of the elements involved. To accommodate the technical trend above, package structures for use with multiple-pin semiconductor devices have been shifted from those having

connection terminals at two opposite sides of a semiconductor element to others having connection terminals arrayed along four side edges thereof. Further, in order to meet the needs for multi-pin package schemes, so-called "grid array" structures have been developed and reduced to practice, which are designed to employ a multilayer carrier substrate for permitting required connection terminals to be laid out into a grid-like pattern on the entire area of a parts-mount surface. The grid-array structures typically include a ball grid array (BGA) structure that has presently been employed from time to time, which is arranged so that those terminals used therein are of a ball-like shape to thereby enable achievement of high-speed signal transmission and low inductance. In addition, to attain the high-speed signal transmissivity required, the multilayer carrier substrate made of chosen organic materials have been used which are inherently low in dielectricity than currently available inorganic materials. Unfortunately, use of such organic materials is encountered with many problems as to difficulty of attaining enhanced reliability due to the presence of risks of readily occurrence of electrical connection defects, including unwanted open-circuiting and/or short-circuiting, because of the fact that the organic materials are inherently greater in thermal

expansion coefficient than standard silicon-based materials that have been often employed for semiconductor elements and, for this reason, thermal stresses can take place due to possible differences in thermal expansion coefficient therebetween.

Moreover, in a view point of high-density mounting/packaging design schemes today, a need also exists for a semiconductor device of the chip scale package (CSP) structure type which is substantially the same in size as a semiconductor element associated therewith. One typical known approach to achieving this is to employ a specific structure that eliminates the use of any carrier substrate in the CSP with BGA structures. This is a mount structure permitting direct connection between a semiconductor element and its associated mount substrate or board, and one typical package structure incorporating this principle has been disclosed (in United States Patent No. 5,148,265), which is capable of improving the reliability of connector portions by making use of a chosen material that is low in modulus of elasticity to reduce or "relax" any possible stress forces occurring due to thermal expansion coefficient differences between the semiconductor element and its mount board. This package structure is designed so that the required electrical interconnection between the semiconductor element and the

mount board is done by use of a lead tape made of an organic material such as polyimide or else in the alternative of the carrier substrate. Due to this, wire-bonding techniques or other similar bonding methods using electrical leads are employed for electrical connection portions including external terminals of the semiconductor element and those conductive circuit sections of such lead tape. Additionally ball-like terminals made of solder or the like are used for connection between the lead tape and the mount board's conductive portions. Manufacturing of this structure does require an increased number of new process steps including, but not limited to, the steps of disposing a low-elasticity material at the semiconductor element, connecting the lead tape, forming ball terminals, and then sealing electrical connection portions; accordingly, this approach requires new manufacturing facility while also requiring that the individual one of resultant semiconductor devices be assembled and mounted on a per-chip basis, which would result in association of many disadvantages as to the manufacturability when compared to prior art methods thereby causing the CSP structure's inherent advantages of high-density mountability to be less achievable during reduction to practice.

The present invention has been made in light of the

technical background stated above to provide an improved semiconductor device manufacturing method low in cost and excellent in mass-productivity for enabling by using low-elasticity organic materials reduction or relaxation of thermal stresses occurring between a semiconductor element or elements of grid-array structure accommodatable to multi-pin design schemes and its associative mount substrate or board for fabrication into a specific form mountable in units of wafers to thereby achieve subdivision into necessary sizes, along with a semiconductor device or module excellent in reliability of electrical connection and high-speed signal transmissivity plus multi-pin scheme accommodatability.

SUMMARY OF THE INVENTION

The present invention provides a semiconductor device which comprises a semiconductor element for formation of integrated circuitry, a plurality of electrode pads that is formed on an integrated circuit formation surface side of the semiconductor element, bump electrodes for external connection as electrically connected to the electrode pads through a conductive layer, and a stress relaxation layer that is formed between the integrated circuit formation surface and electrode pads on one hand and the bump electrodes and conductive layer on the other hand and is

adhered thereto, wherein the semiconductor device is featured in that more than one third of the stress relaxation layer from a surface thereof is cut away for removal and in that the stress relaxation layer is divided into a plurality of regions.

The present invention may be applied to a semiconductor device having a plurality of pads as formed in peripheral regions of the integrated circuit formation surface of a semiconductor element, one or several external electrodes as electrically connected via a conductive layer to the pads, and a stress relaxation layer that is adhered to the integrated circuit formation surface and the pads plus the external electrodes as well as the conductive layer. The stress relaxation layer or stress buffering layer may be subdivided into a plurality of portions independently of one another. Optionally a sealing resin may be provided which is in close contact with the stress relax layer. Where necessary, the sealing resin may come with division slits at appropriate positions for reduction of virtual modulus of elasticity to thereby suppress those stress forces being applied to the semiconductor element. More than one third of the stress relax material from its surface is cut away for removal, and this stress relax material may be divided in a way corresponding to each conductive layer.

The stress relax layer or stress buffer layer functions to make moderate or "soften" those thermal stresses that can take place due to possible differences in thermal expansion coefficient between the semiconductor elements and its associative mount substrate or board. Any one of the stress relax layer and buffer materials along with an elastic material layer and buffering layer plus buffer-material layer as well as low-elasticity material layer as will be discussed later in the description offers similar functionalities for suppression of thermal stress forces.

The present invention also provides a semiconductor device which comprises a semiconductor chip having a plurality of unitary semiconductor elements that are arranged to form an integrated circuit, a plurality of electrode pads that are formed on an integrated circuit formation surface side of the semiconductor elements, one or more bump electrodes for external connection that are connected via a conductive layer to the electrode pads, and an elastic material layer that is bonded to the integrated circuit formation surfaces of the semiconductor elements and the pads plus the bump electrodes as well as the conductive layer, featured in that the elastic layer is divided into a plurality of regions with respect to each of the unitary semiconductor elements.

In addition, the present invention provides a semiconductor wafer which comprises a semiconductive wafer having thereon a plurality of unitary semiconductor elements that form integrated circuitry, a plurality of conductive connection portions as formed on the side of integrated circuit formation surfaces of the semiconductor elements, more than one external electrode for external connection that is connected to the conductive connection portions via a conductive layer, and a buffering material that is adhered to the integrated circuit formation surfaces of the semiconductor elements and the conductive connection portions plus the external electrode as well as the conductive layer, featured in that the buffer material is subdivided into a plurality of regions within a region of the unitary semiconductor elements.

The instant invention also provides a method for manufacturing a semiconductor device featured in that the method comprises the steps of forming a buffer layer on an integrated circuit formation surface of a semiconductor wafer that has a plurality of unitary semiconductor elements arranged to form integrated circuitry and also has a plurality of electrode pads on the side of integrated circuit formation surfaces of the unitary semiconductor elements in a way such that the buffer layer is adhered to the integrated circuit formation surfaces and the

electrode pads, subdividing the buffer layer into a plurality of regions by cutting away for removal more than one third thereof from its surface, forming on or over the resultant buffer layer thus subdivided those bump electrodes for external connection and a conductive layer for use in connecting the electrode pads to the bump electrodes, and thereafter performing subdivision in units of the unitary semiconductor elements.

Further, this invention provides a method for manufacturing a semiconductor device featured by comprising the steps of forming a buffer material layer on an integrated circuit formation surface of a semiconductor wafer that has a plurality of unitary semiconductor elements arranged to form integrated circuitry and also has a plurality of conductive pads in peripheral regions on the integrated circuit formation surfaces of the unitary semiconductor elements in such a manner that the buffer layer is adhered or bonded to the integrated circuit formation surfaces and the conductive pads, dividing the buffer layer into a plurality of regions by cutting it for removal, forming on or over the resultant buffer layer thus divided those external connection bumps and a conductive layer for letting the electrode pads be connected to the bump electrodes, and thereafter performing separation in units of the unitary

semiconductor elements.

The invention may also be applicable to a method of manufacturing a semiconductor device that employs a semiconductor wafer having thereon a plurality of pads as formed in the central region of the integrated circuit formation surface of a semiconductor element. This manufacturing method is arranged to include the steps of forming a low-elasticity material layer on the integrated circuit formation surface of a semiconductor wafer having a plurality of pads in a way such that the low-elasticity material layer is adhered or bonded to the integrated circuit formation surface and the pads, dividing the low-elasticity material layer into a plurality of regions through cutaway for removal of more than one third of the low-elasticity material layer from its surface, forming on or over the resultant low-elasticity material layer thus divided certain bump electrodes and a conductive layer for use in letting the pads be connected to the bump electrodes, and performing separation with respect to each chip that contains therein at least one unitary semiconductor element.

The invention is also applicable to a semiconductor wafer manufacturing method which includes the step of forming a buffering material on an integrated circuit formation surface of a semiconductor wafer having a

plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of electrode pads on the side of integrated circuit formation surfaces of the semiconductor elements in such a manner that the buffering material is bonded to the integrated circuit surfaces and the electrode pads in a way independent in units of the electrode pads.

The present invention further provides a semiconductor module that is featured by comprising a semiconductor device including a semiconductor chip having a plurality of unitary semiconductor elements, a plurality of electrode pads as formed at the unitary semiconductor elements, a stress relax layer that is adhered to the integrated circuit formation surfaces of the semiconductor elements and the electrode pads plus the bump electrodes as well as the conductive layer and is subdivided into a plurality of regions, and any one of a sealing layer made of resin and protective coating as formed on the integrated circuit formation surfaces of the unitary semiconductor elements, wherein the semiconductor device is electrically connected to a mount substrate or board via the bump electrode for external connection. The invention is also applicable to a semiconductor module having a plurality of semiconductor devices that are mounted on a single mount substrate.

In the foregoing and following explanations, any one of those terms "pad electrodes," "pads," "conductive connection sections," "conductive pads," "circuit electrodes," "connection conductor portions," and "circuit pads," which are formed on the integrated circuit formation surface(s) of the semiconductor element(s), may refer to certain nodes or terminals for connection to either external electrodes or bump electrodes concerned. Additionally the terms "bumps" and "bump electrodes" as well as "external electrodes" as used herein may refer to those external terminals adapted for connection to the parts-mount substrate used.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 are process flow diagrams showing one example of a method of manufacturing a semiconductor device of the present invention.

Fig. 3 is a plan-view diagram showing a planar structure of a semiconductor wafer as used in the instant invention.

Fig. 4 shows a perspective view of a semiconductor device of this invention.

Figs. 5-6 are diagrams each depicting a plan view of a semiconductor device of the invention.

Fig. 7 is a flow diagram showing a method of forming

a stress relaxation layer.

Fig. 8 is a partial diagram at said flow process.

Fig. 9 is a diagram showing a plan view of a semiconductor device embodying the invention for indication of a stress relax layer and electrical lead thereof.

Fig. 10 is a diagram showing several plan views of a variety of kinds of structures of those semiconductor chips as used in the invention.

Figs. 11-12 are diagrams each showing a perspective view of the entire structure of another example of the semiconductor device of the invention.

Fig. 13 is a process flow diagram showing another method of manufacturing the semiconductor device.

Figs. 14-15 are sectional diagrams each showing a structure of a module with the semiconductor device of the invention being mounted thereon.

Fig. 16 depicts an enlarged perspective view of a stress relax layer and conductive layer used in the semiconductor device embodying the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An explanation will now be given of the means for achieving the present invention in detail below.

In the present invention the wording "semiconductor

element arranged to form integrated circuitry" as used herein may refer to an integrated circuit having at least one built-in circuit including a memory, logic, and microcomputer or else—practically, such as an LSI, VLSI, ULSI or other similar highly integrated ICs. In such semiconductor element one or more electrode pads for use as input/output terminal regions capable of inputting and outputting from and to external circuitry are formed so that these are electrically connected to a circuit section on the integrated circuit formation side. Further in this invention, bump electrodes for external connection are formed overlying the electrode pads with a conductive layer laid therebetween. In this invention, it is required that more than one conductor section be formed on or over an insulative or dielectric layer as subdivided through patterning into a plurality of portions in order to finally let the semiconductor element be electrically connected to its associative mount substrate or board. This dielectric layer will later be served as an stress relaxation layer or stress buffering layer. This conductor section is comprised of a conductive layer portion that is formed to extend from an electrode pad of an element along the side-wall(s) of the dielectric layer for serving as an electrical lead and a bump electrode portion for direct connection with the mount board.

As a method of forming the conductor section, there are two methods one of which is for fabricating both the conductive layer portion and the bump electrode at a time and the other of which is for forming them at separate process steps. The conductive layer portion may preferably be made of copper-based materials in view of lower resistivity. Methods for forming conductive leads made of copper include a metal-plating method and deposition method. Although the metal-plating method may be more advantageous and preferable than the deposition method for successful fabrication of the intended conductive layer that stays uniform up to inside of a hole of a circuit shape with increased aspect ratio, the former should require a longer period of time for completing the fabrication than the latter. One example is that while the deposition method requires approximately five (5) minutes to form the copper to a thickness of 3 micrometers (μm), the metal-plating method requires one hour or more. Due to this, it will be required to adequately select which one of such methods must be used to form a pattern shape of the dielectric layer for forming a copper conductive circuit layer made of copper.

As a method for patterning the conductive section, there are two approaches, one of which is for selectively metallizing or depositing only required portions in

advance by resist printing techniques, and the other of which is for pre-performing either metallization or deposition with respect to the entire surface and then using a resist or the like to let necessary portions continue to reside while removing away the remaining unnecessary portions. In the case of the former, addition of the selectivity of either the metal-plating or deposition between an exposed dielectric layer portion and a resist surface is important. To do this, optimization or the like is carried out for deposition of catalytic substance and/or resist surface conditions. In case a conductive layer is formed on the entire surface of the dielectric layer of the latter, use of electro-deposited resist will be effective due to the fact that a conductor is formed on the entire surface. Performing a series of process steps including resist electro-deposition and exposure plus development along with etching treatment makes it possible to effectuation of the intended patterning of the conductive section. Etching liquid used therein may be currently available copper etchant such as dilute sulfuric acid, nitric acid, iron chloride, copper chloride, ammonium persulfate or the like. It will be preferable that said conductive layer be formed to extend along the sidewall of either the stress relax layer or buffer layer which acts as a stress relaxation layer having

inclination. Forming a conductive layer on the sidewall of such slanted or inclined stress relax layer makes it possible to make moderate or "relax" any possible distortion occurring due to thermal stress forces along the thickness and/or mechanical stresses, which in turn enables further increase in reliability at connection portions concerned.

It should be noted here that the conductive layer that has been formed along the sidewall of the slanted stress relax layer is such that letting it change continuously in conductor width makes it possible to provide successful relaxation. Practically the intended relaxation is effectively achievable by making finer or narrower the semiconductor element's electrode pad side thereby causing it to gradually increase in width in a direction toward the side of a bump electrode that acts as an external terminal. One representative example is shown in Fig. 16.

Next, seal the dielectric layer's pattern section for protection of those connection portions between the semiconductor element's electrode pads and the conductive layer. At this time, although this sealing material may be made unlimitedly of any materials that offer sufficient adhesive strength relative to the dielectric layer, it will be desirable that certain materials be employed which are the same in base material as that forming the dielectric

layer. Use of such same-system materials enables addition of increased adhesivity because of their good affinity due to the fact that they have the same values in physical property such as elasticity and thermal resistivity or else and also are similar in chemical structure.

Even after having completed the sealing process, the result is not completely predictable—in one case the resultant stress relax layer is capable of retaining the intended division state; in another case, the expected effect of subdivision is lost due to resin sealing. In the latter case, it will be preferable that division by use of a laser be done after the resin sealing was applied to the entire surface. Also note that in cases where the seal material used is less in elasticity than the stress relax layer, such division using the laser is no longer required because of the fact that even if the stress relax layer's region thus divided is buried by the seal material then transmission of the force would function as an independent stress relax layer in some cases to ensure that the effect of division is hardly deteriorated. The sealing method may include, but not limited to, injection methods using dispensers, mask print methods or the like.

In the instant invention, it is required to form bump electrodes for use as external terminal portions for letting the semiconductor element be electrically

connected to a mount substrate or board via a conductive layer. These bump electrodes may be designed to have ball bumps, land bump structures or else. Such bump electrodes are manufacturable by metal-plating/metallization methods, ball transfer methods, paste printing methods and others. Certain materials with excellent corrosion resistance and increased mountability may be chosen therefor, which typically conclude gold, gold/nickel-lamination film, gold/copper-lamination film or other similar suitable film-like layers. A variety of kinds of solder-composition materials will also be useful since these are good in mass-productivity.

In the present invention a stress relaxation layer is formed between said bump electrodes and said conductive layer, which layer is for relaxation of those stress forces based on possible differences in coefficient of thermal expansion between the semiconductor element and its associated mount substrate or board while at the same time serving as an electrical insulative layer. This stress relax layer is the one that corresponds to said dielectric layer.

In this invention either the stress relax layer or buffer layer is the layer that has its elasticity capable of offering the intended effects of the invention. Preferably this layer is made of a chosen material of

0.1 MPa to 1 GPa at room temperatures. Particularly but not exclusively, the thickness of it is preferably determined to fall within a range of from 1 to 1,500 μm—more preferably, 10 to 200 μm.

In this invention the stress relax layer or buffer layer is comprised of certain resin materials such as for example epoxy resin, phenol resin, urethane resin, maleyimide resin, polyimide, polyoxazole, polyfluoroethylene, polysiloxane, polybutadiene, or other similar suitable materials, along with copolymer materials thereof and denatured ones. To let such stress relax layer or buffer layer be low in elasticity, it will be permissible to design it to have multi-cellular or porous structures. Note however that as long as this stress relax layer or buffer layer is subdivided into portions to thereby eliminate unwanted application of excessive stress forces to a semiconductor chip and conductive layer bumps, and in cases where a sealing resin as filled into the space is of low elasticity it will not always be necessary that the stress relax layer's resin per se is of a low-elasticity material.

One typical methodology adaptable for use as the method of forming the stress relax layer may be a method that is designed to proceed with the next process step of forming a stress relax layer and external terminals while

permitting the size of a wafer to be kept unchanged without performing dicing of a circuitry-fabricated wafer into pieces, by way of example. The first step is to form a stress relax layer made of low-elasticity dielectric material that is employable as the stress relax layer. In this case several methods are available, one of which is to make use of photosensitive materials. The photosensitive materials may be generally classified in nature into two groups: liquid resin, and film-like one. In the former case, spin-coating or curtain-coating or printing techniques are used to form a deposition film to thereby fabricate the intended dielectric layer on the entire surface of a wafer under manufacture (this will function as a stress relax layer in case it is disposed on a semiconductor device). In the case of a film, it is possible to use roll-lamination methods or press-machining methods or else to form such dielectric layer on the entire wafer surface. Next, let the dielectric layer be subject to patterning by use of an appropriate mask. Through such patterning process, let those connection pads on the wafer be exposed while simultaneously defining the shape of the dielectric layer as required to form one or more conductor portions having the intended stress relaxation mechanism.

At this time the stress relax layer may be formed so that it is subdivided into a plurality of individual

portions. Note here that another approach to attaining the same is also available—that is, after having formed a stress relax layer having an integral structure on the entire wafer surface, then at a separate later process step remove and cut away more than one third thereof from a surface layer by using a laser or else thereby causing the stress relax layer to be divided into a plurality of regions.

Photosensitive resin materials capable of exposure and development stated supra may include acrylic resin, resin composition comprised of epoxy resin and acrylic resin, vinyl-ester resin composition of epoxy resin and acrylic acid plus vinyl monomer as chemically reacted together, polyimide, and the like. For presently available many photosensitive dielectric materials and their rubber denatured compositions which have been employed as resist and/or photo-via materials, these will also be applicable through careful selection of the elasticity thereof.

The photovia materials are particularly preferable among them, which consist essentially of a resist material including vinyl-ester resin and also epoxy resin composition along with a resin composition that contains therein epoxy resin and acrylic resin components. In cases where these are employed, one preferable way is such that a roll laminator is set to be under pressures of 0.01 to

10 kgf/cm at temperatures ranging from the room temperature up to 200°C by way of example; in the case of press-machining schemes, processing is done under pressures of 1 to 50 kgf/cm at temperatures of from the room temperature up to 200°C. In the case of printing methods, if screen-print techniques are preferable then it is a general approach that printing is carried out at those temperatures at or near the room temperature. For spin-coat methods, it will be preferable that the intended printing be done at the number of revolution of from 100 to 10,000 rpm at the room temperature. For curtain-coat methods, printing is done at speeds of from 10 to 100 mm/second at the room temperature.

Upon effectuation of such patterning, a high-pressure mercury lamp or lamps are employed to give off rays of ultraviolet (UV) light for exposure. Developing solution may be chosen on a case-by-case basis depending on what kind of resin is used—preferably, but not limitatively, known alkali liquid developer is used.

An alternative method of forming the dielectric layer required is such that a liquid resin or film—this may be comprised of generally known low-elasticity materials without exhibiting any photosensitivity—is formed on the entire surface of a wafer of interest by using the similar method as discussed previously; then, patterning is

carried out by use of either a laser or a combination of an oxygen plasma and a mask to thereby obtain a specified shape. At this time the plasma is typically obtainable by using either an oxygen gas or a mixture gas of oxygen and fluoride such as CF_4 or the like. In addition, as the laser, there are excimer laser, YAG laser, carbon deoxide gas laser and others—among them, the carbon deoxide gas laser will be effective because it offers increased processing speeds and enhanced usability. Any material for use as the dielectric layer in this case will not always be required to offer photosensitivity, and it is preferable that material selection be made by taking account of specific physical characteristics of resin including the low elasticity and high heat resistivity. Representative low-elasticity materials must be epoxy resin, polyimide resin, oxazole resin and cyanate resin along with rubber denatured materials and rubber-added ones thereof. Use of porous materials will also be preferable in view of achievement of low elasticity. Among these materials, epoxy resin is preferably employable due to the fact that this resin is hardenable at relatively low temperatures at or near 150°C while its hardened material stays low in moisture absorption characteristic with production costs reduced.

Other methods for achieving simultaneous effectuation

of both the dielectric layer fabrication and the patterning required are available, which include print methods, ink-jet methods, optical shaping/molding methods, deposition methods, multiphoton polymerization methods or else. Among these methods, the print methods may be easy methodology that is capable of obtaining the intended dielectric layer by performing printing processes by a method of patterning a resin with certain flowability by use of either a screen mask or stencil mask and thereafter effectuating hardening and solidifying of the resin due to optical or thermal cross-linking reaction. In contrast, the ink-jet methods and optical shaping methods require installation of specially designed apparatus; however, these methods offer enhanced micro-patterning abilities and are thus effective in forming dielectric layers that measure 50 μm or less in width. Further, deposition methods and multi-photon polymerization methods with semiconductor circuit fabrication technologies applied thereto offer an ability to fabricate finer shapes, which will thus be effective for fabrication of thin dielectric layers of 1 μm or less in width.

One significant feature of the semiconductor device incorporating the principles of the invention is that more than one third of its stress relax layer or buffer layer from the surface thereof is removed and cut away to be

subdivided into a plurality of regions on a semiconductor chip. One example is that a semiconductor device having on a wafer with a semiconductor integrated circuit formed thereon a stress relax layer for reduction of thermal stress forces relative to a mount substrate or board and also its overlying structure having bump electrodes for use as external terminals while letting said stress relax layer be such that more than one third thereof is cut away from its surface to be split into a plurality of regions is manufactured to have a dimension equivalent to the wafer size and then is finally divided into pieces. Cutting away more than one third of the stress relax layer from its surface for subdividing this stress relax layer into a plurality of regions makes it possible to make smaller a region that moves cooperatively when absorbing stress forces to thereby obtain a readily deformable structure, which in turn enables enhancement of the stress relaxation effects. This makes it possible to permit the stress relax layer to offer sufficient plasticity or resiliency even in the event that thermal stress forces can take place between the semiconductor element and its associated mount substrate or board in temperature cycles or else, which leads to an ability to improve the electrical connection reliability of those external terminals for use in connecting between the semiconductor element and mount

substrate. Additionally, dividing the stress relax layer advantageously serves to facilitate any water components as absorbed by a package during storage or custody of such semiconductor device to escape toward the outside during reflowing of mount parts or components, thereby allowing the package to increase in anti-reflow reliability.

In accordance with the present invention, there is provided a method of manufacturing individual semiconductor devices by preparing an aggregated body of the semiconductor devices having the above-noted arrangements in units of wafers and finally separating it into those chips each containing a unitary semiconductor element. In addition, as a module with the semiconductor device of this invention mounted therein comprises a semiconductor device excellent in anti-reflow characteristics and temperature cycle resistivity, the device is higher in integration density and reliability than the prior art. The stress relax layer at this time may be obtained by performing specified patterning processes using a photosensitive resin or alternatively by patterning a thermally hardenable resin using either a laser or oxygen plasma. Still another methodology of forming the stress relax layer is available, which may include those methods which follow: patterning by print techniques using either a screen mask or stencil mask,

patterning by ink-jet techniques, patterning by optical shaping techniques, organic deposition techniques as used in semiconductor lead manufacturing processes, multi-photon polymerization techniques employing microelectronics mechanical systems. Also note that letting the stress relax layer be set at 1 GPa or less in elasticity at 25°C makes it possible to obtain superior reliability in electrical connection between the semiconductor element and mount substrate or board used.

One possible approach to dividing the stress relax layer is to employ division methods using the patterning techniques discussed above; another approach to such layer division is to use a laser or the like to remove and cut away more than one third from a top surface layer at a specified location after having formed a stress relax layer on the entire surface. In addition, various forms are still available as the division state covering from a binary-division scheme for causing a plurality of bump electrodes to be formed at a single stress relax layer to an independent structure with each of such bump electrodes being formed at the individual one of stress relax layers involved.

An explanation will next be given of preferred embodiments of the present invention in conjunction with the accompanying figures of the drawing.

See Fig. 1, which shows one exemplary method of manufacturing a semiconductor device in accordance with one preferred embodiment of the instant invention. Fig. 2 illustrates, in cross-section, some of the major process steps in the manufacture of semiconductor chips on a per-wafer basis by use of the manufacturing method of Fig. 1. The manufacturing procedure begins with a step of depositing by screen-print techniques an epoxy-based photosensitive liquid resin material on the entire surface of a wafer 1 with integrated circuitry (not shown) formed thereon. After completion of such deposition, dry any residual solvent and electrode pads 2 to thereby obtain a film that measures 150 micrometers (μm) in thickness. Then, put a mask (not shown) on the resultant structure to perform ultraviolet (UV) exposure for effectuation of cross-link reaction at specified portions; thereafter, perform patterning by using an alkali developer liquid to thereby fabricate a stress relaxation layer 3 as shown in Fig. 2(a). At this time the electrode pads 2 on the wafer are also exposed due to patterning.

The procedure goes next to a step of forming by electroless metal-plating or metallization techniques a copper layer on the entire surface of the wafer 1 and stress relax layer 3, to a thickness of 10 μm. Then, for patterning of conductor portions, form an electro-

deposited resist film to a thickness of 5 μm; thereafter, perform UV exposure using a mask for acceleration of the cross-link reaction with respect to specified portions; then, perform patterning by using an alkali developer liquid to thereby remove away unnecessary copper portions (conductive portions) by a chosen etching liquid, thus forming after removal of the resist a conductive layer 4 as shown in Fig. 2(b). Next, use screen-print techniques to provide an epoxy-based liquid sealing resin material for fulfillment as shown in Fig. 2(c) for purposes of protection of certain contact or junction portions from external environments, which portions are between the electrode pads 2 on the wafer 1 and the metallized conductive layer 4. Use of such liquid resin of the solvent-less type at this time ensures that any unwanted film loss does no longer take place after completion of hardening process, which makes it possible to achieve successful filling/sealing effects. Additionally, as shown in Fig. 2(d), the resultant seal resin layer 5 is subject to laser machining for defining therein cutaway portions to thereby reduce or suppress stress forces that can be applied to chips. It will be desirable that the depth of cutaway portions as designated by reference character "x" be set at a prespecified value that is greater than or equal to one third of the thickness of the seal

resin layer.

Next, fabricate ball-like bump electrodes 6 by solder ball-transfer and reflow techniques at exposed portions of the conductor sections as shown in Fig. 2(e) in order to facilitate electrical interconnection with a mount substrate or board.

Finally, subdivide the wafer into individual pieces to thereby obtain the intended semiconductor device 10.

Turning to Fig. 3, there is shown an example with electrode pads 2 formed in two opposite regions at the periphery of a circuit type surface side of the wafer, which diagram is a plan view of the wafer 1 that is usable in the present invention with the electrode pads 2 being formed thereon.

Fig. 4 is a diagram showing a perspective view of the semiconductor device embodying the invention in the state that the sealing layer made of resin is not formed yet. The sealing resin layer 5 is formed as indicated by dash-dot lines. As shown in Fig. 4, the stress relax layer 3 is arranged so that it is subdivided in a way corresponding to the bump electrodes 6 or the conductive layer 4 that is to be connected to these bump electrodes or the electrode pads 2 to thereby minimize those stress forces being applied to the wafer 1.

Figs. 5 and 6 are diagrams each showing a plan view

of a semiconductor device also embodying the invention. Fig. 5 shows a structure with the electrode pads 2 being formed in two opposite regions near or around the circuit formation surface side whereas Fig. 6 depicts a structure with the electrode pads 2 formed in a single direction in a central region of the circuit formation surface. In Figs. 5-6, reference character "Y" is used to designate a groove for subdivision, which groove is defined in the stress relax layer 3 by cutting for removal more than one third of the thickness thereof, which is for lowering a virtual elastic coefficient or modulus of the stress relax layer thereby reducing the stress force components as applied to semiconductor chips. Reference character "x" as used herein designates those slits as formed in the sealing resin layer 5. In Fig. 6, the dividing groove Y is not provided because of the fact that the positions of the electrode pads are center pads.

Figs. 7 and 8 show a method of forming by ink-jet techniques a resin material only at specified locations, which resin is for use in forming a stress relax layer 11 overlying the wafer 1 with a semiconductor circuit formed thereon. Whereby, the stress relax layer 11 is formed on the electrode pads 2 of a chip or chips. Fig. 9 is a diagram that shows a top plan view of a single electrode pad unit of a semiconductor element of Fig. 8(a).

Next, a copper film was formed by sputter-deposition techniques to a thickness of 5μm, on both a pattern surface of the exposed stress relax layer 11 and surfaces of the electrode pads 2 on the wafer 1; further, form a gold film to a thickness of 0.5 μm so that a conductive layer 12 was formed. In this case, it is possible to uniformly fabricate by deposition the conductive layer 12 due to the absence of any hole shapes of high aspect ratios or the like.

It is also noted that as any etching treatment is not required for the conductive layer 12, those surfaces of the electrode pads 2 on the wafer 1 are perfectly covered or coated with a corrosion-resistant metallic material. Owing to this, resin sealing of pad junction interfaces is generally unnecessary; however, certain resin may optionally be filled therein for purposes of increasing the reliability when the need arises. Liquid resin fulfillment using dispensers is an easy-to-use method as it requires no masks. Since a stress relax layer obtained by this method with a conductive layer attached thereto has a convex structure of low elasticity from the wafer surface, this layer per se will be used as an external terminal for electrical connection to its associated mount substrate. It is thus possible to eliminate the need for bump fabrication process steps. To enhance the

mountability, more than one ball-like bumps may be added. Bump forming methods may include paste-printing techniques, paste ink-jet techniques, ball transfer techniques and the like. Finally, cut the wafer into chips each including a unitary semiconductor element to thereby obtain the intended semiconductor device as shown in Fig. 8(b).

In Fig. 10, semiconductor chips 14-17 may be split into a unitary semiconductor element (a) or those (b) to (d) each containing a plurality of unitary semiconductor elements.

Figs. 11 and 12 are examples of the semiconductor device which are different from the stress relax layer stated previously. In Fig. 11 a stress relax layer 19 is formed so that it is subdivided in units of columns of the bump electrodes 6 for use as external terminals. Alternatively, Fig. 12 is one example of the semiconductor device with an integrated stress relax layer 21 being finally divided. Letting a plurality of stress relax layers be divided in this way makes it possible to reduce or make moderate those stress forces with respect to semiconductor elements thereby enabling reduction in amount of any possible distortion occurring at such semiconductor elements. It is also possible to facilitate water components absorbed by a package to escape toward the outside; thus, the connection reliability during

parts-mount reflow processes may be greatly improved.

Fig. 13 shows still another method for manufacturing the semiconductor device in accordance with the invention. As shown in Fig. 13(a), split a stress relax layer 22 into a plurality of portions to thereby ensure that vacant or "gap" regions that are not integrated by resin materials 2, 3 are present even after completion of such resin sealing. This method is free from any limitations as to the elasticity of a seal material used while avoiding the need for cutaway processes using a laser or else, which makes it possible to provide a manufacturing method that is extremely high in degree of freedom.

Figs. 14 and 15 are diagrams each showing a sectional view of a module with the semiconductor devices of this invention being built on a mount board or substrate 25. As the semiconductor devices 10 of the invention are excellent in anti-reflow characteristics and connection reliability, it becomes possible to permit the semiconductor devices to be laid out to come closer to each other when compared to the prior art to thereby enable achievement of high-integration mountability, which in turn makes it possible to obtain an improved module of further increased reliability.

As has been explained above in detail, according to the present invention, it is possible to offer several

advantages which follow. More specifically, it is possible to significantly reduce the production cost and time while providing the structure of high reliability, by manufacturing, on a wafer with semiconductor circuitry formed thereon, a structure in per-wafer size which has both a stress relax layer for reduction of the thermal stress relative to a parts-mount substrate or board and one or more external terminals capable of electrically connection with the mount substrate and then finally subdividing it into individual pieces or chips to thereby obtain the intended semiconductor device(s). Another advantage is that use of the stress relax layer as arranged within the semiconductor device makes it possible to reduce thermal stress forces occurring between the mount substrate and associative elements during temperature cycling test procedures thus attaining higher reliability. A further advantage is that the semiconductor device is identical in size to the semiconductor element thereby enabling achievement of high-density mounting.

The present invention as disclosed and claimed herein is successfully adaptable for use in providing those semiconductor devices that are excellent in reliability of connection between semiconductor elements and a mount substrate or board associated therewith and also in high-speed signal transmission as well as in multiple-

pin accommodatability along with high-density/high-reliability modules which employ such semiconductor devices.



WHAT IS CLAIMED IS:

1. A semiconductor device comprising a semiconductor element for formation of integrated circuitry, a plurality of electrode pads formed on an integrated circuit formation surface side of said semiconductor element, bump electrodes for external connection as electrically connected to said electrode pads through a conductive layer, and a stress relaxation layer being formed between the integrated circuit formation surface and electrode pads on one hand and the bump electrodes and conductive layer on the other hand and being adhered thereto, characterized in that more than one third of said stress relaxation layer from a surface thereof is cut away for removal and in that said stress relaxation layer is divided into a plurality of regions.

2. A semiconductor device comprising a semiconductor element, a plurality of circuit electrodes as formed on a circuit formation surface side of said semiconductor element, external electrodes for connection with a mount substrate and for being connected to said circuit electrodes through a conductive layer, and a stress relaxation layer adhered to the circuit formation surface of said semiconductor element and said circuit electrodes plus said external electrodes as well as said conductive layer, characterized in that said stress relaxation layer



is subdivided into a plurality of regions.

3. The semiconductor device as recited in claim 2, wherein a sealing layer made of resin is formed to be in close contact with said stress relaxation layer.

4. A semiconductor device comprising a semiconductor element for formation of an integrated circuit, a plurality of electrode pads as formed in a peripheral region on an integrated circuit formation surface side of said semiconductor element, external electrodes for external connection as electrically connected to said electrode pads through a conductive layer, and a stress relaxation material adhered to the integrated circuit formation surface and said electrode pads plus said external electrodes as well as said conductive layer, characterized in that more than one third of said stress relaxation material from a surface thereof is cut away for removal, and in that said stress relaxation layer is divided per each conductive layer.

5. The semiconductor device as recited in claim 4, characterized in that a resin is sealed in those spaces in which said stress relaxation layer is divided into a plurality of regions.

6. A semiconductor device comprising a semiconductor element, a plurality of circuit electrodes as formed on a circuit formation surface side of said semiconductor

element, more than one external electrode for connection with a mount substrate, said external electrode being connected to said circuit electrodes via a conductive layer, and a stress relaxation layer as connected to the circuit formation surface of said semiconductor element and said circuit electrodes plus said external electrode as well as said conductive layer, characterized in that said stress relaxation layer is split into a plurality of regions.

7. The semiconductor device as recited in claim 6, wherein a seal layer made of resin is formed into close contact with said stress relaxation layer.

8. A semiconductor device comprising a semiconductor element arranged to form an integrated circuit, a plurality of electrode pads as formed on two opposite sides of a peripheral region on a circuit formation surface side of said semiconductor element, one or more external electrodes for external connection as electrically connected to said electrode pads through a conductive layer, and a stress relaxation layer bonded to said integrated circuit formation surface and said electrode pads along with said external electrodes and said conductive layer, characterized in that more than one third of said stress relaxation layer from its surface is cut away and in that said stress relaxation layer is subdivided with respect to each conductive layer.

9. The semiconductor device as recited in claim 8, wherein a sealing layer of resin is formed to be in close contact with said stress relaxation layer.

10. A semiconductor device comprising more than one semiconductor element forming an integrated circuit, a plurality of electrode pads as formed along one direction in a central region on an integrated circuit formation surface side of said semiconductor element, external connection bumps as connected to said pads through a conductive layer, and a stress relaxation layer adhered to said integrated circuit formation surface and said pads plus said bumps as well as said conductive layer and in that said stress relaxation layer is divided into a plurality of regions.

11. A semiconductor device comprising a semiconductor chip having a plurality of unitary semiconductor elements arranged to form an integrated circuit, a plurality of electrode pads as formed on an integrated circuit formation surface side of each of said semiconductor elements, one or more bump electrodes for external connection, said bump electrodes being connected to said electrode pads through a conductive layer, and an elastic layer as bonded to the integrated circuit formation surface of said semiconductor elements and said pads plus said bump electrodes as well as said conductive layer,

characterized in that said elastic layer is divided into a plurality of regions with respect to each of said unitary semiconductor elements.

12. The semiconductor device as recited in claim 11, wherein a sealing layer of resin is formed into close contact with said elastic layer.

13. A semiconductor device comprising a semiconductor wafer having thereon a plurality of unitary semiconductor elements forming integrated circuitry, a plurality of conductive connection portions as formed on an integrated circuit formation surface side of a respective one of said semiconductor elements, more than one external electrode for external connection being connected to said conductive connection portions through a conductive layer, and a buffer material adhered to integrated circuit formation surfaces of said semiconductor elements and said conductive connection portions plus said external electrode as well as said conductive layer, characterized in that said buffer material is subdivided into a plurality of regions within a region of said unitary semiconductor elements.

14. The semiconductor device as recited in claim 13, wherein a sealing layer made of resin is formed to be in close contact with said buffer material.

15. A method for manufacturing a semiconductor device

characterized by comprising the steps of forming a buffer layer on an integrated circuit formation surface side of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of electrode pads on the side of integrated circuit formation surfaces of said unitary semiconductor elements in a way such that said buffer layer is adhered to the integrated circuit formation surfaces and said electrode pads, subdividing said buffer layer into a plurality of regions by cutting away for removal more than one third thereof from its surface, forming on or over a resultant buffer layer subdivided bump electrodes for external connection and a conductive layer for use in connecting said electrode pads to said bump electrodes, and thereafter performing subdivision in units of the unitary semiconductor elements.

16. A method of manufacturing a semiconductor device characterized by comprising the steps of forming a buffer material layer on an integrated circuit formation surface side of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of electrode pads in two opposite peripheral regions on the side of integrated circuit formation surfaces of said unitary semiconductor elements in a way such that the buffer layer

is adhered to the integrated circuit formation surfaces and said electrode pads, dividing said buffer layer into a plurality of regions by cutting for removal said buffer layer in a direction along a thickness thereof, forming on or over a resultant buffer layer thus divided external connection bumps and a conductive layer for letting said electrode pads be connected to said bumps, and then performing separation in units of the unitary semiconductor elements.

17. A method of manufacturing a semiconductor device characterized by comprising the steps of forming a stress relaxation layer on an integrated circuit formation surface of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of pads aligned in one direction in a central region on an integrated circuit formation surface side of said unitary semiconductor elements in such a manner that said stress relaxation layer is independent per pad, forming on or over said stress relaxation layer certain bumps and a conductive layer for letting the bumps be connected to external connector bumps, and thereafter performing separation in units of the unitary semiconductor elements.

18. A method for manufacturing a semiconductor device characterized by comprising the steps of forming a

low-elasticity material layer on an integrated circuit formation surface side of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of pads on the side of integrated circuit formation surfaces of said unitary semiconductor elements in a way such that said low-elasticity material layer is in close contact with said integrated circuit formation surface and said pads, dividing said low-elasticity material layer into a plurality of regions through cutaway for removal of more than one third of said low-elasticity material layer from a surface thereof, forming on or over resultant low-elasticity material layer thus divided certain bumps and a conductive layer for letting said pads be connected to said bumps, and then performing separation with respect to each chip containing therein at least one of said unitary semiconductor elements.

19. A method of manufacturing a semiconductor device characterized by comprising the steps of forming a stress relaxation layer on an integrated circuit formation surface side of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of electrode pads in two opposite peripheral regions on the side of integrated circuit formation surfaces of said

unitary semiconductor elements while letting said stress relaxation layer be adhered to the integrated circuit formation surfaces and said electrode pads, subdividing said stress relaxation layer into a plurality of regions by cutting away more than one third of said stress relaxation layer from a surface thereof, and forming on or over such divided stress relaxation layer certain bump electrodes and a conductive layer for connecting said electrode pads to said bump electrodes.

20. A method of manufacturing a semiconductor device characterized by comprising the steps of forming a buffer material on an integrated circuit formation surface of a semiconductor wafer having a plurality of unitary semiconductor elements arranged to form integrated circuitry and also having a plurality of electrode pads as formed on the side of integrated circuit formation surfaces of said unitary semiconductor elements in such a way that said buffer layer is adhered to the integrated circuit formation surfaces and said electrode pads while being independent per electrode pad, forming on or over such resultant divided buffer layer external connection bump electrodes and a conductive layer for use in letting said electrode pads be connected to said bump electrodes, and then using a resin in close contact with said buffer material to seal necessary part of an exposed surface.

21. A semiconductor module characterized by comprising: a semiconductor device including a semiconductor chip having a unitary semiconductor element, a plurality of electrode pads as formed at said unitary semiconductor element, a stress relaxation layer adhered to an integrated circuit formation surface of said unitary semiconductor element and said electrode pads as well as a conductive layer for use in letting said electrode pads be connected to external connection bump electrodes, and a protective coating as formed on the integrated circuit formation surface of said unitary semiconductor element while causing said stress relaxation layer to be subdivided into a plurality of regions; and a mount substrate as electrically connected via said external connection bump electrodes.

22. A semiconductor module characterized in that a plurality of pieces of semiconductor devices each including a semiconductor chip having thereon a unitary semiconductor element, a plurality of circuit pads as formed on an integrated circuit formation surface of said unitary semiconductor element, external connection bumps as connected via a conductive layer to said circuit pads, and a stress relaxation layer being connected to the integrated circuit formation surface of said unitary semiconductor element and said circuit pads plus said

external connection bumps as well as said conductive layer and being divided into a plurality of regions is connected to a mount board via said external connection bumps.

23. A semiconductor module characterized by comprising a plurality of semiconductor devices each including a semiconductor chip having a unitary semiconductor element arranged to form integrated circuitry, electrode pads as formed in two opposite regions near or around an integrated circuit formation surface of said unitary semiconductor element, external connection bump electrodes as electrically connected via a conductive layer to said electrode pads, a buffer layer adhered to the integrated circuit formation surface of said semiconductor element and said electrode pads plus said bump electrodes as well as said conductive layer, and an insulative material formed on the integrated circuit formation surface of said unitary semiconductor element to be in close contact with said buffer layer while letting said buffer layer be subdivided into a plurality of regions, said semiconductor devices being connected to a mount substrate via said bump electrodes.

24. A semiconductor device comprising more than one semiconductor element forming an integrated circuit, a plurality of electrode pads as formed on an integrated circuit formation surface side of said semiconductor

element, an external connection bump electrode as electrically connected to said electrode pads via a conductive layer, and a stress relaxation layer as formed to be bonded to said electrode pads and said conductive layer plus said external connection bump electrode, characterized in that said stress relaxation layer has an inclined structure in a direction along the thickness thereof and in that said conductive layer is formed along an inclined plane of the stress relaxation layer.

25. A semiconductor device comprising more than one semiconductor element arranged to form an integrated circuit, a plurality of electrode pads formed on an integrated circuit formation surface side of said semiconductor element, one or more external connection bump electrodes as electrically connected to said electrode pads via a conductive layer, and a stress relaxation layer formed and adhered to said electrode pads and said conductive layer as well as said external connection bump electrodes, characterized in that said conductive layer is arranged to continuously change in conductor width from said electrode pads up to said external connection bump electrode.

26. The semiconductor device as recited in claim 25, characterized in that the conductor width of said conductive layer is decreased on its electrode pad side

and is increased on an external connection bump electrode side.