INSPECTION SYSTEM, INSPECTING DEVICE AND GAMING CHIP

CROSS REFERENCE TO RELATED APPLICATION

[0001]

This nonprovisional application is based on Japanese Patent Application No. 2016-225540 filed with the Japan Patent Office on November 18, 2016, the entire contents of which are hereby incorporated by reference.

FIELD

[0002]

The present invention relates to an inspection system and an inspecting device which are capable of inspecting a gaming chip, and more particularly to, an inspection system and an inspecting device which are capable of inspecting a plurality of gaming chips contained in a case.

BACKGROUND

[0003]

Gaming chips used in game halls such as casinos are manufactured in factories and then transported to game halls, stored in a storage, and moved from the storage to cashiers or game tables in the hall, but it is necessary to prevent gaming chips from being stolen or being replaced with fake gaming chips in the process of transporting, storing, and moving. To this end, a case containing gaming chips is used. If a plurality of gaming chips are contained in the case and, then the case is sealed, it is possible to discover a situation in which the gaming chips are withdrawn from the case after the sealing.

[0004]

As a gaming chip in which a radio tag storing identification information or type information is internally installed, and optically readable code information indicating the identification information or the type information is assigned to a side surface is known (for example, JP 2009-66172 A).

[0005]

A system using a gaming chip is disclosed in JP 2009-66172 A. In the system, the number of gaming chips placed on a betting board of a game table is calculated on the basis of identification information stored in a radio tag, the number of gaming chips is calculated on the basis of identification information assigned to a side surface, and the calculated numbers of gaming chips are compared. Accordingly, it is possible to detect an unauthorized gaming chip when the unauthorized gaming chip is used in the game table.

[0006]

However, since the system disclosed in JP 2009-66172 A detects a fraud by calculating the number of bet gaming chips (placed on the betting board), the system is unable to inspect a plurality of gaming chips contained in the case in a state where the gaming chips are contained in the case and detect the unauthorized gaming chip.

[0007]

In this regard, ~~it is an object of the~~ embodiments of the present disclosure seek to provide an inspection system and an inspecting device which ~~are~~ may be

capable of inspecting a plurality of gaming chips contained in a case in a state where the gaming chips are contained in the case.

SUMMARY

[0008]

An aspect of the present invention provides an inspection system comprising an area on which a plurality of gaming chips is configured to be placed, each gaming chip of the plurality of gaming chips includes a radio frequency identification (RFID) tag; and an inspecting device that includes: a first sensing device, wherein the first sensing device is configured to acquire, by way of RFID, first gaming chip information from the plurality of gaming chips placed in the area; a second sensing device, wherein the second sensing device is configured to optically determine the presence or absence of a gaming chip placed in the area, wherein second gaming chip information indicates the determined presence or absence of the gaming chip; and a processor, wherein the processor is configured to use the first gaming chip information acquired by the first sensing device and the second gaming chip information determined by the second sensing device to determine a damage status of the gaming chip placed in the area by combining (a) the first gaming chip information acquired by the first sensing device and (b) the second gaming chip information determined by the second sensing device.

[0008a]

An inspection system according to a first aspect of the embodiment is an inspection system that inspects a gaming chip having at least first gaming chip information and second gaming chip information, the second gaming chip information is arranged on a side surface of the gaming chip in an optically readable form, the inspection system includes a case that

contains a plurality of gaming chips in a stacked manner and an inspecting device that inspects the gaming chip contained in the case, wherein the inspecting device includes a first reading device that acquires the first gaming chip information of the gaming chip contained in the case, a second reading device that optically reads the side surface of the gaming chip contained in the case and acquires the second gaming chip information, and a determining unit that determines whether a plurality of gaming chips contained in the case are pass or fail by determining the authenticity or damages of all the gaming chips contained the case or the number of gaming chips for each value using the first gaming chip information acquired by the first reading device and the second gaming chip information acquired by the second reading device.

[0009]

With this configuration, since both the first reading unit and the second reading unit acquire the first gaming chip

CLAIMS

~~1. An inspection system that inspects gaming chips, the inspection system comprising:~~

~~an area in which can be placed, in a stacked manner, a plurality of gaming chips that include (a) first gaming chip information and (b) second gaming chip information, the second gaming chip information provided in an optically readable form on respective side surfaces of the gaming chips; and~~

~~an inspecting device configured to inspect the gaming chips placed in the area, the inspecting device includes:~~

~~a first reader configured to acquire the first gaming chip information of all of the gaming chips placed in the area;~~

~~a second reader configured to optically read the side surfaces of the gaming chips placed in the area; and~~

~~a processor configured to determine, respectively for each gaming chip of the plurality of gaming chips placed in the area, whether there is a discrepancy between (a) the respective first gaming chip information acquired by the first reader for the respective gaming chip and (b) the respective second gaming chip information acquired by the second reader for the respective second gaming chip to thereby determine whether the gaming chips placed in the area are in a pass state or a fail state.~~

~~2. The inspection system according to claim 1, wherein the first gaming chip information and the second gaming chip information of respective ones of the gaming chips include common information portions for inclusion of respective common information of the respective gaming chips, and the processor is configured to determine that the plurality of the gaming chips placed in the area are in the fail state when the common information portions of a plurality of pieces of the first gaming chip information acquired by the first reader do not coincide with corresponding common information portions of a plurality of pieces of the second gaming chip information acquired by the second reader.~~

~~3. The inspection system according to claim 1, wherein one or both of the first gaming chip information and the second gaming chip information includes individual identification information individually identifying respective ones of the gaming chips.~~

~~4. The inspection system according to claim 3, wherein the processor is configured to determine that the plurality of the gaming chips placed in the area are determined to be in the fail state when the individual identification information of a plurality of pieces of first gaming chip information acquired by the first reader does not coincide with the individual identification information of a plurality of pieces of second gaming chip information acquired by the second reader.~~

~~5. The inspection system according to claim 1, wherein the second gaming chip information includes information indicated by designated colors that indicate respective values of the gaming chips.~~

~~6. The inspection system according to claim 1, further comprising:~~

~~a storage unit configured to store respective individual identification information of at least the first or second gaming chip information of the gaming chips authorized to be placed in the area, and~~

~~wherein the processor is configured to determine that the plurality of gaming chips placed in the area in the fail state when a plurality of pieces of individual identification information of the respective first gaming chip information of the respective gaming chips acquired by the first reader or a plurality of pieces of individual identification information of the respective second gaming chip information of the respective gaming chips acquired by the second reader do not coincide with a plurality of pieces of individual identification information of the first and second gaming chip information stored in the storage unit.~~

~~7. The inspection system according to claim 1, wherein the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when a number of pieces of the first gaming chip information acquired by the first reader or a number of pieces of the second gaming chip information acquired by the second reader is not a predetermined number.~~

~~8. The inspection system according to claim 1, wherein:~~

~~the gaming chips include color information indicating respective values of the gaming chips as the second gaming chip information, and include respective value information identifying respective values of~~

~~the gaming chips as the first gaming chip information; and~~

~~the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when the color information does not coincide with the value information of the first gaming chip information.~~

~~9. The inspection system according to claim 8, wherein:~~

~~the second gaming chip information further includes respective value information of the respective gaming chips in addition to the color information; and~~

~~the inspection system further includes a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that a respective one of the gaming chips that is in the fail state can be identified when a value of the respective gaming chip indicated by the color information in the second gaming chip information of the respective gaming chip does not coincide with the value information of the second gaming chip information, the value information of the first gaming chip information of the respective gaming chip, or a combination thereof.~~

~~10. The inspection system according to claim 8, wherein:~~

~~the second gaming chip information further includes respective value information of the respective gaming chips in addition to the color information; and~~

~~the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when a value of a respective one of the gaming chips indicated by the color information in the second gaming chip information of the respective gaming chip does not coincide with the value information of the second gaming chip information, the value information of the first gaming chip information, or a combination thereof.~~

~~11. The inspection system according to claim 10, wherein the processor is configured to determine a respective number of the gaming chips placed in the area for each of the values or a total amount of the values of all of the gaming chips based on the color information or the value information of the first gaming chip information or the second gaming chip information.~~

~~12. The inspection system according to claim 10, wherein the processor is configured to determine that the plurality of the gaming chips placed in the area are in the fail state when the color information does not coincide with (a) the value information of the first gaming chip information or the second gaming chip information, (b) common information, or (c) individual identification information of the first gaming chip information or the second gaming chip information.~~

~~13. The inspection system according to claim 1, wherein the first gaming chip information is included in respective radio tags of the gaming chips.~~

~~14. The inspection system according to claim 1, wherein~~

the first gaming chip information, the second gaming chip information, or both the first and second gaming chip information includes group information indicating respective groups to which respective ones of the gaming chips belong, and the groups are classified in accordance with respective values of the gaming chips, manufacturing times, manufacturers, use game halls, or a combination thereof.

15. The inspection system according to claim 1, wherein:

the second gaming chip information includes respective designated colors indicating respective values of the gaming chips on respective side surfaces of the gaming chips; and

the second reader comprises:

a camera configured to capture an image of the side surfaces of the gaming chips placed in the area; and

a processor that is configured to:

analyze the image captured by the camera;

identify and output the respective designated colors of each of the plurality of gaming chips based on the analysis; and

identify and output the respective values of the plurality of gaming chips in accordance with the identified designated colors.

16. The inspection system according to claim 15, wherein the designated colors are respectively interposed, in a thickness direction of the side surfaces of the gaming chips, between common colors which are commonly assigned to gaming chips having different values.

17. The inspection system according to claim 1, wherein:

the second gaming chip information is notation information inscribed on the side surfaces to be optically readable; and

the second reader comprises:

a camera that is configured to capture an image of the side surfaces of the gaming chips stacked and placed in the area; and

a processor configured to:

analyze the image captured by the camera;

based on the analysis, identify the respective notation information of each of the gaming chips; and

identify and output the second gaming chip information of each of the gaming chips in accordance with the identified notation information.

18. The inspection system according to claim 17, wherein:

the notation information is inscribed using infrared reaction ink that emits in response to infrared rays or using infrared absorption ink that absorbs infrared rays; and

the camera includes an infrared camera.

19. The inspection system according to claim 17, wherein:

the notation information is inscribed using ink that emits light in response to ultraviolet rays; and

the inspecting device further includes an ultraviolet irradiator that is configured to irradiate the side surfaces of the gaming chips with ultraviolet rays.

~~20. The inspection system according to claim 1, wherein:~~

~~the area is a case that has a seal which is broken when the case is opened to allow the gaming chips to be withdrawn from the case;~~

~~the inspecting device further comprises a sensor that is configured to detect whether the seal is unbroken; and~~

~~the processor is configured to determine that the gaming chips contained in the case are in the fail state when the unbroken seal is not detected by the sensor.~~

~~21. The inspection system according to claim 1, wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a number of the acquired first gaming chip information does not coincide with a number of the acquired second gaming chip information.~~

~~22. The inspection system according to claim 1, wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a number of the acquired first gaming chip information for a respective value does not coincide with a number of the acquired second gaming chip information for the respective value.~~

~~23. The inspection system according to claim 1, further comprising a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that in the pass state and those of the gaming chips that are in the fail state so that the gaming chips for which there is a lack of correspondence between the respective acquired first~~

~~gaming chip information and the respective acquired second gaming chip information are identifiable.~~

~~24. The inspection system according to claim 1, wherein:~~

~~both of the first gaming chip information and the second gaming chip information includes individual identification information individually identifying respective ones of the gaming chips; and~~

~~the inspection system further comprises a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that in the pass state and those of the gaming chips that are in the fail state so that the gaming chips in the fail state are identifiable when a plurality of piece of individual identification information of a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of piece of individual identification information of a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with each other.~~

~~25. The inspection system according to claim 1, further comprising:~~

~~a storage unit, wherein the storage unit is configured to store respective individual identification information of at least the first or the second gaming chip information of the gaming chips authorized to be placed in the area, and~~

wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a plurality of pieces of individual identification information of a plurality of pieces of the first gaming chip information acquired by the first reader or a plurality of piece of individual identification information of a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with a plurality of pieces of individual identification information of the first or the second gaming chip information stored in the storage unit.

26. The inspection system according to claim 1, further comprising:

a storage unit, wherein the storage unit is configured to store a correspondence relation between the first gaming chip information and the second gaming chip information, and wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with the correspondence relation stored in the storage unit.

27. The inspection system according to claim 1, further comprising:

a display; and

a storage unit;

wherein:

both of the first gaming chip information and the second gaming chip information include individual identification information individually identifying respective ones of the gaming chips;

the storage unit is configured to store respective individual identification information of at least the first or the second gaming chip information of the gaming chips authorized be placed in the area; and

the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that the gaming chips that are in the fail state can be identified when a plurality of pieces of individual identification information of the plurality of pieces of the first gaming chip information acquired by the first reader or a plurality of pieces of individual identification information of the plurality of pieces of the second gaming chip information acquired by the second reader does not coincide with the individual identification information of the first or the second gaming chip information stored in the storage unit.

28. The inspection system according to claim 1, further comprising:

a storage unit configured to store a correspondence relation between the first gaming chip information

and the second gaming chip information; and

a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that the gaming chips in the fail state can be identified when a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with the correspondence relation stored in the storage unit.

29. The inspection system according to claim 1, wherein:

the gaming chips include color information indicating respective values of the gaming chips as the second gaming chip information and include respective value information identifying respective values of the gaming chips as the first gaming chip information; and

the inspection system further comprises a display via which the inspection system is configured to display a result of the determination that distinguishes between the gaming chips in the pass state and the gaming chips in the fail state so that the gaming chips in the fail state can be identified when the respective color information of the gaming chips in the fail state does not coincide with the respective value information of the first gaming chip information of the gaming chips in the fail state.

~~30. The inspection system according to claim 1, wherein:~~

~~the area is a case that has a light transmitting part through which light transmits; and~~

~~the second reader is configured to optically read the surface of the gaming chips contained in the case through the light transmitting part.~~

~~31. The inspection system according to claim 30, wherein the light transmitting part is made of transparent material.~~

~~32. The inspection system according to claim 1, wherein:~~

~~the area is a case; and~~

~~the inspecting device further includes a receiving portion in which the case is received.~~

~~33. The inspection system according to claim 1, wherein the area is a portable case.~~

~~34. The inspection system according to claim 1, wherein the area comprises a two-tiered chip float or chip tray configured to hold the gaming chips at a game table.~~

1. An inspection system comprising:

an area on which a plurality of gaming chips is configured to be placed, each gaming chip of the plurality of gaming chips includes a radio frequency identification (RFID) tag; and

an inspecting device that includes:

a first sensing device, wherein the first sensing device is configured to acquire, by way of RFID, first gaming chip information from the

plurality of gaming chips placed in the area;

a second sensing device, wherein the second sensing device is configured to optically determine the presence or absence of a gaming chip placed in the area, wherein second gaming chip information indicates the determined presence or absence of the gaming chip; and

a processor, wherein the processor is configured to use the first gaming chip information acquired by the first sensing device and the second gaming chip information determined by the second sensing device to determine a damage status of the gaming chip placed in the area by combining (a) the first gaming chip information acquired by the first sensing device and (b) the second gaming chip information determined by the second sensing device.

2. The inspection system according to claim 1, wherein, to determine the damage status, the processor is further configured to, determine whether the gaming chip is damaged.

3. The inspection system according to claim 1, wherein, to determine the damage status, the processor is further configured to, (a) based on the acquired first gaming chip information and the second gaming chip information, determine for each of a plurality of chip values, a respective number of the gaming chips placed on the area that are assigned the respective chip value.

4. The inspection system according to claim 1, wherein each RFID tag is configured to stores individual

identification information individually identifying a respective gaming chip of the plurality of gaming chips.

5. The inspection system according to claim 4, further comprising:

a storage unit, wherein the storage unit is configured to store the individual identification information and the processor is configured to determine the damage status or a fake status when the individual identification information acquired by the first sensing device does not coincide with the individual identification information stored in the storage unit.

6. The inspection system according to claim 1, wherein each RFID tag is configured to store information indicated by designated colors that indicate respective values of the gaming chip that includes the RFID tag.

7. The inspection system according to claim 1, wherein:

the plurality of gaming chips include color information indicating respective values of the plurality of gaming chips, and include respective value information identifying respective values of the plurality of gaming chips as the first gaming chip information;

the second gaming chip information includes first color information of the gaming chip; and

the processor is configured to determine that a first set of the plurality of gaming chips placed on the area are in a fail state when the color information does not coincide with the value information of the first gaming chip information.

8. The inspection system according to claim 7, wherein:

the second gaming chip information further includes respective value information of the gaming chip in addition to the color information; and

the processor is configured to determine that a second set of the plurality of gaming chips placed on the area are in the fail state when a value of a respective one of the plurality of gaming chips indicated by the color information in the second gaming chip information of the respective gaming chip does not coincide with the value information of the second gaming chip information and/or the value information of the first gaming chip information.

9. The inspection system according to claim 8, wherein the processor is configured to determine a respective number of the plurality of gaming chips placed on the area for each of the values or a total amount of the values of all of the gaming chips based on the color information or the value information of the first gaming chip information or the second gaming chip information.

10. The inspection system according to claim 7, wherein:

the second gaming chip information further includes respective value information of the gaming chip in addition to the color information; and

the processor is configured to determine that a third set of the plurality of gaming chips placed on the area are in the fail state when the color information does not coincide with at least one of (a) the value information of the first or second gaming chip information, (b) common information of the first gaming chip information and the second

gaming chip information, or (c) individual identification information included in the first or second gaming chip information.

11. The inspection system according to claim 1, wherein the first gaming chip information is included in respective radio tags of the gaming chips.

12. The inspection system according to claim 1, wherein the first gaming chip information and/or the second gaming chip information include group information indicating respective groups to which respective ones of the gaming chips belong, and the groups are classified in accordance with respective values of the gaming chips, manufacturing times, manufacturers, and/or use game halls.

13. The inspection system according to claim 1, wherein:

the second gaming chip information includes respective designated colors indicating a respective value of the gaming chip on a respective side surface of the gaming chip; and

the second sensing device comprises:

a camera that is configured to photograph the side surface of the gaming chip placed on the area to capture an image; and

a second processor that is configured to:

perform an analysis on an image captured by the camera;

identify and output the respective designated colors of the gaming chip based on the analysis; and

identify and output the respective value of the gaming chip in accordance with the identified designated colors.

14. The inspection system according to claim 13, wherein the designated colors are respectively interposed, in a thickness direction of the side surface of the gaming chip, between common colors which are commonly assigned to gaming chips having different values.

15. The inspection system according to claim 1, wherein:

the second gaming chip information is notation information inscribed on a side surface of the gaming chip to be optically readable; and

the second sensing device comprises:

a camera that is configured to photograph the side surface of the gaming chip stacked and placed on the area to capture an image; and

a second processor configured to:

perform an analysis on the image captured by the camera;

based on the analysis, identify the respective notation information of the gaming chip; and

identify and output the second gaming chip information of the gaming chip in accordance with the identified respective notation information.

16. The inspection system according to claim 15, wherein:

the notation information is inscribed using infrared reaction ink that emits in response to infrared rays or using infrared absorption ink that absorbs infrared rays; and

the camera comprises an infrared camera.

17. The inspection system according to claim 15, wherein:

the notation information is inscribed using ink that

emits light in response to ultraviolet rays; and

the inspecting device further includes an ultraviolet irradiator that is configured to irradiate the side surfaces of the gaming chips placed on the area with ultraviolet rays.

18. The inspection system according to claim 1, wherein:

the area is a case that has a seal which is configured to be broken when the case is opened to allow the gaming chip to be withdrawn from the case;

the inspecting device further comprises a sensor that is configured to detect whether the seal is unbroken; and

the processor is configured to determine that the gaming chip is in a fail state when the unbroken seal is not detected by the sensor.

19. The inspection system according to claim 1, wherein the area is defined by a container.

20. The inspection system according to claim 19, wherein the container includes a case or a chip tray.

21. The inspection system according to claim 20, wherein the case is portable.

22. The inspection system according to claim 1, wherein the area includes a three-dimensional space.

23. The inspection system according to claim 22, wherein the first sensing device is configured to acquire the first gaming chip information of the gaming chip placed in the area, and the second sensing device is configured to optically read a side surface of the gaming chip placed in the area.

24. The inspection system according to claim 1, wherein the first sensing device is different from the second sensing device.

25. The inspection system according to claim 1, wherein the first sensing device includes a first camera and the second sensing device include a second camera.

26. The inspection system according to claim 25, wherein the first camera is different from the second camera.

27. The inspection system according to claim 1, wherein the first sensing device is configured to optically read the plurality of gaming chips and to acquire the first gaming chip information based on the optical read of the gaming chips, and the second sensing device is configured to acquire the second gaming chip information based on the optical read of a side surface of the gaming chip.

28. The inspection system according to claim 1, wherein, to optically read the plurality of gaming chips, the first sensing device is configured to capture a first image of the plurality of gaming chips, and, to optically read the plurality of gaming chips, the second sensing device is configured to capture a second image of the gaming chip.

29. The inspection system according to claim 28, wherein the first image is different from the second image.