

"PUSH-PULL AMPLIFIER"**2076605**

The invention relates to a push-pull amplifier arrangement having an input terminal, an output terminal, and first and second supply terminals, which arrangement comprises first and second transistors of one and the same conductivity type having their main current paths connected in series in a current path between said supply terminals in such manner that the collector of the first transistor is connected to the first supply terminal, the emitter of the second transistor is connected to the second supply terminal and the emitter of the first transistor is connected to the collector of the second transistor, a connection from the emitter of the first transistor to the output terminal, a first coupling from the input terminal to the base of the first transistor, a semiconductor junction included in said current path in such manner that it is poled in the forward direction for currents flowing in said main current paths, for generating a voltage which is a measure of the current flowing at the collector of a said transistor, a voltage measuring circuit constructed to generate at an output thereof a signal which is a function of voltage present between first and second input terminals thereof, which input terminals have said semiconductor junction included therebetween, and a second coupling from the output of said voltage measuring circuit to the base of said second transistor, which coupling is such that the resulting coupling from the input terminal to the base of the second transistor is inverting relative to the coupling from the input terminal to the base of the first transistor, the combination of said voltage measuring circuit and said second coupling including a third transistor of a conductivity type opposite to that of said first and second transistors, which third transistor is connected to operate in the common-base mode and is included in the signal path from the voltage measuring circuit input to the base of the second transistor.

A push-pull output stage of this general type is known from: "Electronics Letters" Vol. 10, No. 15 of 25 July 1974, pages 317, 318 and 319.

In order to enable the second transistor in this known circuit to be driven in a suitable manner the semiconductor junction is included in the collector circuit of the first transistor. The voltage across said junction, which is a measure of the current through the first transistor, is converted by the voltage measuring circuit (which in the known arrangement includes the third transistor) into a drive current which is in phase opposition to the input signal, and this drive current is applied from the third transistor to the base of the second transistor. As a result of this, any signal current through the second transistor will be in phase opposition to that through the first transistor.

If a push-pull amplifier arrangement of the said type is constructed as an integrated circuit the first and second transistors will generally be vertical npn transistors, whilst it will generally be necessary to employ a horizontal pnp transistor for the third transistor. As is known, such a horizontal pnp transistor is likely to have poor high-frequency properties. In order to mitigate the influence of said poor high-frequency properties in the known circuit arrangement it is advisable to bypass the emitter-collector path of the third transistor with a series combination of a resistor and a capacitor. However, the signal voltage on the emitter of the third transistor is generally insufficient to properly drive the second transistor via this series combination, so that the bandwidth and the drive range at high frequencies tend to be very limited.

In the known circuit the asymmetry of the voltage measuring circuit and, moreover, the fact that the second transistor is in practice driven via a resistor connected in parallel with its base-emitter junction give rise to a substantial dependence of the quiescent current setting on temperature and to non-linear signal transfer. Furthermore, the input impedance of the known circuit arrangement is highly dependent on the value of the input signal.

It is an object of the invention to provide a circuit arrangement of the type set forth in the opening paragraph, which can have an improved linearity, a larger bandwidth, and a substantially temperature-independent quiescent-current setting and the input impedance of which can be rendered substantially independent of the value of the input signal.

The invention provides a push-pull amplifier arrangement having an input terminal, an output terminal, and first and second supply terminals, which arrangement comprises first and second transistors of one and the same conductivity type having their main current paths connected in series in a current path between said supply terminals in such manner that the collector of the first transistor is connected to the first supply terminal, the emitter of the second transistor is connected to the second supply terminal and the emitter of the first transistor is connected to the collector of the second transistor, a connection from the emitter of the first transistor to the output terminal, a first coupling from the input terminal to the base of the first transistor, a semiconductor junction included in said current path in such manner that it is poled in the forward direction for currents flowing in said main current paths, for generating a voltage which is a measure of the current flowing at the collector of a said transistor, a voltage measuring circuit constructed to generate at an output thereof a signal which is a function of voltage present between first and second input terminals thereof, which input terminals have said semiconductor junction included therebetween, and a second coupling from the output of said voltage measuring circuit to the base of said second transistor, which coupling is such that the resulting coupling from the input terminal to the base of the second transistor is inverting relative to the coupling from the input terminal to the base of the first transistor, the combination of said voltage measuring circuit and said second coupling including a third transistor of a conductivity type opposite to that of said first and second transistors, which third transistor is connected to operate in the common-base mode and is included in the signal path from the voltage measuring circuit input to the base of

the second transistor, characterised in that said semiconductor junction is included between the collector of the second transistor and the connection from the emitter of the first transistor to the arrangement output terminal, said first and second input terminals have the series combination of said semiconductor junction and the base-emitter junction of said first transistor included therebetween so that said voltage measuring circuit will generate at its output a signal which is a function of the voltage across said series combination, said second coupling includes said third transistor and a series impedance in the signal path from the output of said voltage measuring circuit to the emitter of said third transistor, and a capacitor is included in parallel with the signal path through said series impedance and said third transistor.

By including the semiconductor junction between the collector of the second transistor and the connection from the emitter of the first transistor to the arrangement output terminal and by deriving the drive current for the second transistor by means of a voltage measuring circuit the input of which is connected in parallel with the series combination of the semiconductor junction and the base-emitter junction of the first transistor, it can be achieved that said drive current depends both on the current through the first and the current through the second transistor. Thus, the drive current can contain a component which also depends on the drive current itself. Because of the relative phasing there will be negative feedback, which can have a stabilizing effect on the quiescent-current setting and the current distribution between the first and the second transistor. The latter can result in a smooth cross-over.

A further advantage can be that, by shifting the measuring circuit input to the specified part of the circuit arrangement, a signal-voltage swing can be obtained between the measuring circuit and the first supply terminal, this allowing the higher frequencies of the signal voltage required for driving the second transistor to be obtained by means of the series impedance (suitably a resistor) via the capacitor.

The measuring circuit may comprise a second series combination of a second semiconductor junction and the base-emitter junction of a fourth transistor of the same conductivity type as said first and second transistors, said second series combination being included between said first and second input terminals in such manner that said second semiconductor junction and the base-emitter junction of said fourth transistor are poled in the same direction, as seen from said first and second input terminals, as are the first-mentioned semiconductor junction and the base-emitter junction of said first transistor, the collector of said fourth transistor constituting the output of said voltage measuring circuit.

Class-B operation can then be obtained by means of the two said junctions in the measuring circuit, which enable a signal suitable for feeding to the second transistor as a drive signal to become available in a high-impedance manner on the collector of the fourth transistor.

If this is the case the collector of the fourth transistor may be connected to the emitter of the third transistor via said series impedance and the common point of said series impedance and the emitter of the third transistor may be connected to the first supply terminal via a further impedance, suitably a current-source circuit.

In this way the phase reversal of the drive current necessary for class-B operation can be realized in a simple manner.

The base-emitter junction of the fourth transistor may be included between the second semiconductor junction and the base of the first transistor. Alternatively the second semiconductor junction may be included between the base-emitter junction of the fourth transistor and the base of the first transistor.

As previously mentioned, a further drawback of the push-pull output stage published in "Electronics Letters" is that the input impedance greatly depends on the value of the input signal. The cause of this is that when the first transistor supplies the load current to the output terminal only one current-amplifying semiconductor junction is included between the input terminal

and the output terminal, whilst when the second transistor supplies the load current two current-amplifying semiconductor junctions, namely the base-emitter junctions of the first and second transistors, are present in the signal path from the input to the output terminal, so that the input impedance in the last-mentioned case is higher by a factor of the order of magnitude of β (β being the current-gain factor of the first and second transistors) than in the case when the first transistor supplies the load current.

In order that an arrangement according to the present invention can have an input impedance which is substantially independent of the value of the input signal the measuring circuit may include the base-emitter junction of a fifth transistor of the same conductivity type as said first and second transistors, said fifth transistor being connected to operate in the common-collector mode and the base-emitter junction thereof being included between said second series combination and the base of said first transistor, the arrangement input terminal being coupled to the base of said first transistor via said fifth transistor in such manner that it is coupled to the arrangement output terminal via the first-mentioned semiconductor junction via the same number of active current-amplifying semiconductor junctions or equivalents thereof as that via which it is coupled to the arrangement output via the base-emitter junctions of the fifth and first transistors.

Such an arrangement may include a sixth transistor of the same conductivity type as the first and second transistors is included in the coupling from the arrangement input to the arrangement output, which transistor has its base connected to the arrangement input terminal, its emitter connected to the base of the fourth transistor and its collector connected to the emitter of the fifth transistor and to the base of the first transistor, the arrangement also including an impedance connecting the base of the fifth transistor to the first supply terminal, an impedance connecting the base of the fourth transistor to the second supply terminal, and a third semiconductor junction in the

connection between said second series combination and the base of said fifth transistor, said third semiconductor junction having the same polarity as that of the base-emitter junction of the fifth transistor as seen from the common point of the base of the fifth transistor and the third semiconductor junction. Because in such an arrangement the collector of the sixth transistor may carry substantially the same signal as its base, the influence of the "Miller" capacitance can be substantially reduced, so that considerably better high frequency properties can be obtained when driving the arrangement from a high-impedance signal source. Furthermore, because the collector current of the sixth transistor passes through the main current path of the fifth transistor, only one current source may be needed for biasing both the fifth and the sixth transistors.

As a modification, the base, emitter and collector of at least one of the aforesaid transistors may be replaced by the gate, source and drain respectively of a corresponding field-effect transistor.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings in which:

Figure 1 shows the circuit diagram of the aforesaid known push-pull output stage,

Figure 2 shows the circuit diagram of a first embodiment of the invention,

Figure 3 shows a variant of the circuit of Figure 2, and

Figure 4 shows the circuit diagram of another embodiment of the invention.

In the various Figures transistor T_1 and transistor T_2 are the two npn output transistors of a push-pull output stage, transistor T_1 being connected to operate in the common-collector mode. The collector of transistor T_1 is connected to a positive supply terminal 5 and its base is fed from an input 3. The emitter of transistor T_2 is connected to a negative supply terminal 10.

Transistor T_1 is employed as an emitter-follower for the input signal and transistor T_2 , which is connected to operate in the common-emitter mode, is employed as a controlled current source, it being driven

by a drive current which depends on the drive of transistor T_1 and which is applied to the base of transistor T_2 via a pnp transistor T_3 . Transistor T_3 is connected to operate in the common-base mode.

A known method of producing the said drive current can be found in said article in "Electronics Letters" and is shown in Figure 1. In Fig. 1 the collector of transistor T_1 is connected to the positive supply terminal 5 via a pnp transistor T_7 , which is connected as a diode poled in the forward direction. The emitter of transistor T_3 is connected to the base and collector of transistor T_7 , to the collector of transistor T_1 and to a terminal 4. The collector of transistor T_3 is connected to the negative supply terminal 10 via a resistor R_{12} and is also connected directly to the base of transistor T_2 and to a terminal 7. The base of transistor T_3 is connected to the negative supply terminal 10 via a resistor R_{11} and furthermore to the positive supply terminal 5 via a series combination of two pnp transistors T_8 and T_9 , which are connected as diodes poled in the forward direction. The base of transistor T_3 is thus maintained at a substantially constant potential relative to the positive supply terminal 5.

Assuming that the voltage on input 3 decreases from a high positive value, the collector current of transistor T_1 and thus the voltage across transistor T_7 will also decrease, causing the voltage across the base-emitter junction of transistor T_3 to increase in the forward direction. Eventually transistor T_3 is turned on (this corresponds to the start of the cross-over region) which results in the application of drive current to transistor T_2 , so that the last-mentioned transistor will supply the load current to an increasing extent as the voltage at terminal 3 is reduced further, as well as sufficient current to the emitter of transistor T_1 to maintain this transistor just conductive, thereby maintaining the coupling from terminal 3 to transistor T_2 .

The signal loop comprising the transistors T_1 , T_7 , T_3 and T_2 may therefore be regarded as a control loop, which ensures that transistor T_1 remains conductive. Because of the inevitable horizontal pnp transistor T_3 it is found that said control loop has poor high-frequency properties, which limit the bandwidth of the circuit and which are difficult to remedy. The inclusion of a series combination

of a resistor R_{13} and a capacitor C_1 between the terminals 4 and 7, as is recommended in said article published in "Electronics Letters", does not provide much improvement, because the signal voltage occurring on the emitter of transistor T_3 is insufficient to drive transistor T_2 at high frequencies via this series combination. At low frequencies T_2 is driven normally via transistor T_3 .

Further disadvantages are the non-linear transfer of signals from input to output and the temperature dependence of the quiescent-current setting, which are caused by the asymmetrical nature of the measuring circuit for the collector current of transistor T_1 , which circuit comprises the transistors T_3 , T_7 , T_8 and T_9 , and the presence of the resistor R_{12} .

Figure 2 shows a first embodiment of the invention. In the push-pull output stage of Fig. 2 the collector of transistor T_1 is connected directly to the positive supply terminal 5, its base is connected to the input 3 and its emitter to the output 1.

The emitter of the transistor T_2 is connected to the negative supply terminal 10. An npn transistor D_1 , connected as a diode poled in the forward direction, is included between the emitter of transistor T_1 and the collector of transistor T_2 in such a way that the common base-collector terminal of transistor D_1 is connected to the emitter of transistor T_1 and the emitter of transistor D_1 is connected to the collector of transistor T_2 .

A voltage measuring circuit M, which is included within a dashed line in Figure 2, comprises an npn transistor D_2 , which is connected as a diode, and the base-emitter junction of an npn transistor T_4 .

The emitter of transistor D_2 is connected to the emitter of transistor D_1 .

The emitter of transistor T_4 is connected to the common base-collector terminal of transistor D_2 and its base is connected to the base of transistor T_1 .

The emitter of transistor T_3 is connected to the collector of transistor T_4 via a resistor R_1 and to the positive supply

terminal 5 via a current source circuit SB_1 . Its base is connected to a constant voltage V_{ref} .

The collector of transistor T_3 is connected to the base of transistor T_2 and, via a current source circuit SB_2 , to the negative supply terminal 10. It should be noted that the current source circuit SB_1 may alternatively be connected between the positive supply terminal 5 and the collector of transistor T_4 . A terminal 6 is connected to the collector of transistor T_4 and a terminal 7 is connected to the collector of transistor T_3 .

The circuit operates as follows:

The measuring circuit M, enclosed within a dashed line in Figure 2, causes a drive current I_s which depends on the voltage between the base of transistor T_1 and the emitter of transistor D_1 to become available in a high-impedance manner on the collector of transistor T_4 . Phase inversion of the drive current I_s is achieved by subtracting it from the current I_1 supplied by the current source circuit SB_1 and applying the resulting difference current I_v to the emitter of transistor T_3 . Said difference current I_v , after the loss of a fraction equal to the base current of transistor T_3 , is applied to the base of transistor T_2 via the emitter-collector path of transistor T_3 and after subtraction from it of the current I_2 supplied by the current source circuit SB_2 . The customary class-B operation is obtained in that, because of the action of the control loop comprising the measuring circuit, the coupling including transistor T_3 , and transistor T_2 , the sum of the voltages across the base-emitter junction of transistor T_1 and diode-connected transistor D_1 is maintained substantially constant, the quiescent-current setting being mainly determined by the magnitude of the currents I_1 and I_2 which are supplied by the current-source circuits SB_1 and SB_2 respectively.

The effect of the poor high-frequency properties of the horizontal pnp transistor T_3 can be eliminated by including a capacitor C_2 between the terminals 6 and 7, so that for high frequencies the resistor R_1 and the transistor T_3 are bypassed.

Since the drive current I_g produces sufficient signal voltage across the resistor R_1 to drive transistor T_2 via capacitor C_2 , the circuit also performs satisfactorily at high frequencies.

5 Figure 3 shows a variant of the circuit arrangement of Figure 2. In this variant a voltage measuring circuit M is again indicated by a dashed line. The common base-collector terminal of transistor D_2 is now connected to the base of transistor T_1 and input 3. The emitter of transistor D_2 is now connected to the
10 base of transistor T_4 and the emitter of transistor T_4 is now connected to the emitter of transistor D_1 . With this variant it is advisable to include a current source SB_4 , shown dashed in Figure 3, in order to obtain sufficient quiescent current in the output stage. For the remainder the design and operation of
15 this circuit arrangement are the same as for that of Figure 2. The properties of the two circuits only differ with respect to the input impedance, which for the circuit of Fig. 3 is slightly lower than for the circuit of Figure 2. The contribution of the impedance of diode-connected transistor D_2 to the input impedance
20 of the push-pull output stage in the circuit of Figure 2 is approximately β times that for the variant of Figure 3.

Figure 4 shows another embodiment of the invention which has an input impedance which is substantially independent of the value of the input signal. In comparison with the push-pull output
25 stage of Figure 3 the circuit has been extended by means of npn transistors T_5 and T_6 , an npn transistor D_3 , which is connected as a diode, and current-source circuits SB_3 and SB_4 . The base of transistor T_6 is connected to the input 3, its emitter is connected to the base of transistor T_4 via a junction point 11, and its
30 collector is connected to the emitter of transistor T_5 and to the base of transistor T_1 .

The collector of transistor T_5 is connected to the positive supply terminal 5 directly and its base is connected to the positive supply terminal 5 via the current-source circuit SB_3 .

35 The junction point 11 is connected to the negative supply

terminal 10 via current-source circuit SB_4 and a series combination of transistors D_2 and D_3 , which are connected as diodes, is included between the base of transistor T_5 and the junction point 11 in such a way that these transistors are poled in the forward direction.

In the push-pull amplifier arrangement of Fig. 4 a signal path is formed between input 3 and the base of transistor T_1 by the base-emitter junction of transistor T_6 , the diode-connected transistors D_2 and D_3 , and the base-emitter junction of transistor T_5 .

A voltage measuring circuit M, which is denoted by a dashed line in Figure 4, comprises the base-emitter junction of transistor T_4 , the diode-connected transistors D_2 and D_3 , and the base-emitter junction of transistor T_5 .

Apart from the advantages of the circuit arrangements of Figures 2 and 3 the embodiment of Fig. 4 has the major advantage that its input impedance is high (because of the input emitter follower transistor T_6) and is substantially independent of the value of the input signal (because the signal path from the input 3 to the output 1 via the base-emitter junction of transistor T_6 , the base-emitter junction of transistor T_4 and the diode-connected transistor D_1 passes through two amplifying semiconductor junctions plus one equivalent thereof, and the signal path from the input 3 to the output 1 via the base-emitter junction of transistor T_6 , transistors D_2 and D_3 , the base-emitter junction of transistor T_5 and the base-emitter junction of T_1 passes through three current-amplifying semiconductor junctions; it should be noted that the signal current amplified by transistor T_1 passes through transistor D_1 so that with respect to its impedance transistor D_1 behaves as a current-amplifying semiconductor junction and may therefore be regarded as an equivalent thereof).

Further advantages of the arrangement of Fig. 4 are that the input capacitance of the circuit is substantially reduced by compensation for the effect of the "Miller" capacitance C_M

of transistor T_6 , this being an advantage in the case of a high-impedance drive of the arrangement. This is achieved because the collector of transistor T_6 is supplied with substantially the same signal via the signal path constituted by transistors D_2 and D_3 and the base-emitter junction of transistor T_5 as that which is present on the emitter of transistor T_6 and thus on its base. Moreover, because the collector current of transistor T_6 passes through the main current path of transistor T_5 , only one current source circuit is needed for biasing both transistors T_5 and T_6 .

It will be appreciated that one or more of the bipolar transistors of Figs. 2-4 may be replaced by a corresponding field-effect transistor. Furthermore, a resistor may be included in series with the various capacitors C_2 , for example for stabilisation reasons.

**CLAIMS:**

1. A push-pull amplifier arrangement having an input terminal, an output terminal, and first and second supply terminals, which arrangement comprises:

- 5 first and second transistors of one and the same conductivity type having their main current paths connected in series in a current path between said supply terminals in such manner that the collector of the first transistor is connected to the first supply terminal, the emitter of the second transistor is connected
- 10 to the second supply terminal and the emitter of the first transistor is connected to the collector of the second transistor, a connection from the emitter of the first transistor to the output terminal,
- a first coupling from the input terminal to the base of the
- 15 first transistor,
- a semiconductor junction included in said current path in such manner that it is poled in the forward direction for currents flowing in said main current paths, for generating a voltage which is a measure of the current flowing at the collector of a said transistor,
- 20 a voltage measuring circuit constructed to generate at an output thereof a signal which is a function of voltage present between first and second input terminals thereof, which input terminals have said semiconductor junction included therebetween, and
- a second coupling from the output of said voltage measuring
- 25 circuit to the base of said second transistor, which coupling is such that the resulting coupling from the input terminal to the base of the second transistor is inverting relative to the coupling from the input terminal to the base of the first transistor, the combination of said voltage measuring circuit and said second coupling
- 30 including a third transistor of a conductivity type opposite to that of said first and second transistors, which third transistor



is connected to operate in the common-base mode and is included in the signal path from the voltage measuring circuit input to the base of the second transistor,

characterised in that said semiconductor junction is included
5 between the collector of the second transistor and the connection from the emitter of the first transistor to the arrangement output terminal,

said first and second input terminals have the series combination of said semiconductor junction and the base-emitter
10 junction of said first transistor included therebetween so that said voltage measuring circuit will generate at its output a signal which is a function of the voltage across said series combination,

said second coupling includes said third transistor
15 and a series impedance in the signal path from the output of said voltage measuring circuit to the emitter of said third transistor, and

a capacitor is included in parallel with the signal path through said series impedance and said third transistor.

2. An arrangement as claimed in Claim 1, characterised in
20 that the measuring circuit comprises a second series combination of a second semiconductor junction and the base-emitter junction of a fourth transistor of the same conductivity type as said first and second transistors, said second series combination
25 being included between said first and second input terminals in such manner that said second semiconductor junction and the base-emitter junction of said fourth transistor are poled in the same direction, as seen from said first and second input terminals, as are the semiconductor junction specified in Claim 1 and the
30 base-emitter junction of said first transistor, the collector of said fourth transistor constituting the output of said voltage measuring circuit.

3. An arrangement as claimed in Claim 2, characterised in
that the collector of the fourth transistor is connected to the
35 emitter of the third transistor via said series impedance,



(29)

and the common point of said series impedance and the emitter of the third transistor is connected to the first supply terminal via a further impedance.

4. An arrangement as claimed in Claim 3, characterised in that said further impedance is a constant current source circuit.

5. An arrangement as claimed in Claim 2, Claim 3 or Claim 4, characterised in that the base-emitter junction of the fourth transistor is included between the second semiconductor junction and the base of the first transistor.

6. An arrangement as claimed in Claim 2, Claim 3 or Claim 4, characterised in that the second semiconductor junction is included between the base-emitter junction of the fourth transistor and the base of the first transistor.

7. An arrangement as claimed in any of Claims 2 to 4 or Claim 6, characterised in that the measuring circuit includes the base-emitter junction of a fifth transistor of the same conductivity type as said first and second transistors, said fifth transistor being connected to operate in the common-collector mode and the base-emitter junction thereof being included between said second series combination and the base of said first transistor, the arrangement input terminal being coupled to the base of said first transistor via said fifth transistor in such manner that it is coupled to the arrangement output terminal via the semiconductor junction specified in Claim 1 via the same number of active current-amplifying semiconductor junctions or equivalents thereof as that via which it is coupled to the arrangement output via the base-emitter junctions of the fifth and first transistors.

8. An arrangement as claimed in Claim 7 when appended to Claim 6, characterised in that a sixth transistor of the same conductivity type as the first and second transistors is included in the coupling from the arrangement input to the arrangement output, which transistor has its base connected to the arrangement input terminal, its emitter connected to the base of the fourth transistor and its collector connected to the emitter of the fifth transistor and to the base of the first transistor, the



arrangement also including an impedance connecting the base of the fifth transistor to the first supply terminal, an impedance connecting the base of the fourth transistor to the second supply terminal, and a third semiconductor junction in the connection between said second series combination and the base of said fifth transistor, said third semiconductor junction having the same polarity as that of the base-emitter junction of the fifth transistor as seen from the common point of the base of the fifth transistor and the third semiconductor junction.

9. An arrangement as claimed in Claim 8, characterised in that the impedances specified in Claim 8 are constant current source circuits.

10. A modification of an arrangement as claimed in any preceding claim, wherein the base, emitter and collector of at least one of the said transistors are replaced by the gate, source and drain respectively of a corresponding field-effect transistor.

11. A push-pull amplifier arrangement substantially as described herein with reference to Fig. 2, Fig. 3 or Fig. 4 of the drawings.

The text of the specification has been reproduced by photocopying the applicants original typescript. It may contain a few amendments which are difficult to read. The original typescript containing these amendments may be inspected on the premises of the Patent Office