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PATENT SPECIFICATION

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(19)

(54) CHARGE TRANSFER DEVICE

(71) We, HEWLETT-PACKARD COMPANY, of 1501 Page Mill Road, Palo Alto, California 94304, United States of America, a corporation organized and existing under the laws of the State of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to charge transfer devices.

Charge transfer devices are semiconductor devices which operate to store clumps of charge in localized regions of a semiconductor and to transfer the stored charge systematically from one region to another. A typical MOS charge transfer device consists of an array of metal electrodes overlayed on a dielectric layer which is itself deposited on a semiconductor substrate. The device operates by storing minority carriers in the semiconductor substrate in localized regions under certain ones of the metal electrodes. In one type of device, commonly called an interface device, the charge is stored at the boundary between the dielectric layer and the semiconductor substrate. In another type of device, called a bulk device, the stored charge is instead distributed in the semiconductor to some distance below the dielectric semiconductor interface. In both types of devices, the charge is localized by applying external voltages to the electrodes to create potential minima (potential wells) in the semiconductor substrate in the vicinity of the electrodes. By suitably varying the voltages on the different electrodes, the potential minima can be moved from one electrode to the next, thereby inducing a transfer of the stored charge from one region to another.

In all charge transfer devices, it is important that the transfer of charge be directional; i.e. the charge must be transferred in one direction only, with no charge "spilling backward" in the opposite direction when a transfer in the preferred direction is effected. A basic method to achieve directional charge transfer is to use a three phase device in which every third electrode is connected in common. When charge is transferred, the three phase voltage operates to establish a very shallow potential well under the electrodes adjacent on one side to those electrodes beneath which charge was initially stored. This shallow potential well acts as a "potential shoulder" to prevent charge from spilling backwards when it is transferred in the preferred direction.

However, it is often desirable to provide directionality without the complexity inherent in a three-phase system. Thus, in the prior art there have been developed various schemes for prviding directionality in a charge transfer device which uses a simpler two-phase system to store and transfer charge. Some of these two phase devices operate by segmenting each electrode into two associated sections. Typically, it is provided that there is maintained between the two associated sections a potential difference. Thus, when the two-phase system changes phase, the voltage on each of the associated sections of an electrode vary in tandem, there being always a potential difference between them. This potential difference functions as the required potential shoulder to prevent charge from slipping backwards when it is transferred from the region beneath one electrode to the region beneath an adjacent electrode. One difficulty with two-phase charge transfer devices of this type is that to create the tandem variation of voltages on two sections of an electrode, there is typically required the use of four different electrical bus lines and associated interconnections between those lines and

the electrodes. This problem is especially important when a charge transfer device is arranged on a semiconductor chip to use in a computer memory, since much of the space on the semiconductor chip which would otherwise be available as memory storage is instead occupied by the various bus lines and interconnections.

In devices of the interface type, there has been another serious problem of losses occuring at the dielectric semiconductor boundary during transfer of charge. These losses have been found to be very significant in regions in which charge is transferred through, but not stored. The problem is evidently caused by trapping centers existing at the dielectric semiconductor interface which slows down the transfer of charge sufficiently so that some charge can slip backwards over the potential shoulders, thereby causing a degradation in the transfer signal. To overcome this problem, it is known to modify the charge transfer device so that charge is stored and transferred at some distance beneath the dielectric semiconductor boundary rather than at the boundary itself. This has been accomplished for example, by doping the semiconductor substrate near the interface with ions of a conductivity type opposite that of the bulk substrate. For example, phosphorus has been implanted in p-type silicon substrates. However, in order to insure that the minority carriers are stored and transferred at some distance below the surface, it is necessary that the concentration of the implanted ions be higly nonuniform as a function of depth beneath the surface. Typically the concentration is low near the surface rising to some peak value at some distance below the surface, and then falling again. Such nonuniform doping is a complicated and expensive procedure. Additionally, it has been found that while doping of the substrate with ions of an opposite conductivity type increases the minority charge carrying capability of the device, the non-uniform doping required in the prior art is not optimal insofar as increasing the charge carrying capability is concerned. It would therefore be desirable to increase the charge carrying capability by uniformly doping the upper region of the substrate, while also providing that in regions where losses are very significant, the minority charge carriers are transferred at some distance below the surface of the substrate.

The present invention provides a semiconductor charge transfer device for storing and transferring charge comprising: a substrate layer of a semiconductor material of a first conductivity type; a first insulating layer on said substrate layer; a plurality of electrodes on said first insulating layer, for inducing an electrical potential distribution in said substrate layer in response to electrical voltages applied to said electrodes; a region of ions of a second conductivity type opposite to said first conductivity type implanted in said substrate layer to a predetermined depth below the entire boundary between said first insulating layer and said substrate layer; a plurality of regions of ions of said first conductivity type implanted in said substrate layer to a depth less than said substrate depth, each of said plurality of regions being positioned in spatial relation with a portion of an associated one of said plurality of electrodes, for diverting the charge under transfer below the boundary between said first insulating layer and said substrate layer into the bulk of said region of ions of the second conductivity type beneath each of said plurality of regions and for altering the electrical potential distribution in said substrate layer to provide directionality to the transfer of charge.

Preferably a second insulating layer is included on said first insulating layer, and each electrode of said plurality of electrodes comprising two sections spatially separated from each other by said second insulating layer.

Said two sections of each electrode may be electrically interconnected with each other, whereby a voltage applied to one section will be applied also to the other section.

Preferably said substrate layer is made of a semicondutor material selected from silicon, GaAs and GaP; said ions of a second conductivity type are selected from phosphorus, arsenic and antimony and said ions of said first conductivity type are selected from boron, gallium and indium.

In accordance with the illustrated preferred embodiments, the present invention provides a charge transfer device in which ions of one conductivity type are implanted in a semiconductor substrate of the opposite conductivity type to some distance below a boundary between a dielectric layer and the semiconductor substrate. This doping substantially increases the charge carrying capability of the device. In accordance with the preferred embodiment of the device there are also implanted in selected regions of the semiconductor substrate, ions of the same conductivity type as that of the bulk substrate. This latter implantation is done by doping the substrate with ions near the dielectric-substrate interface, but only in certain regions where very significant losses occur, e.g. in those regions through which charge is transferred but not stored. In operation the ion doping in these selected regions repels charge from

the dielectric-substrate boundary into the bulk of the semiconductor substrate. In effect then, the charge which is being transferred "ducks under" the surface at those places where the most significant losses would otherwise occur.

The selective doping of the present invention with ions of the same type as the substrate accomplishes yet another purpose; by suitably varying the concentration of the ions of the same conductivity type as the substrate, the doping may be used to vary the depth of the potential wells in certain regions of the semiconductor substrate. Thus, the same doping which minimizes charge losses at the insulator-semiconductor interface can also provide a "potential shoulder" necessary to insure directionality of the charge transfer.

There now follows a detailed description which is to be read with reference to the accompanying drawings of a charge transfer device according to the present invention; it is to be clearly understood that this device has been selected for description to illustrate the invention by way of example and not by way of limitation.

In the drawings:—

Figure 1 is a cross-sectional view of a charge transfer device in accordance with the preferred embodiment of the invention; and

Figure 2 is a graph on which is plotted typical concentration of doped ions in a substrate of a charge transfer device according to the present invention.

In Figure 1 there is shown a section of a charge transfer device including a substrate layer 11 of a semiconductor material, for example silicon, GaAs, GaP or other suitable semiconductor materials known in the art. Deposited onto the substrate layer 11 is a first insulating layer 13 of a dielectric material, which may be, for example, SiO_2, Si_3N_4, Al_2O_3, or other suitable dielectric materials. Overlayed on the insulating layer 13 is an array of electrodes which are driven by a two-phase voltage source (not shown). In accordance with a preferred embodiment of the invention, each of the electrodes in the array comprises two sections separated by a second insulating layer 15, which may be constructed from materials such as SiO_2, Si_3N_4, Al_2O_3 or other suitable dielectric materials. Three electrodes of the array are illustrated, the two sections of the first electrode being labelled 17A and 17B, while the sections of the second and third electrodes are labelled 19A, 19B and 21A, 21B, respectively. In Figure 1, the two sections of each electrode are shown as being electrically connected to a single voltage line representing one phase of a two-phase voltage source. Alternate electrodes are connected to alternate phases of the source, so that the electrode 17 is connected with a voltage line representing a phase ϕ_1, the electrode 19 is connected to a voltage line representing the phase ϕ_1. Other electrode arrangements are possible and may be appropriate for certain situations. The electrodes of a charge transfer device according to the present invention may be constructed, for example from materials such as polysilicon or a thin metal layer (thickness of a few thousand Å). In the illustrated embodiment, typical dimensions of the electrodes are about 10μm by 5μm, while the spacing between corresponding sections of adjacent electrodes may be about 5μm.

Although the principles of the invention may be applied in an N-channel charge transfer device or a P-channel transfer device, an N-channel device will be described for purposes of illustration. In an N-channel device, the substrate layer 11 is fabricated from a P-type material such as Si, GaAs, or GaP, or other suitable P-type materials as described above. Typically, the depth of the substrate layer 11 is about 250—500μm. A layer of donor ions 23 of an N-type material such as phosphorus, or As or Sb is implanted in the substrate layer 11 to a distance of about 0.5—1μm below the insulator-substrate boundary 14. The phosphorus implantation may be accomplished by doping the substrate layer 11 directly through the layer 13 before the electrodes are laid on the dielectric layer 13. According to the invention, the entire active surface is uniformly doped with donor ions to provide a region or layer 23. In accordance with the invention, acceptor ions are then implanted in selected regions 25 of the substrate layer 11 immediately below the insulator-substrate boundary 14. For reasons which will become clear below, the selected regions 25 in which acceptor ions are implanted are preferably located below the electrode sections 17B, 19B and 21B. An advantageous method for implanting the acceptor ions is to deposit a first electrode layer including the electrode sections 17A, 19A and 21A on the insulating layer 13. This electrode layer may then itself serve as a mask for the implantation of acceptor ions thereby eliminating the need for an additional masking step. Acceptor ions of a material such as boron, or Ga, or In are implanted into the regions 25 of the substrate layer 11 to a depth of about 0.1μm below the insulator-substrate boundary 14. The insulating layer 15 is then deposited on the device, after which the electrode layer

including the sections 17B, 19B and 21B is deposited onto the insulating layer 15 to complete fabrication of a charge transfer chip.

The selective implanting of regions 25 of acceptor ions in the layer 23 of donor ions serves several different functions in the charge transfer device. First, the fixed charges implanted in the selected regions 25 serve to reduce depth of potential wells generated in these regions of the substrate layer 11 by voltages applied to the various electrodes described above. Thus, it is possible to create the "potential shoulders" required for directionality of charge transfer without maintaining a potential difference between the two sections of each electrode. Thus, both sections of each electrode may be driven by the same potential, such as is illustrated by the electrode sections 17A and 17B being connected to the voltage line representing a phase 0_1 of a two-phase voltage source. Although the ration of the voltages on these electrodes is unity, the fixed negative charge implanted in the regions 25 of the substrate layer 11, acts to reduce the potential wells seen in those regions, thereby creating a "potential shoulder" to insure dirctionally of charge transfer. Superfluous electrical bus lines and interconnections are thereby eliminated, resultng in more space on each semiconductor utilizable for memory storage or the like. In the illustrated embodiment, a part of the difference in potential well depth seen in the substrate layer 11 below the electrode sections 17A and 17B is also accounted for by the fact that the electrode section 17B is further displaced from the substrate 11 than is the electrode section 17A. In devices which have been constructed without selective implantation of acceptor ions (using an insulating layer 15 of thickness of about 3000 Å) ratio of voltage on the two sections of each electrode of about 3.3 were required to provide sufficiently adequate "potential shoulders" in the substrate layer 11 to insure directionality to charge transfer. However, when boron ions were selectively introduced into the regions 25 of the substrate layer 11 as described above, in concentrations on the surface of about 10 to 20 times the substrate concentration, and to a depth of about 1000 Å it was found possible to have the voltage ratios on the two sections of each electrode at unity.

In addition to providing a "potential shoulder" for directionality of charge transfer, the acceptor ion implant in the regions 25 also serves to greatly increase the charge transfer efficiency. In the absence of an implantation of acceptor ions, charge transfer would occur at least in part at the boundary 14 between the insulating layer 13 and the substrate layer 11. In the regions 25 beneath the electrode sections 17B, 19B and 21B where charge is not stored, but only transferred through, the effect of trapping centers at the surface appears to slow down the transfer of charge sufficiently so that some charge can slip backwards during transfer. However, if selective implantation of acceptor ions is performed according to the invention, then charge in the regions 25 is deflected beneath the surface and transferred in the bulk of the substrate layer 11, as indicated by the arrows 27, thereby reducing losses that would otherwise occur at the surface.

The invention thus combines increased charge carrying capacity provided by a uniform implantation of a layer 23 of donor ions with increased efficiency resulting from the buried channel charge transfer of charge in the regions 25 where surface losses would otherwise be important.

In Figure 2 there is shown a graph on which are plotted the concentrations of the various donor and acceptor ions as a function of depth in the substrate layer 11 below the insulator-substrate boundary 14. A straight line 31 indicates a uniform doping of the substrate with P-type acceptor ions in a concentration of about $1.10^{15}/cm^3$. A curve 33 represents the doping of a layer of a donor ions of approximately uniform concentration of about $3.10^{16}/cm^3$ to a depth of about 0.5—1.0 μm. A curve 35 represents the concentration of acceptor ions doped in regions 25 of Figure 1. As indicated by the curve, the concentration of acceptor ions at the surface is about $1—2.10^{16}/cm^3$ falling off to substrate concentration at a depth of about 1000 Å.

As was mentioned above, a charge transfer device according to the present invention may also be constructed which is a P-channel device; i.e. the substrate material would be an N-type material such as P or As doped, while the layer 23 would comprise a P-type material such as B or Ga doped. Suitable materials for the selective doping of the regions 25 would be P or As or Sb.

WHAT WE CLAIM IS:—

1. A semiconductor charge transfer device for storing and transferring charge comprising:

a substrate layer of a semiconductor material of a first conductivity type;

a first insulating layer on said substrate layer;

a plurality of electrodes on said first insulating layer, for inducing an electrical potential distribution in said substrate layer

including the sections 17B, 19B and 21B is deposited onto the insulating layer 15 to complete fabrication of a charge transfer chip.

The selective implanting of regions 25 of acceptor ions in the layer 23 of donor ions serves several different functions in the charge transfer device. First, the fixed charges implanted in the selected regions 25 serve to reduce depth of potential wells generated in these regions of the substrate layer 11 by voltages applied to the various electrodes described above. Thus, it is possible to create the "potential shoulders" required for directionality of charge transfer without maintaining a potential difference between the two sections of each electrode. Thus, both sections of each electrode may be driven by the same potential, such as is illustrated by the electrode sections 17A and 17B being connected to the voltage line representing a phase 0_1 of a two-phase voltage source. Although the ration of the voltages on these electrodes is unity, the fixed negative charge implanted in the regions 25 of the substrate layer 11, acts to reduce the potential wells seen in those regions, thereby creating a "potential shoulder" to insure dirctionally of charge transfer. Superfluous electrical bus lines and interconnections are thereby eliminated, resultng in more space on each semiconductor utilizable for memory storage or the like. In the illustrated embodiment, a part of the difference in potential well depth seen in the substrate layer 11 below the electrode sections 17A and 17B is also accounted for by the fact that the electrode section 17B is further displaced from the substrate 11 than is the electrode section 17A. In devices which have been constructed without selective implantation of acceptor ions (using an insulating layer 15 of thickness of about 3000 Å) ratio of voltage on the two sections of each electrode of about 3.3 were required to provide sufficiently adequate "potential shoulders" in the substrate layer 11 to insure directionality to charge transfer. However, when boron ions were selectively introduced into the regions 25 of the substrate layer 11 as described above, in concentrations on the surface of about 10 to 20 times the substrate concentration, and to a depth of about 1000 Å it was found possible to have the voltage ratios on the two sections of each electrode at unity.

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The invention thus combines increased charge carrying capacity provided by a uniform implantation of a layer 23 of donor ions with increased efficiency resulting from the buried channel charge transfer of charge in the regions 25 where surface losses would otherwise be important.

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As was mentioned above, a charge transfer device according to the present invention may also be constructed which is a P-channel device; i.e. the substrate material would be an N-type material such as P or As doped, while the layer 23 would comprise a P-type material such as B or Ga doped. Suitable materials for the selective doping of the regions 25 would be P or As or Sb.

WHAT WE CLAIM IS:—

1. A semiconductor charge transfer device for storing and transferring charge comprising:

a substrate layer of a semiconductor material of a first conductivity type;

a first insulating layer on said substrate layer;

a plurality of electrodes on said first insulating layer, for inducing an electrical potential distribution in said substrate layer

in response to electrical voltages applied to said electrodes;

a region of ions of a second conductivity type opposite to said first conductivity type implanted in said substrate layer to a predetermined depth below the entire boundary between said first insulating layer and said substrate layer;

a plurality of regions of ions of said first conductivity type implanted in said substrate layer to a depth less than said predetermined depth, each of said plurality of regions being positioned in spatial relation with a portion of an associated one of said plurality of electrodes, for diverting the charge under transfer below the boundary between said first insulating layer and said substrate layer into the bulk of said regions of ions of the second conductivity type beneath each of said plurality of regions and for altering the electrical potential distribution in said substrate layer to provide directionality to the transfer of charge.

2. A semiconductor charge transfer device according to claim 1 wherein a second insulating layer is included on said first insulating layer, and each electrode of said plurality of electrodes comprises two sections spatially separated from each other by said second insulating layer.

3. A semiconductor charge transfer device according to claim 2 wherein said two sections of each electrode are electrically interconnected with each other, whereby a voltage applied to one section will be applied also to the other section.

4. A semiconductor charge transfer device according to any one of the preceding claims where said substrate layer is made of a semiconductor material selected from silicon, GaAs and GaP;

said ions of a second conductivity type are selected from phosphorus, arsenic and antimony and

said ions of said first conductivity type are selected from boron, gallium and indium.

5. A semiconductor charge transfer device according to claim 1 substantially as hereinbefore described with reference to the accompanying drawings.

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