

Abstract

**MULTIPLE VOLTAGE SUPPLIES FOR FIELD
PROGRAMMABLE GATE ARRAYS AND THE LIKE**

A field programmable array of application circuitry (C1,C2,...) is
5 programmed (or reprogrammed) by first applying application circuitry power supply
($AV_{dd}=5v$) to the application circuitry, and then applying a binary digital data signal
(D0/D1) through the source-drain path of an access transistor (N3) in its on condition
to the SRAM that controls the on/off condition of its associated controlled pass
transistor (N4). This SRAM is one of a row-column array of similar SRAMs, and
10 the access transistors for all SRAMs on the same row are similarly supplied with
data signals through access transistors. The pass transistor determines whether
application circuitry interconnection points (A1,A2), are going to be connected after
the programming (or reprogramming) is terminated. While the data signal (D0/D1)
is applied to the SRAM, and the power supply (PV_{DD}) for the SRAM is maintained
15 at an intermediate level (3v) below the level of the application circuitry power
supply voltage ($AV_{dd}=5v$) and below the high binary level (D1), a row-select pulse
(S) is applied to a control terminal of the access transistor, as well as to all control
terminals of access transistors for accessing all other SRAMs on the same row. The
row-select pulse (S) is then terminated and the SRAMs on other rows (if need be) are
20 similarly written (or re-written). Then the power supply (PV_{DD}) for the SRAMs is
increased to a level ($PV_{DD}=6v$) advantageously higher, by a threshold of the pass
transistor (N4), than that of the application circuitry ($AV_{dd}=5v$), to reduce both
voltage drops and power losses in pass transistors.

This Sheet Has Been Replaced

