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DRAWINGS ATTACHED

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(54) AUTOMATIC GAIN CONTROL CIRCUIT

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to automatic gain control (AGC) circuits, and more particularly, to impulse noise protected AGC circuits for television receivers. AGC circuits embodying the invention are particularly suitable for fabrication using integrated circuit techniques.

As used herein, the term integrated circuit refers to a unitary or monolithic semiconductor device or chip which is the equivalent of a network of interconnected active and passive circuit elements.

AGC circuits are commonly used in television receivers to derive a suitable control voltage for application to the radio frequency (RF) and intermediate frequency (IF) amplifier stages of the receiver. The control voltage is effective to vary the gain of these stages inversely with respect to the level of the synchronizing pulse components of a detected video signal. Thus, a constant amplitude detected video output signal is provided. The synchronizing pulse components of the video signal are thereafter separated and used for synchronizing the horizontal and vertical oscillators associated with the respective horizontal and vertical sweep circuits of the receiver.

Noise pulses having amplitudes greater than the amplitude of the synchronizing pulses often become super-imposed on the received composite television signal and may cause the generation of an incorrect automatic gain control voltage for the receiver and thus cause improper amplification of the received signal. Additionally, noise in the received television signal may tend to upset the synchronization of either the horizontal or vertical sweep circuits of the receiver with resulting picture deterioration.

[*Price 25p*]

While various AGC circuits having impulse noise protection or immunity are known, their application for fabrication in integrated circuits have heretofore been impractical. This has been due to several of the limitations involved in the utilization of integrated circuits—namely, the difficulty in fabricating the relative large valued capacitors required and/or the relative scarcity, due to economic and packaging design considerations, of available terminals on an integrated circuit for connection thereto of discrete large valued capacitors.

It is therefore an object of this invention to provide an improved automatic gain control circuit suitable for fabrication on an integrated circuit and which reduces the effects of impulse noise.

With the above object in mind, the present invention consists of an automatic gain control circuit for a television receiver including means for providing from a received signal a video signal with recurrent synchronizing signal components which may be accompanied by impulse noise and a source of recurrent voltage pulses coincident with the synchronizing pulses components. Gain control means are provided, responsive to the synchronizing signal components of the video signal. The gain control means are also responsive to the recurrent voltage pulses and undesirably responsive to the impulse noise for developing an automatic gain control voltage. Protection means are provided which are also responsive to the impulse noise accompanying the video signal. The protection means are coupled to the source of voltage pulses to control the amplitude of the voltage pulses applied to the gain control means in response to the impulse noise and thereby substantially preventing the gain control means from undesirably responding to impulse noise.

In the accompanying drawing:

FIGURE 1 is a schematic circuit diagram partially in block form of a portion of a television receiver embodying the AGC circuit incorporating the principles of the present invention; and

FIGURES 2a and 2b are potential wave-

form diagrams useful in illustrating the operation of the present invention.

Referring now to the drawing, the dashed rectangle 10 schematically represents a monolithic semiconductor integrated circuit chip. The chip has a plurality of contact areas or terminals about its periphery through which external connections to the various circuits on the chip can be made. In this regard and compatible with present day technology and design philosophy, there may be included on the chip 10 a video signal processing channel which includes a first intermediate frequency amplifier 12, second and third intermediate frequency amplifiers 14 and 16, a video detector 18, first video amplifier 20 and a sound channel 22 which may include an intercarrier sound detector and intermediate frequency amplifier.

In a television receiver employing the chip 10, a modulated carrier wave television signal is intercepted by an antenna 24 and coupled to a tuner 26. The tuner 26 may include, as is known, a radio frequency (RF) amplifier and a frequency converter for converting the received radio frequency signal to an intermediate frequency signal.

The intermediate frequency signal derived from the tuner 26 is coupled by means of first frequency selective filter network 28 to the first intermediate frequency (IF) amplifier 12 located on the chip 10. Amplified intermediate frequency signals are coupled by means of a second frequency selective filter network 30 external to the chip 10 to second and third directly coupled IF amplifiers 14 and 16. A second output terminal of the second frequency selective filter network 30 is coupled to the sound channel 22, the output of which is a 4.5 MHz carrier wave in accordance with U.S.A. television standards frequency modulated by the accompanying television sound information.

The amplified intermediate frequency output of the third IF amplifier 16 is applied to a video detector stage 18 which is operative to recover the video signal information from the intermediate frequency signal. The signal output of the detector 18 is amplified in a first video amplifier 20 and is then coupled by a pair of emitter follower transistors 21a and 21b to the video output chip terminal 32 to other amplifiers (not shown) and external of the chip 10 for further amplification of the video signal prior to its being applied to the appropriate control electrodes of a cathode ray tube for display. The video amplifier 20 also supplies signals for the sync separator circuits of the receiver (not shown) and located external to the chip 10.

Referring now with particularity to the schematic portion of the drawing, a keyed AGC circuit is shown therein as part of the integrated circuit chip 10. The circuit includes a first transistor 34 having its emitter electrode connected to a point of reference potential or ground and its collector connected via a resistor 36 to the base electrode of a second transistor 38 also having its emitter electrode grounded.

The collector electrode of the second transistor 38 is connected via a terminal 40 on the chip to the junction of external resistors 42 and 44 which are connected between a source of B+ operating potential and ground. A capacitor 46 is shunted across resistor 42 for the purpose of maintaining a derived AGC control voltage as will be hereinafter detailed.

Connection is also made from the junction of resistors 42 and 44 via a third resistor 48 to the first frequency selective filter network 28 for the application of a derived AGC voltage to the input terminal of the first IF amplifier 12 on the chip so as to control the gain thereof. An example of an IF amplifier suitable for fabrication on an integrated circuit and receptive to an AGC voltage is shown and described in our Specification 1272655.

Operating potential for the transistor 34 and base current drive for the second transistor 38 is supplied from a source 50 in the form of recurrent voltage pulses coincident with the synchronizing components of the received video signal. Connection to the source 50 is made via terminal 51 on the chip 10 through an adjustable external source resistor 53. The source 50 includes means for deriving recurrent flyback voltage pulses from an output transformer associated with the receiver horizontal deflection circuit.

The voltage pulses are coupled from the chip terminal 51 through a Zener diode 52 in series with a current limiting resistor 54 to the junction of the resistor 36 and the base electrode of transistor 38. The Zener diode 52 serves to offset the base level of the recurrent voltage pulses slightly above ground and above the level of any a.c. ripple voltage components that may accompany the voltage pulses, in order to prevent false keying of the transistor 34. A small capacitor 56 of the order of 10 picofarads (pf) is connected between the base and collector electrodes of the transistor 34 for reducing its bandwidth response. Connected for forward conduction across the collector-emitter electrodes of the transistor 34 is a diode 58, which may be formed on the chip 10 by a transistor having its collector and base electrodes directly connected together.

A detected video signal having negative going sync tip excursions is coupled from the video amplifier 20 via emitter followers 21a and 21b through a decoupling resistor 60 in series with a current limiting resistor 62 to the base electrode of the transistor 34.

The collector-emitter path of a transistor 23 is connected between the emitter of the output emitter-follower transistor 21b and ground. The transistor 23 effectively constitutes a con-

stant current source for the emitters of transistors 21a and 21b.

When the output of the video amplifier 20 exceeds a predetermined level, the AGC circuit operates to decrease the gain of the IF amplifiers and/or RF amplifiers in the tuner 26 to maintain a substantially constant video output signal level. Conversely, when the video amplifier output signal falls below said predetermined level, the AGC circuit operates to increase the gain of the signal amplifiers within the limits of their maximum capabilities.

The AGC transistors 34 and 38 operate as follows. The quiescent voltage at the base electrode of transistor 34 is held at a positive potential determined by a d.c. voltage coupled from the first video amplifier 20 through transistors 21a and 21b and resistors 60 and 62 to the base electrode of the transistor 34. Thus, in the absence of signal, the transistor 34 is biased to a highly conductive condition so as to exhibit a low collector impedance. The keying pulses from the source 50 are thus clamped to ground by the transistor 34. When the level of the received signal rises above a predetermined threshold, the synchronizing pulse components (sync tips) will extend far enough in the negative direction to cut off the transistor 34 during the occurrence of the recurring voltage pulses from the source 50.

The transistor 34 will thus be seen to operate as a keyed switch providing a relatively low impedance shunt path across the diode 58 during weak signal conditions, and an open circuit or high impedance path with respect to its effect in shunt circuit across the diode 58 during periods when strong signals are received.

Noting that the anode-cathode junction of the diode 58 is fabricated on the chip 10 from the same conductivity materials, has the same geometry and is in the same thermal environment as the base-emitter junctions of the transistors 34 and 38, the conduction threshold potentials of the diode anode-cathode junction and the base-emitter junctions of the transistors 34 and 38 are all substantially equal.

For maximum gain conditions, wherein the sync tip voltage is insufficient to cut off the transistor 34, the recurring voltage pulses from source 50 will be clamped to about 0.2 volts above ground by the collector-to-emitter path of transistor 34. The 0.2 volts d.c. voltage is also developed across the diode 58. The value of the resistor 36 is chosen such that with the transistor 34 biased full-on, the voltage across the diode 58 together with the voltage developed across the resistor 36 coupled to the base-emitter junction of the second transistor 38 will be less than its threshold potential ($\approx$0.6 volts d.c.) and therefore insufficient to turn it on.

For these conditions, the collector voltage of the transistor 38 will stay at its maximum operating potential as determined by the divider network resistors 44 and 42, and the AGC output capacitor 46 will proceed to charge to this level. An increase in the amplitude level of the video signal or the presence of impulse noise will drive the base electrode of the first transistor 34 sufficiently negative to increase the collector-to-emitter impedance thereof. For these conditions, current from the keying voltage source 50 will be shunted through the diode 58 and the voltage developed thereacross will rise to the contact potential of the diode.

With a suitable choice in value for the resistor 36, the voltage developed thereacross together with the voltage drop across the diode (approximately 0.6 volts d.c. for silicon) will be sufficient to bias the transistor 38 into conduction, thereby causing a decrease in its collector output voltage and subsequent decrease in the charge voltage on the AGC output capacitor 46.

Thus, the base current injection to the transistor 38 can be preset to provide a desired amount of collector current flow through the transistor 38 during conduction thereof. The more negative AGC voltage developed across the capacitor 46 is fed via the resistor 48 through the coupling network 28 to appropriate input terminal(s) of the IF amplifier 12 so as to be effective to bring about a gain reduction of the IF amplifier output.

Since the capacitor 46 will normally be charging to the collector operating potential of the transistor 38 both during keyed cutoff thereof and during the time intervals between keying, the ratio of collector current flow through the transistor 38 during conduction and discharging of the capacitor 46 to the capacitor charge current through the resistor 44 is preferably adjusted to be in the order 100:1. This ratio of currents has been found suitable for maintaining the average level of the AGC voltage developed across the capacitor 46 during intervals between keying, proportional to the strength of the detected video signal output from the amplifier 20 as referenced by the amplitude of the sync tip excursions of the video signal during keyed operation of the AGC circuit.

Referring to FIGURE 2a, it will be apparent that if impulse noise 70 accompanying the detected video signal output of the amplifier 20 overshoots the level V_t of the sync tips 72, as illustrated in the waveform diagram of a detected video signal, and this overshoot occurs during a time interval coincident with keying of the AGC transistor 34, an incorrect AGC set-up voltage may be developed across the output capacitor 46. This may cause improper amplification of the received signal which in turn may affect the receiver's sync separator circuits resulting in a possible loss of vertical and/or horizontal synchronization.

The horizontal sync pulse is about 5 microseconds in duration, and the keying pulse is about 15 microseconds in duration. A noise pulse occurring during the keying pulse interval will cause the transistor 38 to conduct more current than is desirable, and hence produce an undesirable change in the AGC output voltage developed across the capacitor 46.

In accordance with the present invention and referring again to FIGURE 1, a circuit suitable for fabrication using integrated circuit techniques and which complements the above-described AGC transistor circuit by providing impulse noise protection against a false AGC setup voltage on the capacitor 46 includes three transistors 74, 76 and 78 in cascade arrangement. Transistors 74 and 76 are connected as emitter followers with the emitter electrode of the transistor 74 being directly connected to the base of the transistor 76 and through a capacitor 80 to ground. Capacitor 80 is of the order of 10 pf and as such is easily fabricated on the integrated circuit chip 10.

The emitter electrode of the transistor 76 is directly connected to the base of the transistors 78 which has its emitter electrode returned to ground through a resistor 82. The collector electrodes of the transistors 74 and 76 are commonly connected via the chip terminal 84 to the source of operating potential B+. Connection from the collector electrode of the transistor 78 is made via the chip terminal 51 to the recurrent voltage pulse source 50. The base electrode of the transistor 74 is returned to ground through a resistor 86. Connection is also made from the base electrode of the transistor 74 to the junction of resistors 60 and 62 via a capacitor 88. Resistor 86 and capacitor 88 form a high pass filter for differentiating noise impulses which may accompany the video signal output of the amplifier 20 to the base input electrode of the transistor 74. Operation of the circuit is as follows.

Noting that impulse noise generally has a greater high frequency content and higher energy level than that of a normal video signal, the high pass filter is designed, using a relatively small capacitor 88 (approximately 10 pf and therefore easily fabricated on an integrated circuit chip), to sense impulse noise such that the leading and trailing edges of the noise pulses will pass through the capacitor 88 and be developed across the resistor 86, thereby to be coupled to the base electrode of the transistor 74. A waveform diagram illustrating the noise pulse output of the highpass filter is shown in FIGURE 2b.

In the absence of impulse noise, the transistor 74 is normally biased off. The relatively large amplitude excursion of the trailing edge of the noise pulses coupled to the base electrode of the transistor 74 turns the transistor on to peak detect the positive going trailing edges of the differentiated noise pulses and develop a voltage across the emitter connected capacitor 80. The load impedance for the transistor 74 is the base-emitter impedance of the transistor 76 in series with the base-emitter impedance of the transistor 78 and resistor 82.

The time constants of the circuit are such that a detected noise impulse, typically about one microsecond in duration is stretched about 5 microseconds. As a result, noise impulses occurring just before the keying pulse in addition to noise impulses occurring during the keying pulses are detected and cause current to flow through the base-emitter path of transistor 78. This lowers the collector impedance of transistor 78, which in turn reduces the amplitude or level of the keying voltage from the source 50 coupled to the AGC transistors 34 and 38.

The extent of conduction of the transistor 78 and therefore the amount by which the level of the keying voltage from the source 50 will be reduced will be dependent on the charge voltage on the capacitor 80 which in turn is dependent on the amplitude and quantity of the peak detected noise pulses.

To see the effect of the preceding circuit on the operation of the AGC circuit, assume the presence of impulse noise in the video signal wherein the noise pulses are of a polarity such that they extend below the level V_t of the video signal sync tip components and occur during the sync tip intervals as shown, for example, in FIGURE 2a. As was heretofore described, the sync tip excursion below the level V_t (due to the addition of the impulse noise) will bias the keyed AGC transistor 34 into cutoff.

For this condition, the fraction or portion of the keying voltage developed across the diode 58 and resistor 36 will be of a magnitude sufficient to bias the transistor 38 into conduction to bring about a predetermined collector current flow through the transistor 38 to discharge the capacitor 46. This in turn would normally result in the development of an AGC voltage across the output capacitor 46 which tends to reduce the gain of IF amplifier 12 more than desired.

However, with the circuit embodying the present invention, the noise impulses present in the video signal will also be applied via the high pass filter to the base input of the peak detector transistor 74. The application of noise pulses to the base of the transistor 74 will reduce the collector impedance of transistor 78, thereby bringing about a reduction in the amplitude level of the keying voltage.

The extent of conduction of the transistor 38 is a function of the magnitude of the bias voltage coupled across its base-emitter junction which in turn is the predetermined fraction of the keying voltage developed across

the resistor 36 and diode 58. It will be seen that this reduced level in the keying voltage due to conduction of the transistor 78 will decrease the magnitude of the voltage developed across the resistor 36 and diode 58 and thereby tend to counteract the increase in the voltage normally developed across the resistor 36 and diode 58 due to cut off of the keyed switching transistor 34.

The adjustable resistor 53 in series with the keying source 50 provides a convenient means for externally adjusting the amplitude level of the keying voltage at the collector electrode of the transistor 78, so that in the presence of impulse noise, the fraction of the reduced keying voltage developed across the diode 58 and resistor 36 will be insufficient to bias the transistor 38 into conduction, thereby preventing discharge of the capacitor 46 due to a false triggering or cut-off biasing of the AGC transistor 34.

From the foregoing, it will be seen than an improved automatic gain control circuit suitable for fabrication on an integrated circuit chip has been provided.

WHAT WE CLAIM IS:—

1. An automatic gain control circuit for a television receiver including means for providing from a received signal a video signal having recurrent synchronizing signal components which may be accompanied by impulse noise, a source of recurrent voltage pulses coincident with said synchronizing pulse components, gain control means responsive to the synchronizing signal components of said video signal, to said recurrent voltage pulses and undesirably to said impulse noise for developing an automatic gain control voltage, and protection means responsive to impulse noise accompanying said video signal and coupled to said source of voltage pulses to control the amplitude of said voltage pulses applied to said gain control means in response to said impulse noise and thereby substantially prevent said gain control means from undesirably responding to impulse noise.

2. An automatic gain control circuit as claimed in claim 1 in which said gain control means includes an amplifying device having an input and an output circuit, said recurrent voltage pulses being applied to said input circuit, said automatic gain control voltage being developed at said output circuit and varying as a function of the average conductivity of said device during the intervals corresponding with the occurrences of said voltage pulses and in which said protection means includes switch means connected to said input circuit.

3. An automatic gain control circuit as claimed in claim 2 in which said amplifying device includes first and second transistors each having base, emitter and collector electrodes; means connecting the collector-to-emitter path of said first transistor between the base and emitter electrodes of said second transistor, said recurrent synchronizing pulse components extending in a first polarity direction, and being coupled between the base and emitter electrodes of said first transistor, said source of recurrent voltage pulses extending in a polarity direction opposite to that of said first polarity direction and being coupled between the base and emitter electrodes of said second transistor, said gain control voltage being developed between the collector and emitter electrodes of said second transistor.

4. An automatic gain control circuit as claimed in claim 3 comprising biasing means for biasing said first transistor to exhibit a low collector impedance in the absence of video signals, and wherein said synchronizing pulse components extend in a polarity direction to reduce the conduction in said first transistor, and wherein said second transistor is biased to cut-off in the absence of video signals and said recurrent voltage pulses extend in a polarity direction to drive said second transistor into conduction.

5. An automatic gain control circuit as claimed in claim 4 comprising a rectifier connected between the collector and emitter electrodes of said first transistor and poled to conduct current when the base-to-emitter path of said second transistor conducts current.

6. An automatic gain control circuit as claimed in claim 5 comprising a first resistor connected between said source of recurrent voltage pulses and the base electrode of said second transistor, and a second resistor connected between the base electrode of said second transistor and said rectifier.

7. An automatic gain control circuit as claimed in any of claims 3—6 in which said protection means includes a differentiating circuit means coupled to said means for providing video signals, and amplitude detector means having an input coupled to said differentiating circuit means and an output so coupled to said gain control means, that said gain control means is subject to control of the amplitude of said voltage pulses applied thereto in response to control signals provided at said output of said amplitude detector means.

8. An automatic gain control circuit as claimed in claim 7 in which said second transistor exhibits a relatively high collector impedance in the presence of noise impulses, and thus exhibits reduced gain control effectively.

9. An automatic gain control circuit as claimed in claim 4 comprising a third transistor having base, emitter and collector electrodes, said biasing means including a source of biasing voltage for coupling said source of video signals between the base and emitter electrodes of said first transistor, said biasing voltage being poled to forward bias the base-emitter junction of said first transistor, said

the resistor 36 and diode 58. It will be seen that this reduced level in the keying voltage due to conduction of the transistor 78 will decrease the magnitude of the voltage developed across the resistor 36 and diode 58 and thereby tend to counteract the increase in the voltage normally developed across the resistor 36 and diode 58 due to cut off of the keyed switching transistor 34.

The adjustable resistor 53 in series with the keying source 50 provides a convenient means for externally adjusting the amplitude level of the keying voltage at the collector electrode of the transistor 78, so that in the presence of impulse noise, the fraction of the reduced keying voltage developed across the diode 58 and resistor 36 will be insufficient to bias the transistor 38 into conduction, thereby preventing discharge of the capacitor 46 due to a false triggering or cut-off biasing of the AGC transistor 34.

From the foregoing, it will be seen than an improved automatic gain control circuit suitable for fabrication on an integrated circuit chip has been provided.

WHAT WE CLAIM IS:—

1. An automatic gain control circuit for a television receiver including means for providing from a received signal a video signal having recurrent synchronizing signal components which may be accompanied by impulse noise, a source of recurrent voltage pulses coincident with said synchronizing pulse components, gain control means responsive to the synchronizing signal components of said video signal, to said recurrent voltage pulses and undesirably to said impulse noise for developing an automatic gain control voltage, and protection means responsive to impulse noise accompanying said video signal and coupled to said source of voltage pulses to control the amplitude of said voltage pulses applied to said gain control means in response to said impulse noise and thereby substantially prevent said gain control means from undesirably responding to impulse noise.

2. An automatic gain control circuit as claimed in claim 1 in which said gain control means includes an amplifying device having an input and an output circuit, said recurrent voltage pulses being applied to said input circuit, said automatic gain control voltage being developed at said output circuit and varying as a function of the average conductivity of said device during the intervals corresponding with the occurrences of said voltage pulses and in which said protection means includes switch means connected to said input circuit.

3. An automatic gain control circuit as claimed in claim 2 in which said amplifying device includes first and second transistors each having base, emitter and collector electrodes; means connecting the collector-to-emitter path of said first transistor between the base and emitter electrodes of said second transistor, said recurrent synchronizing pulse components extending in a first polarity direction, and being coupled between the base and emitter electrodes of said first transistor, said source of recurrent voltage pulses extending in a polarity direction opposite to that of said first polarity direction and being coupled between the base and emitter electrodes of said second transistor, said gain control voltage being developed between the collector and emitter electrodes of said second transistor.

4. An automatic gain control circuit as claimed in claim 3 comprising biasing means for biasing said first transistor to exhibit a low collector impedance in the absence of video signals, and wherein said synchronizing pulse components extend in a polarity direction to reduce the conduction in said first transistor, and wherein said second transistor is biased to cut-off in the absence of video signals and said recurrent voltage pulses extend in a polarity direction to drive said second transistor into conduction.

5. An automatic gain control circuit as claimed in claim 4 comprising a rectifier connected between the collector and emitter electrodes of said first transistor and poled to conduct current when the base-to-emitter path of said second transistor conducts current.

6. An automatic gain control circuit as claimed in claim 5 comprising a first resistor connected between said source of recurrent voltage pulses and the base electrode of said second transistor, and a second resistor connected between the base electrode of said second transistor and said rectifier.

7. An automatic gain control circuit as claimed in any of claims 3—6 in which said protection means includes a differentiating circuit means coupled to said means for providing video signals, and amplitude detector means having an input coupled to said differentiating circuit means and an output so coupled to said gain control means, that said gain control means is subject to control of the amplitude of said voltage pulses applied thereto in response to control signals provided at said output of said amplitude detector means.

8. An automatic gain control circuit as claimed in claim 7 in which said second transistor exhibits a relatively high collector impedance in the presence of noise impulses, and thus exhibits reduced gain control effectively.

9. An automatic gain control circuit as claimed in claim 4 comprising a third transistor having base, emitter and collector electrodes, said biasing means including a source of biasing voltage for coupling said source of video signals between the base and emitter electrodes of said first transistor, said biasing voltage being poled to forward bias the base-emitter junction of said first transistor, said

synchronizing signal components extending in a polarity direction to overcome said forward bias, means connecting the collector-to-emitter path of said third transistor substantially across the base and emitter electrodes of said second transistor, said third transistor normally exhibiting a high collector impedance, said protection means including peak detector means coupled to said video signal source and responsive to impulse noise which may undesirably accompany said video signals, and means for coupling said peak detector means between the base and emitter electrodes of said third transistor to forward bias the base-to-emitter junction of said third transistor in the presence of impulse noise.

10. An automatic gain control circuit as claimed in claim 9 in which said peak detector includes a fourth transistor having base, emitter and collector electrodes, a first capacitor and a resistor connected in series across said source of video signals, means connecting the base electrode of said fourth transistor to one terminal of said resistor, a second capacitor connected between the emitter electrode of said fourth transistor and the other terminal of said resistor, said first and second capacitors and said resistor having parameters to be responsive to a rate of change of voltage corresponding to that associated with impulse noise.

11. An automatic gain control circuit as claimed in claim 10 in which said second transistor is biased to cut-off in the absence of video signals and said recurrent voltage pulses extend in a polarity direction to drive said second transistor into conduction.

12. An automatic gain control circuit as claimed in claim 11 in which a rectifier is connected between the collector and emitter electrodes of said first transistor and poled to conduct current when the base-to-emitter path of said second transistor conducts current.

13. An automatic gain control circuit as claimed in claim 12 in which a second resistor is connected between the base electrode of said second transistor and the collector electrode of said first transistor.

14. An automatic gain control circuit as claimed in claim 13 in which a diode is connected between said source of recurrent voltage pulses and the base electrode of said second transistor and poled for current conduction in its reverse voltage breakdown mode.

15. An automatic gain control circuit substantially as described in conjunction with the accompanying drawings.

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