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PROCESS FOR ACHIEVING CONTROLLED PRECIPITATION PROFILES IN SILICON WAFERS

The present invention generally relates to the processes for the fabrication of semiconductor material substrates, especially the so-called silicon "slices" or wafers, for the manufacture of electronic components. More particularly, the present invention relates to a process for the treatement of silicon wafers under conditions suitable for the control of the concentration and of the distribution profile of the "gettering" or internal trapping sites.

As is known, single crystal silicon, which is the starting material for most processes for the fabrication of semiconductor electronic components, is commonly prepared with the so-called Czochralski process wherein a single seed crystal is immersed into molten silicon and then grown by slow extraction. As molten silicon is contained in a quartz crucible, it is contaminated with various impurities, among which mainly oxygen. At the temperature of the silicon molten mass, oxygen comes into the crystal lattice until it reaches a concentration determined by the solubility of oxygen in silicon at the temperature of the molten mass and by the actual segregation coefficient of oxygen in solidified silicon. Such concentrations are greater than the solubility of oxygen in solid silicon at the temperatures typical for the processes for the fabrication of integrated circuits. Therefore, as the crystal grows from the molten mass and cools, the solubility of oxygen in it decreases rapidly, whereby in the resulting slices or wafers, oxygen is present in supersaturated concentrations. As it is in supersaturated concentrations, the subsequent thermal treatement cycles of the wafers cause the precipitation

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of oxygen.

The precipitation of oxygen can cause useful effects and harmful effects. The useful effects are connected with the capability of oxygen precipitates (and of the "defects" connected thereto) to trap the undesired metal impurities that could subsequently come into contact with the wafer during the subsequent manufacture for the fabrication of the electronic component and compromise the performance of the latter. The harmful effects derive from the fact that such precipitates themselves will be contamination agents if they are situated in the active region of the wafer, where, on the contrary, a very high purity for the fabrication e.g. of an integrated circuit is necessary.

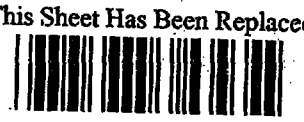
During years, various schemes have been suggested for carrying out the treatement of silicon wafers in such a manner that the active region, that occupies a depth of a few microns from the surface of the wafer, is comparatively devoid of the aforementioned "defects", whereas the remaining thickness of the wafer has a density of such defects sufficiently high for an effective trapping of the undesired metal impurities.

Such techniques are known as trapping or "intrinsic" gettering techniques and the region devoid of defects close to the surface of the wafer is named the denuded zone.

The object of the present invention is to indicate a process for controlling the concentration of the trapping centres present in silicon wafers and, more particularly, for realizing the defect density profile necessary to achieve a good denuded zone and a good intrinsic trapping effect.

In more precise terms, a first aspect of the invention relates to the control of the level of precipitation of oxygen in silicon wafers. A second aspect relates to the control of the density profiled of

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oxygen precipitates, in such a manner that the peak of the profile can act as a trapping region distinct and far from the active region of the device. A third aspect relates, therefore, to the fabrication of controlled precipitation wafers having an effective denuded zone in correspondence with the active region of the device and a highly effective trapping zone in the remaining volume.

These objects are achieved according to the present invention by means of a process for the treatement of silicon slices or wafers intended to the fabrication of integrated circuit electronic components which comprises the following fundamental operations: (a) subjecting the wafers to a preliminary thermal treatement, at a temperature between 950 °C and 1150 °C, in particular at about 1100 °C, for a duration of about 15 minutes; (b) after a standard chemical corrosion (etching) treatement, subjecting pairs of wafers coupled in a close reciprocal thermal contact to a fast thermal annealing treatement, at a temperature between 1200 °C and 1275 °C for a duration of some tens of seconds; (c) subjecting the wafers to a further extended thermal treatement at a temperature between 900 °C and 1000 °C, and, finally, (d) extracting the wafers from the furnace and subjecting the surfaces that were in close reciprocal contact during the fast annealing treatement to a surface polishing. For the coupling of the two slices it suffices to realize a mechanical-thermal contact between the two surfaces: other methodologies for coupling more intimately that realize atomic bonds between the two surfaces (wafer-bonding) aren't necessary, but can be used.

As will be better explained in the following, the treatement according to the invention initially produces high temperature nucleation centres, named the "precursors" during the thermal fast annealing operation

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and these precursors subsequently give rise to the classic "defects".

Although prior publications exist that report the generation of these precursors, considerable differences exist with respect to the work performed in the frame of the present invention. First of all, the generation time scales have shown themselves to be very faster than those precedently recognized. Secondly, a lower bound has been recognized only of about 1200 °C for the high temperature treatement. Thirdly, no need has been found for a treatement at a comparatively low temperature and, about 650 °C, to obtain the formation of a convenient defect density profile.

Finally, by virtue of the coupling of two wafers during the high temperature fast annealing treatement, in each wafer a completely unsymmetrical profile has been realized which sees a very high defect density by the one side and a very low defect density by the other side, achieved only by exploiting the observation that the modality of the cooling of the wafer plays an important rôle in the formation of the density profile.

Further particularities and advantages of the present invention will turn out to be evident from the continuation of the disclosure with reference to the annexed drawings given only as a matter of explanation and not of limitation, and wherein:

Figure 1 shows a profile of the density of the precipitates as a function of the depth for a single silicon wafer heated to a temperature close to 1200 °C for two short, but distinct time intervals, of 20 and 35 seconds, respectively;

Figures 2a and 2b comparisonwise show the case of the treatement of a single wafer and the case of the treatement of a pair of coupled wafers according to the present invention;

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Figure 3 shows the profile of the density of the precipitates as a function of the depth for one of the two wafers sobjected in a coupled form to the treatement according to the present invention.

Before passing to a detailed description of the single stages of the process, it is desired to precisely state that the present invention has started from the observation that subjecting the silicon wafers to a thermal rapid annealing treatement at a high temperature, in particular between 1200 °C and 1300 °C, for short time intervals, a considerable improvement of oxygen precipitation is achieved. In particular, it has been observed that such an intensification depends on temperature and does not present itself homogeneous at the interior of the wafer. Under the latter aspect, the formation has been observed of two concentration peaks, in proximity to the two major surfaces of the wafers, with a minimum plateau in the central zone.

This is clearly put into evidence in Figure 1, wherein the two peaks in proximity to the two major surfaces of the wafer and the central plateau are easily recognized. The diversity of the profile in correspondence to two different treatement durations (20 s and 35 s) is also recognized.

Under the physical aspect, it has been ascertained that this thermal rapid annealing treatement at a high temperature involves the formation of the so-called defects which act as precursors for the subsequent nucleation and growing of the precipitates of oxygen.

A further observation at the basis of the present invention is that a thermal treatement at temperatures of 900 to 1000 °C of the wafers already subjected to a rapid thermal annealing does not favour a further necleation, and on the contrary it involves a dissolution of a certain fraction of the aforementioned

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precursors generated at a high temperature. Indeed, it has been proved that such precursors present a certain instability when they are cooled at temperatures lower than those whereat they have been generated. As a compensation, this treatement at 900 to 1000 °C involves a growing of eventual already existing precipitation nuclei and a general stabilization of the defects created by the rapid thermal annealing treatement.

Finally, at the basis of the present invention there is the discovery that the instability of the precursors generated at a high temperature can be put into so a close relationship with the cooling conditions, that it is hypothesized that a temperature gradient at the interior of the wafer during the cooling can involve a disuniformity of the dissolution of the defects at a high temperature. This hypothesis that, in the first place, could explain the difference of the peak values of the density in correspondence with the two different surfaces making it to derive from the different emissivity values of said two surfaces, one of which is polished and the other is rough, has been corroborated by experimental works that have demonstrated that the peak corresponding to a surface is substantially eliminated when the thermal emissivity through such a surface is greatly reduced and therefore the cooling of the wafer is greatly slowed down for instance by means of a thermal shielding of the surface itself.

With this very important consideration one of the fundamental characetristics is connected of the present invention, which consists in the fact that the wafers are not subjected to the treatement singularly, but physically coupled or paired into a close contact thereby to achieve their reciprocal thermal shielding. In this way, what is the double peak distribution profile of the defects indicated by the arrow of Figure

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2a, in which a single wafer is exposed, remains always a double peak profile as shown with the arrow II in Figure 2b, but such a profile interests this time two paired wafers which, once separated, will have a defect density profile that presents a peak in proximity to a surface and a plateau near zero in proximity to the other surface . It is just the result that one desires to achieve, without having to resort to long and laborious complex thermal treatements for creating a good denuded zone suitable for the subsequent realization of integrated circuits.

In figure 3 the density profiles of the oxygen precipitates are reported more precisely as a function of depth, for a wafer treated under a form paired with another wafer, in the case of two temperatures of 1200 °C and of 1250 °C.

Synthetizing the observations set forth above, the process according to the present invention fundamentally comprises the following treatement operations.

In a second operation the wafers, after having undergone a standard chemical corrosion (etching) treatement, are subjected two by two in a close reciprocal contact to a rapid thermal annealing treatement in which they receive a thermal pulse of the duration of some tens of seconds, at a temperature comprised within the approximative interval between 1200 °C and 1275 °C. As the density of defects that are generated depends on both time and temperature, as already put into evidence in Figures 1 and 3, these parameters depend on the density of the defects that one desires to achieve.

To this operation a further thermal treatement follows at a temperature between 950 °C and 1150 °C, eventually subdivided into two stages (for instance a first stage at 900 °C and a second stage at 1000 °C, for

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time intervals of 4 hours and of 16 hours respectively). the aim of this operation is to stabilize and to grow the precipitation precursors that have been generated in the preceding operation, eliminating at the same time their unstable fraction.

In the subsequent operation the wafers are removed from the furnace and the surfaces that were in a close reciprocal contact during the high temperature thermal rapid annealing treatement are polished in a standard way. In this way, the peak-plateau profile created in the two preceding operations ensures that there is a very low defect density (plateau) in proximity to the polished surface, so realizing a denuded zone perfectly suitable for the fabrication of integrated circuits, and a ghigh and well controlled defect density in proximity to the rear surface of the wafer, far from the active region, perfectly suitable for the desired function of trapping the contamination agents.

Within the frame of the present invention it has been, moreover, ascertained that the form of the precipitation profile is at least affected, if not determined, by the presence of a gaseous atmosphere on the slices, in particular nitrogen.

Therefore, the profile asymmetry that is obtained shielding a face of silicon is also due to the fact that the slice is shielded against the nitrogen atmosphere.

It is, moreover, deisred to precisely state that it is not necessary that the shielding is realized by means of the coupling of slices as the same effect can be obtained with another shielding member, e.g. a quartz plate.

It is even foreseen that the asymmetry of the profile is at least favoured, if not promoted, by a double gaseous atmosphere, of argon on a face and of

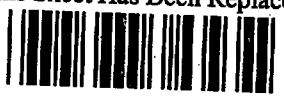
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nitrogen on the other face of the slice.

In the above the preferred embodiment has been disclosedof the present invention, but it is to be expressedly understood that variations and modifications can be made to it, without so departing from the scope of the present invention.

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CLAIMS:

1. A process for the treatement of silicon wafers to achieve therein controlled profiles of the density of precipitations, characterized in that it comprises the following operations:

(a) subjecting the wafers to a preliminary thermal treatement, at a temperature between 950 °C and 1150 °C, in particular at about 1100 °C, for a duration of about 15 minutes;

(b) after a standard chemical corrosion (etching) treatement, subjecting pairs of wafers paired into a close thermal reciprocal contact to a rapid thermal annealing treatement, at a temperature between 1200 °C and 1275 °C for a duration of some tens of seconds;

(c) subjecting the wafers to a further extended thermal treatement at a temperature between 900 °C and 1000 °C, and, finally,

(d) extracting the wafers from the furnace and subjecting the surfaces that were in a close reciprocal contact during the rapid annealing treatement to a surface polishing.

2. The process for the treatement of silicon wafers according to Claim 1, wherein said preliminary thermal treatement is carried out at about 1100 °C, and performs the function of further reducing the "defect" density and establish homogeneous starting conditions.

3. The process for the treatement of silicon wafers according to Claim 1, wherein said rapid thermal annealing treatement consists in subjecting the pairs of coupled wafers to a thermal pulse of a duration of 10 to 40 seconds for the generation of precipitation precursors.

4. The process for the treatement of silicon wafers according to Claim 1, wherein said further

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extended thermal treatement is carried out in one or two stages.

5. The process for the treatement of silicon wafers according to Claim 4, wherein said further extended thermal treatement is carried out in two stages, in particular a first stage at a temperature of 900 °C and a second stage at a temperature of 1000 °C for durations of 4 hours and of 16 hours respectively.

6. The process for the treatement of silicon wafers according to Claim 1, wherein said close thermal contact coupling of the wafers is realized with the simple mechanical-thermal contact between their surfaces.

7. The process for the treatement of silicon wafers according to Claim 1, wherein said close thermal contact coupling of the wafers is realized with intimate coupling methodologies that realize atomic bonds between their surfaces (wafer-bonding).

8. A process for the treatement of silicon wafers to achieve therein controlled profiles of the densities of precipitations, characterized in that it comprises the following operations:

(a) subjecting the wafers to a preliminary thermal treatement, at a temperature between 950 °C and 1150 °C, for a duration of about 15 minutes;

(b) after a standard chemical corrosion treatement, subjecting the wafers in an inert gaseous atmosphere, with a shielded face, to a rapid thermal annealing treatement, at a temperature between 1200 °C and 1275 °C for a duration of some tens of seconds;

(c) subjecting the wafers to a further extended thermal treatement at a temperature between 900 °C and 1000 °C and, finally,

(d) extracting the wafers from the furnace and subjecting the shielded surfaces during the rapid annealing treatement to a surface polishing.

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9. The process according to Claim 8, characterized in that said inert atmosphere is nitrogen.

10. The process according to Claims 8 and 9, characterized in that said shielding is realized with another silicon slice.

11. The process according to Claims 8 and 9, characterized in that said shielding is realized with a quartz plate.

12. The process according to Claims 8 and 9, characterized in that said shielding of one face of the wafer against the nitrogen atmosphere is realized by applying an argon atmosphere upon such a face.

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