ABSTRACT

AN ADVANCED LOW-LEAKAGE ARCHITECTURE FOR SUB-0.18um SALICIDED CMOS DEVICE

A method for forming a stepped shallow trench isolation is described. A pad oxide layer is deposited on the surface of a semiconductor substrate. A first nitride layer is deposited overlying the pad oxide layer. The first nitride layer is etched through where it is not covered by a mask to provide an opening to the pad oxide layer. A first trench is etched through the pad oxide layer within the opening and into the semiconductor substrate. A second nitride layer is deposited overlying the first nitride layer and filling the first trench. Simultaneously, the second nitride layer is anisotropically etched to form nitride spacers on the sidewalls of the first trench and the semiconductor substrate is etched into where it is not covered by the spacers to form a second trench. Ions are implanted into the semiconductor substrate underlying the second trench. The first and second trenches are filled with an oxide layer. Thereafter, the first nitride and pad oxide layers are removed completing the formation of shallow trench isolation in the fabrication of an integrated circuit device. This nitride spacer STI architecture prevents STI corner oxide recess and enables borderless contact formation. This unique process reduces junction leakage and also reduces contact leakage.

(FIGURE 5 IS SUGGESTED FOR PUBLICATION)