

ABSTRACT

A nonvolatile memory device includes a memory cell region and a peripheral circuit region. The memory cell region includes a plurality of memory cell arrays disposed in a first direction. Each of the plurality of memory cell arrays includes a plurality of sub-planes disposed in the first direction and extending in a second direction intersecting the first direction. The peripheral circuit region is disposed below the memory cell region in a vertical direction and includes a plurality of page buffer circuits respectively coupled with the plurality of memory cell arrays. Each of the plurality of memory cell arrays further includes a first common source plate extending in the first direction and commonly coupled with the plurality of sub-planes, and first and second bit line groups respectively coupled with first and second sub-planes of the plurality of sub-planes.

FIG. 5