METHODS FOR FABRICATING AN ELECTRICALLY CORRECT INTEGRATED CIRCUIT

ABSTRACT

A method for fabricating an integrated circuit is disclosed that includes, in accordance with an embodiment, providing a logical design for the semiconductor device and comparing an element in the logical design to a library of element patterns. The library of element patterns is derived by identifying layout patterns having electrical properties that deviate from modeled properties; the library also includes a quantitative measure of deviation from the modeled properties. In response to the comparing and with consideration of the quantitative measure, a determination is made as to whether the element is acceptable in the logical design. A mask set is generated that implements the logical design using either the element or a modified element if the element is not acceptable, and the mask set is employed to implement the logical design in and on a semiconductor substrate.

Fig. 3