

RECORDING/REPRODUCING APPARATUS AND RECORDING MEDIUM ROTATION
CONTROL METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an apparatus for recording/reproducing and a method for controlling rotation of a recording medium, and more particularly relates to an apparatus for recording/reproducing a method for controlling rotation of a recording medium which are capable of reducing polarity fluctuation of error signals due to noise and performing accurately rotation control.

Description of Related Art

Heretofore, as the method for controlling rotation of a disc, two methods, which include a method that a rotation control signal is generated using a synchronizing signal of a signal recorded in a disc as data, and another method that a rotation control signal is generated using a reproducing signal from an address information recorded by wobbling of a track on a disc with a certain period, have been known.

In these rotation control methods, speed term data and phase term data at the irradiated position are generated based on the light reflected from a disc, and these data are

synthesized to obtain an error voltage used for rotation control.

Polarity of the error voltage for indicating the rotation direction (acceleration or deceleration) of a disc and magnitude of the error voltage (absolute value) are obtained, and the signals of polarity and absolute value are synthesized and supplied to a certain spindle motor.

Fig. 9 shows an exemplary structure of a conventional polarity judgment circuit for judging polarity of an error voltage. In detail, an error voltage and a predetermined reference voltage are supplied to a comparator 1, and these two voltages are compared. a signal which indicates positive polarity (acceleration) is outputted if the error voltage is higher than the reference voltage, and a signal which indicates negative polarity (deceleration) is outputted if the error voltage is lower than the reference voltage.

Fig. 10 shows an error voltage for rotation control generated from a record signal on a disc. An error voltage is composed of a rotation variation voltage component which varies periodically every rotation, a certain constant loss voltage, and noise voltage having small amplitude.

On the other hand, Fig. 11 shows an error voltage generated from a wobble signal. Also in this case, though the

error voltage is composed of rotation variation voltage, loss voltage, and noise components, fluctuation due to noise is more significant in comparison with the error voltage generated from a record signal shown in Fig. 10.

As it is apparent from Fig. 10 and Fig. 11, an error voltage includes always positive polarity (polarity of the direction which accelerates rotation). In detail, assuming that the reference voltage in Fig. 9 is 0, then the output from the comparator 1 shows always positive polarity corresponding to the error voltage input shown in Fig. 10 and Fig. 11.

In order to perform higher speed recording/reproducing processing of data, it is considered that rotation speed of a disc is increased to increase transfer speed of data.

Fig. 12A shows an error voltage generated from a record signal on a disc in the case that rotation speed is increased more faster than the case shown in Fig. 10. Fig. 12B shows polarity of the error voltage in such case. As shown in Fig. 12B, the increased rotation speed results in negative polarity, namely, generation of a voltage for deceleration.

Fig. 13A shows an error voltage generated from a wobble signal in the case of increased rotation speed. Fig. 13B shows polarity of the error voltage in such case. Inversion between positive polarity and negative polarity occurs more often in

the case of Fig. 13B than in the case of Fig. 12B. The often inversion is attributed to error voltage fluctuation due to noise more significant in the case of Fig. 13 than in the case of Fig. 12.

Therefore, in the case that transfer speed is intended to be increased by rotating a disc faster, often inversion of polarity which arises along with judgment of polarity of the error voltage generated from a wobble signal results in loud deceleration noise and increased power consumption when decelerating, such noise and power consumption are problems.

SUMMARY OF THE INVENTION

The present invention was accomplished in view of such problems, it is the object of the present invention to provide a method for judging correctly the polarity of an error voltage in view of fluctuation elimination of an error voltage due to noise.

The recording/reproducing apparatus described in claim 1 is provided with a judgment means for judging polarity of an error voltage after fluctuation due to noise included in the error voltage is removed.

The recording/reproducing method described in claim 6 comprises a step for judging polarity of an error voltage after

fluctuation due to noise included in the error voltage is removed.

In the recording/reproducing apparatus described in claim 1, the judgment means removes fluctuation due to noise included in an error voltage and then judges polarity of the error voltage.

In the recording medium rotation control method described in claim 8, fluctuation due to noise included in an error voltage is removed, and then polarity of the error voltage is judged.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram for illustrating an exemplary structure of rotation control mechanism of a recording/reproducing apparatus of the present invention.

Fig. 2 is a block diagram for illustrating an exemplary structure of the polarity judgment circuit 22 in Fig. 1.

Fig. 3 is a circuit diagram for illustrating an exemplary structure of the LPF 31 in Fig. 2.

Figs. 4A to 4D are a set of timing charts for describing processing operation of the polarity judgment circuit 22 in Fig. 2.

Fig. 5 is a block diagram for illustrating another

exemplary structure of rotation control mechanism of a recording/reproducing apparatus of the present invention.

Fig. 6 is a block diagram for illustrating an exemplary structure of the polarity judgment circuit 72 in Fig. 5.

Fig. 7 is a block diagram for illustrating an exemplary structure of the logic circuit 52 in Fig. 6.

Figs. 8A to 8E are a set of timing charts for describing processing operation of the logic circuit 52 in Fig. 7.

Fig. 9 is a block diagram for illustrating an exemplary structure of a conventional polarity judgment circuit.

Fig. 10 is a diagram for illustrating an error voltage generated from a record signal on a disc.

Fig. 11 is a diagram for illustrating an error voltage generated from a wobbling signal.

Figs. 12A to 12B are a set of diagrams for illustrating an error voltage generated from a record signal on a disc during high speed rotation.

Figs. 13A to 13B is a set of diagrams for illustrating an error voltage generated from a wobbling signal during high speed rotation.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Before embodiments of the present invention are

described, in order to describe clearly the correspondence relation between the respective means described in claims and embodiments described hereinafter, the feature of the present invention is described with addition of corresponding embodiment (one example) in parentheses subsequent to each means. Needless to say, such description does not limit the means to the embodiment in the parentheses.

The recording/reproducing apparatus described in claim 1 which controls rotation of a recording medium using a rotation control information recorded in a recording medium when the information is recorded in or reproduced from the recording medium, is provided with a generation means (for example, synthesis circuit 21 in Fig. 1) for generating an error voltage for rotating the recording medium from the rotation control information, a judgment means for judging polarity of the error voltage after removal of fluctuation due to noise included in the error voltage, a detection means (for example, absolute value circuit 23 in Fig. 23) for detecting magnitude of the error voltage, and a rotation means (for example, spindle motor 11 in Fig. 1) for rotating the recording medium dependently on the judged polarity of the error voltage and the detected magnitude of the error voltage.

Fig. 1 is a block diagram for illustrating an exemplary

structure of the rotation control mechanism of a recording/reproducing apparatus of the present invention.

An optical pick-up converts the reflected light from a disc D to a certain electric signal (reproducing signal). A reproducing signal of a wobbling signal corresponding to the track address outputted from the optical pick-up 12 is supplied to PLL 14 through a driver 13.

PLL 14 generates a synchronizing signal which locks the phase of a reproducing signal, and supplies it to a synchronizing detection circuit 16. A clock generation circuit 15 of PLL 14 generates a clock which synchronizes with the phase of the reproducing signal and outputs it to a length judgment circuit 17.

The synchronizing detection circuit 16 detects a synchronizing signal from the signal supplied from PLL 14 and outputs it to a phase detection circuit 18.

A quartz oscillator circuit 19 generates a clock having a predetermined frequency and outputs it to the length judgment circuit 17 and a 1/m frequency dividing circuit 20. The length judgment circuit 17 compares frequency of the clock supplied from the PLL 14 with that of the clock supplied from the quartz oscillator circuit 19 and calculates the speed term of the irradiated position, and outputs the speed term data to a

synthesis circuit 21. The clock generated from the quartz oscillator circuit 19 is converted to a clock having a frequency of $1/m$ and supplied to the phase detection circuit 18. The synchronizing detection circuit 18 compares phase of the synchronizing signal supplied from the synchronizing circuit 16 with that of the clock supplied from the $1/m$ frequency dividing circuit 20 to detect the phase of the irradiated position, and outputs a phase term data to the synthesis circuit 21.

The synthesis circuit 21 combines the speed term data supplied from the length judgment circuit 17 with the phase term data supplied from the phase detection circuit 18 to generate an error voltage, and supplies it to a polarity judgment circuit 22 and absolute value circuit 23.

The polarity judgment circuit 22 judges whether polarity of the error voltage is the polarity which accelerates rotation speed of the disc (positive polarity) or the opposite polarity which decelerates rotation speed of the disc (negative polarity), and outputs the resultant polarity signal judgment to a driver 24.

The absolute value circuit 23 calculates the absolute value of the error voltage, and outputs the calculation result to the driver 24.

The driver 24 generates a rotation control signal using the polarity judgment result (polarity signal) of the error voltage and the absolute value, and supplies the rotation control signal to the spindle motor 11. The spindle motor 11 rotates the disc D dependently on the rotation control signal.

Fig. 2 is a block diagram for illustrating the exemplary structure of one example of the polarity judgment circuit 22. The error voltage generated in the synthesis circuit 21 is first supplied to a comparator 30 and is compared with the 0-level voltage (reference level), and a binary signal of positive polarity or negative polarity corresponding to the comparison result is supplied to a LPF 31 (low pass filter) of the polarity judgment circuit 22. The LPF 31 removes disturbance component generated due to noise from the signal and then the signal is supplied to a comparator 32.

The comparator 32 compares magnitude of the error voltage supplied from the LPF 31 with that of a predetermined reference voltage, for example, 0-level voltage, and a signal of positive polarity or negative polarity obtained dependently on the comparison result is supplied to the driver 24. In detail, if the error voltage supplied from the LPF 31 is higher than 0, then the comparator 32 supplies a signal of positive polarity to the driver 24, and if the error voltage is lower than 0,

the comparator 32 supplies a signal of negative polarity to the driver 24.

Fig. 3 is a circuit diagram for illustrating the structure of one example of the LPF 31. The error voltage supplied to the polarity judgment circuit 22 is applied to a resistor 41 of the LPF 31. Other end of the resistor 41 is connected to the one input side of the comparator 32 and also connected to the one terminal of a capacitor 42. The other end of the capacitor 42 is grounded. When a high frequency voltage is applied to the LPF 31, the capacitor 42 absorbs the voltage. Therefore, a low frequency component is outputted from the output terminal of the LPF 31.

Processing operation of the polarity judgment circuit 22 is described with reference to a timing chart shown in Fig. 4.

A binary signal (error voltage) shown in Fig. 4B is generated by comparing the input signal (Fig. 4A) with 0-level voltage (reference level) by means of the comparator 30. The binary signal is supplied to the LPF 31 of the polarity judgment circuit 22, the high frequency component of the input signal is removed in the LPF 31, and the signal having a waveform as shown in Fig. 4C is supplied to the comparator 32.

The comparator 32 compares the signal of the reference

level (0-level signal) with the signal supplied from the LPF 31 (Fig. 4(c)), and generates a signal (Fig. 4D) which indicates polarity corresponding to the comparison result, and outputs it.

If the binary signal in Fig. 4A is supplied to the comparator 32 without passing through the LPF 31 (that is the case of a conventional polarity judgment circuit), a signal having the same waveform as the input signal is outputted. Therefore, it is apparent from the comparison of the signal of Fig. 4D (a signal in accordance with the present invention) with the same signal as that of Fig. 4B (a signal outputted from a conventional polarity judgment circuit) that high frequency component due to noise is removed from the former signal and frequency of polarity inversion is reduced, thus the former signal is better in signal quality than the latter signal.

Fig. 5 shows the structure of another embodiment of a rotation control mechanism of a recording/reproducing apparatus in accordance with the present invention. Components in the recording/reproducing apparatus shown in Fig. 5 corresponding to components shown in Fig. 1 are given the same characters as shown in Fig. 1, and the description is omitted for convenience.

A duration determining circuit 71 judges the type of the disc using a signal supplied from the optical pick-up 12, also judges whether the operation is now recording processing or reproducing processing, determines a duration while the same polarity continues corresponding to the judgment result, and supplies the determined result to the polarity judgment circuit 72. In detail, for example, if the recording/reproducing apparatus is in reproducing processing, then the duration determining circuit 71 determines a relatively short duration so that the polarity judgment circuit 72 ignores a polarity change shorter than the determined duration. If the recording/reproducing apparatus is in recording processing, then the duration determining circuit 71 determines a relatively long duration so that the polarity judgment circuit 72 ignores a polarity change shorter than the determined duration. Thereby, high frequency component is ignored during reproduction, and high frequency component is reflected on recording with high fidelity during recording. As the result, noise due to deceleration generated when reproducing is suppressed and information is recorded with high fidelity to input signal when recording.

The polarity judgment circuit 72 controls the clock frequency which a built-in clock generation circuit 63 (Fig.

7) outputs corresponding to the determined result supplied from the duration determining circuit 71.

Fig. 6 is a block diagram for illustrating an exemplary structure of the polarity judgment circuit 72. The error voltage supplied from the synthesis circuit 21 is supplied to the one input terminal (non-inversion input) of a comparator 51 in the polarity judgment circuit 72. A certain predetermined reference voltage is supplied to the other input terminal (inversion input) of the comparator 51.

The comparator 51 compares the error voltage with the reference voltage, generates a signal which indicates polarity corresponding to the comparison result, and outputs it to a logic circuit 52. The logic circuit 52 extracts and outputs only the polarity signal that continued for a predetermined time using the frequency clock corresponding to the determined duration result supplied from the duration determining circuit 71.

Fig. 7 is a block diagram for illustrating an exemplary structure of the logic circuit 52. The clock generation circuit 63 generates a frequency clock corresponding to the determined duration result supplied from the duration determining circuit 71, and supplies it to the clock terminals CK of a D-type flip-flop 61-1 and a D-type flip-flop 61-2.

The input signal supplied from the comparator 51 is inverted in a NOT circuit 64, and thereafter supplied to the D-type flip-flop 61-1 and a NAND circuit 62. The output terminal Q of the D-type flip-flop 61-1 is connected to the input terminal D of the D-type flip-flop 61-2. The output terminal Q of the D-type flip-flop 61-2 is connected to the other input terminal of the NAND circuit 62.

Processing operation of the logic circuit 52 is described with reference to a timing chart shown in Fig. 8.

The input signal (Fig. 8A) supplied from the comparator 51 is supplied to the NOT circuit 64 and inverted (Fig. 8B), and also the clock generation circuit generates a clock having a predetermined frequency (Fig. 8D) corresponding to the result determined by the duration determining circuit 71, and the clock is supplied to the clock terminals CK of the D-type flip-flop 61-1 and the D-type flip-flop 61-2.

The input signal (signal shown in Fig. 8B) inverted by the NOT circuit 64 and the two-clock delayed signal (Fig. 8C) supplied through the D-type flip-flops 61-1 and 61-2 are supplied to an input terminal of the NAND circuit 62. In detail, when both two-clock delayed signal and current signal are in H (high level), an output signal (Fig. 8E) outputted from the NAND circuit 62 is L.

As described herein above, high frequency polarization fluctuation due to noise can be removed. Because the clock frequency generated from the clock generation circuit 63 is controlled dependently on the operation of recording or reproducing, the frequency to be removed can be changed depending on the case.

Alternately, in the case of a disc that the type of the disc is detected and the error voltage is generated from a wobbling signal, the polarity judgment circuit 22 or 72 as described herein above may be used, and in the case of a disc that the error voltage is generated from the recorded data, a conventional polarity judgment circuit as shown in Fig. 9 may be used. In the former case, through the servo band becomes somewhat narrow, thereby a wider servo band can be used.

According to a recording/reproducing apparatus described in claim 1 and a recording medium rotation control method described in claim 8, fluctuation due to noise included in the error voltage is removed and thereafter polarity of the error voltage is judged, thereby the polarity judgment of rotation control is performed adequately.



What Is Claimed Is:

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1. A recording/reproducing apparatus which controls rotation of a recording medium using rotation control information recorded in said recording medium when information is recorded in or reproduced from said recording medium, comprising:

generation means for generating an error voltage for rotating said recording medium from said rotation control information,

judgment means for judging polarity of said error voltage after fluctuation due to noise included in said error voltage is removed,

detection means for detecting magnitude of said error voltage, and

rotation means for rotating said recording medium dependently on the judged polarity of said error voltage and the detected magnitude of said error voltage.

2. The recording/reproducing apparatus as claimed in claim 1, wherein said judgment means removes fluctuation due to said noise of said error voltage using a low pass filter.

3. The recording/reproducing apparatus as claimed in claim 1, wherein said judgment means compares the magnitude of said error voltage and a predetermined reference voltage,



and removes fluctuation component due to said noise based on the difference between the signal with a delay of a predetermined time of the comparison result and the signal without delay of the comparison result.

4. The recording/reproducing apparatus as claimed in claim 1, wherein said judgment means changes fluctuation frequency to be removed depending on whether the operation is recording or reproducing.

5. The recording/reproducing apparatus as claimed in claim 1, wherein said judgment means changes fluctuation frequency to be removed depending on the type of said recording medium.

6. The recording/reproducing apparatus as claimed in claim 1, wherein said rotation means is provided with a spindle motor.

7. The recording/reproducing apparatus as claimed in claim 6, wherein said recording/reproducing apparatus is provided additionally a deceleration means for decelerating rotation of said spindle motor.

8. A recording medium rotation control method for controlling rotation of a recording medium using rotation control information recorded in said recording medium when information is recorded in or reproduced from said recording



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medium, comprising steps of;

generating an error voltage for rotating said recording medium from said rotation control information,

judging polarity of said error voltage after fluctuation due to noise included in said error voltage is removed,

detecting magnitude of said error voltage, and

rotating said recording medium dependently on the judged polarity of said error voltage and the detected magnitude of said error voltage.