FIG. 1A

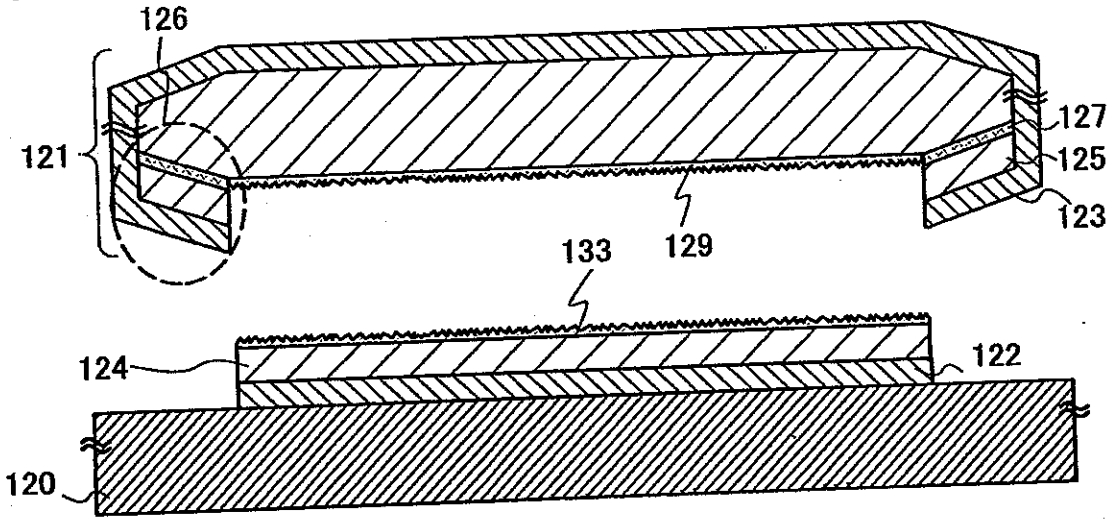


FIG. 1B

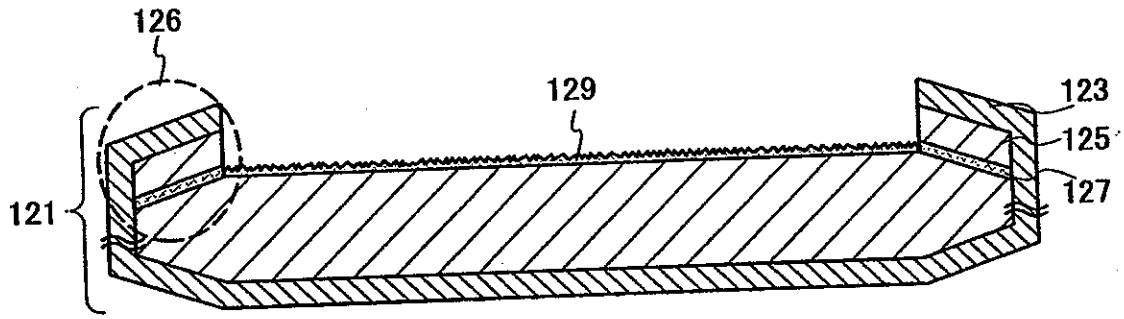


FIG. 1C

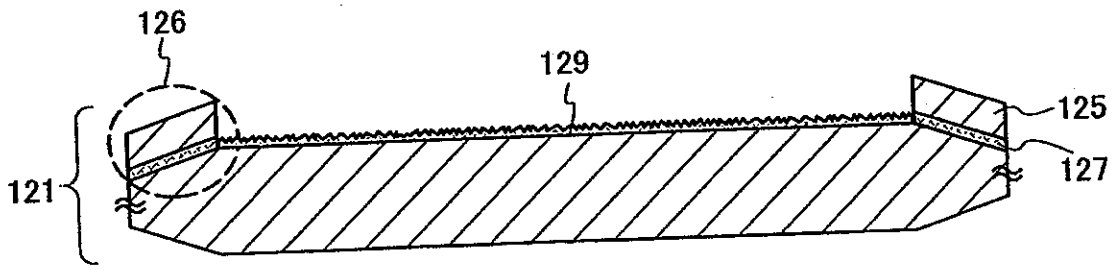


FIG. 1D

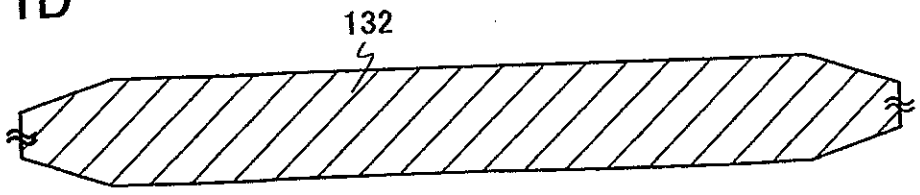


FIG. 2A

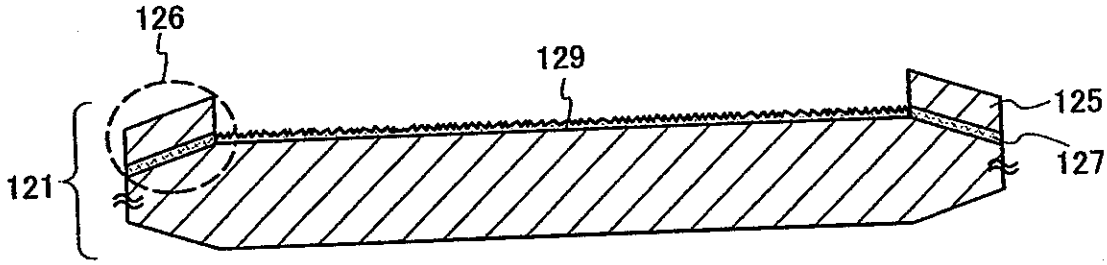


FIG. 2B

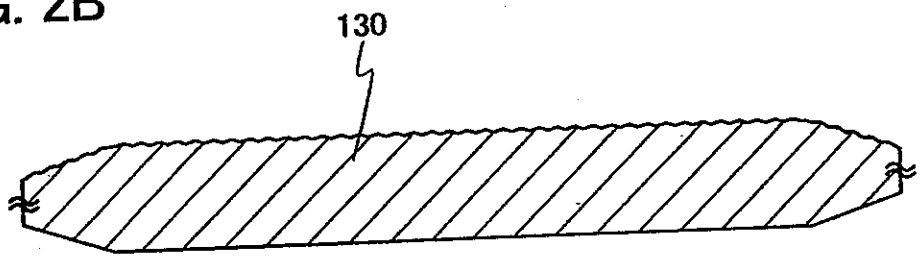


FIG. 2C

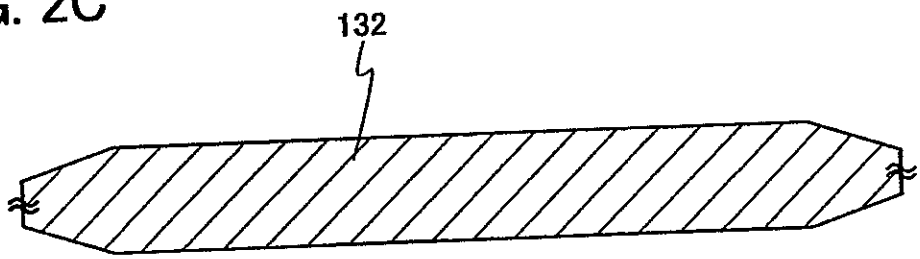


FIG. 3A

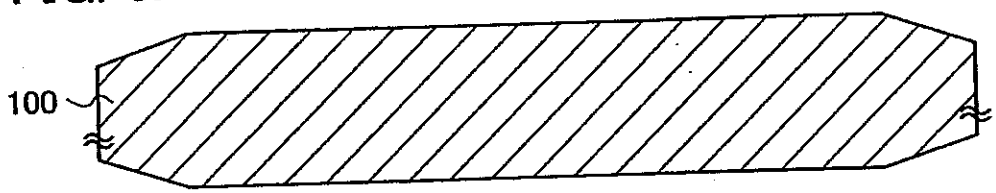


FIG. 3B

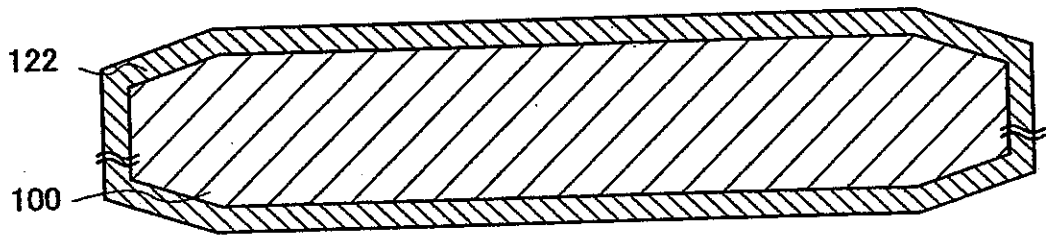


FIG. 3C

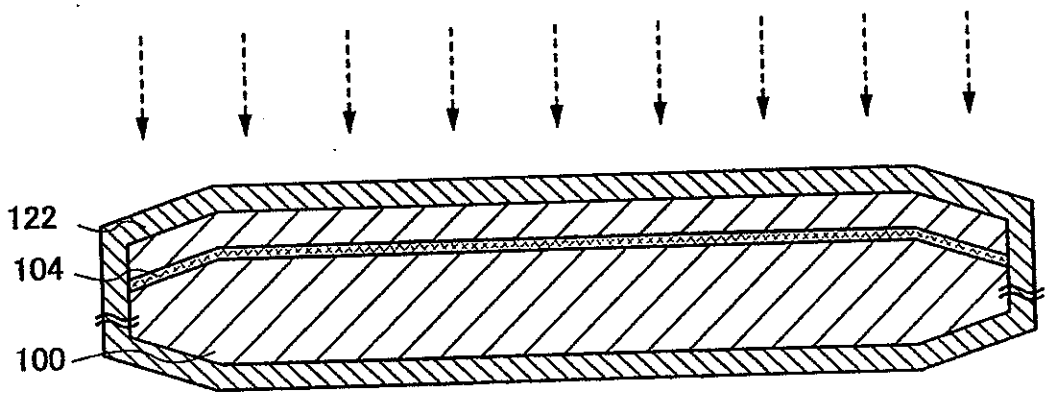


FIG. 4A

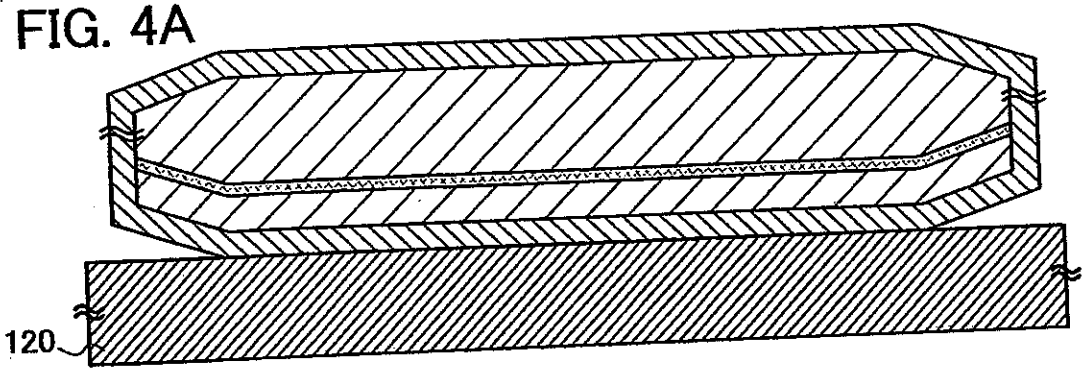


FIG. 4B

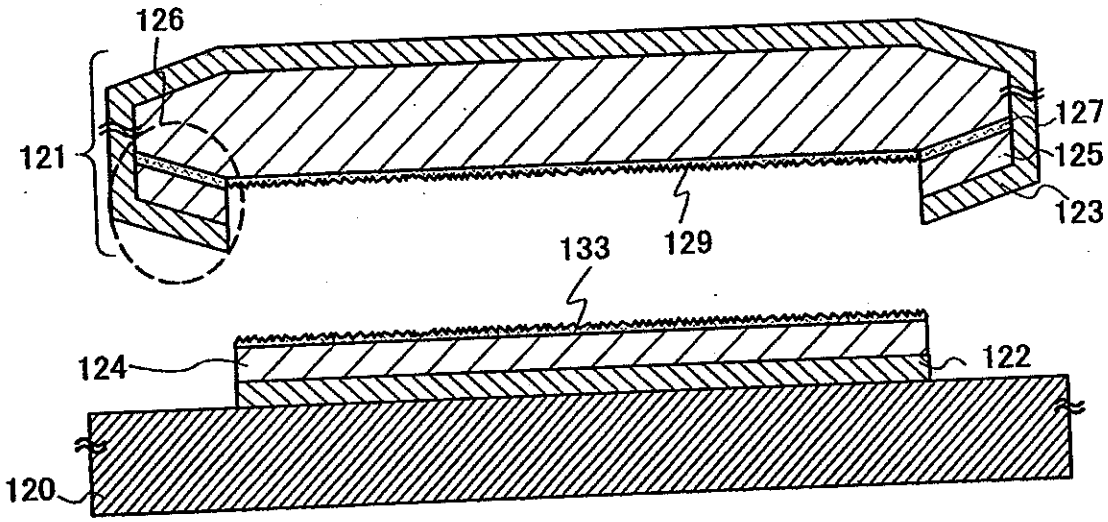


FIG. 4C

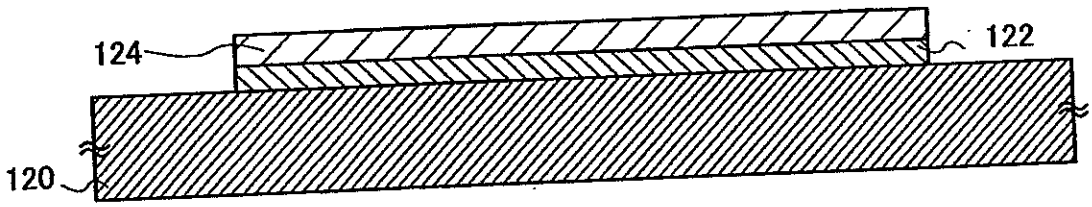


FIG. 5A

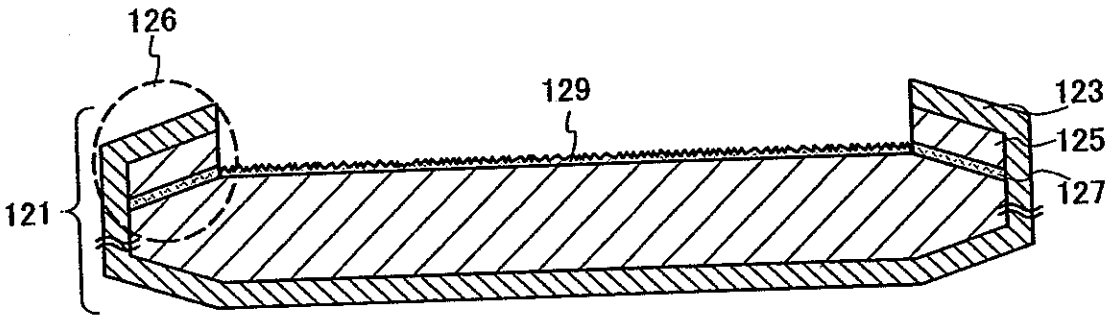


FIG. 5B

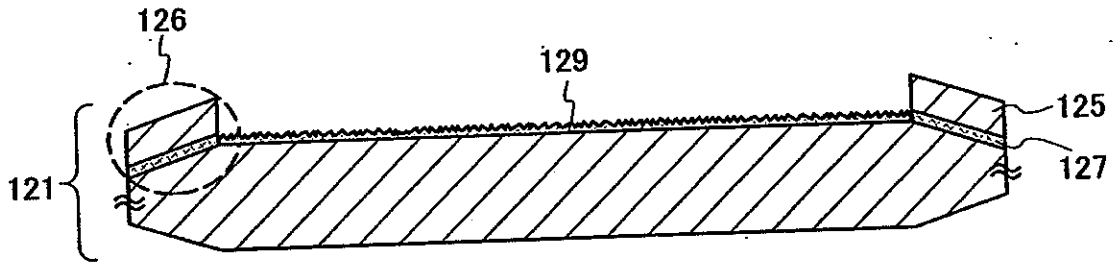


FIG. 5C

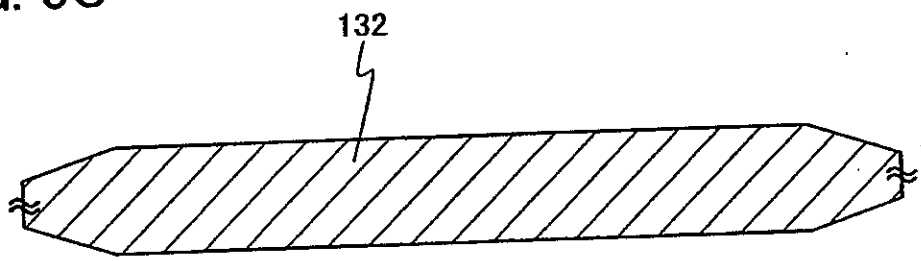


FIG. 6

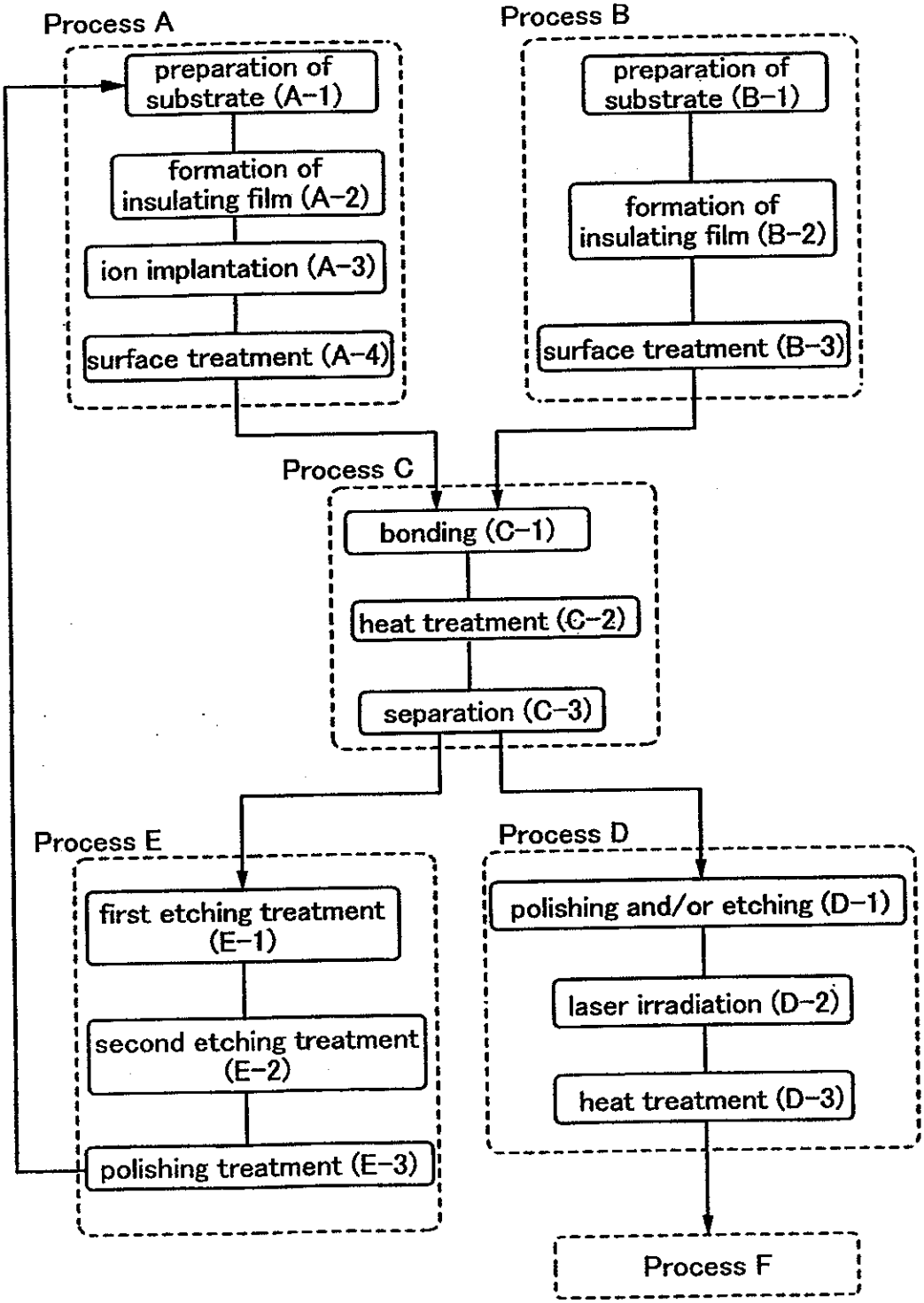
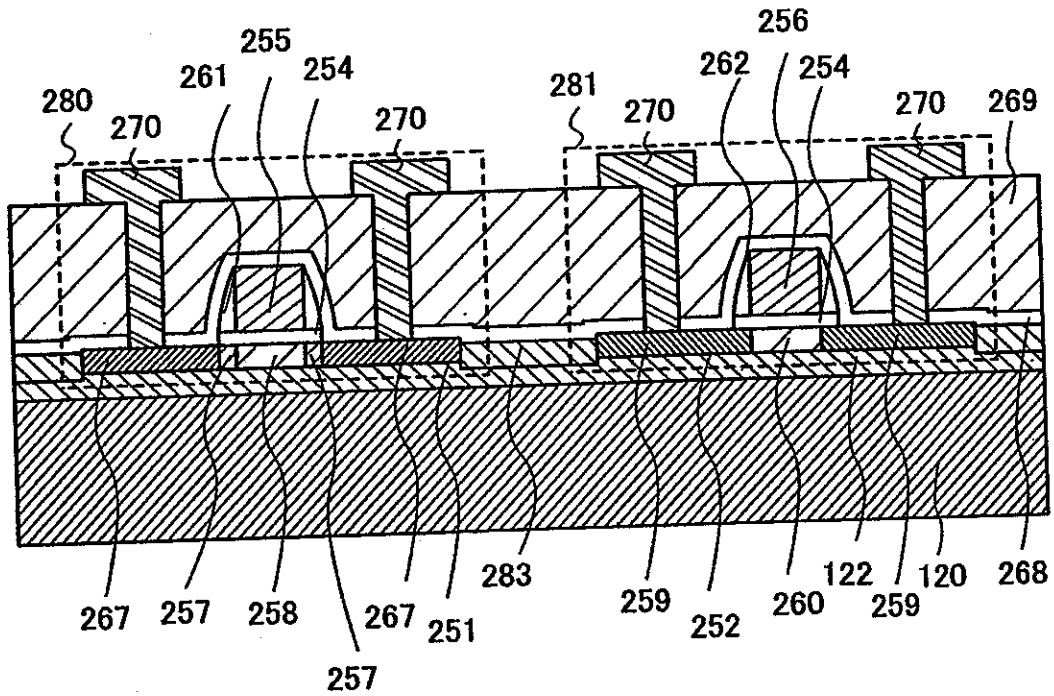

Process A
preparation of substrate (A-1)
formation of insulating film (A-2)
ion implantation (A-3)
surface treatment (A-4)
Process B
preparation of substrate (B-1)
formation of insulating film (B-2)
surface treatment (B-3)
Process C
bonding (C-1)
heat treatment (C-2)
separation (C-3)
Process E
first etching treatment (E-1)
second etching treatment (E-2)
polishing treatment (E-3)
Process D
polishing and/or etching (D-1)
laser irradiation (D-2)
heat treatment (D-3)
Process F

FIG. 7


280
270
261
255
254
270
281
270
262
256
254
270
269
267
257
258
257
267
251
283
259
252
260
122
259
120
268

REFERENCE NUMERALS

100: semiconductor substrate, 104: embrittlement layer, 120: base substrate, 121: semiconductor substrate after separation, 122: insulating film, 123: insulating film, 124: semiconductor film, 125: semiconductor layer, 126: projecting portion, 127: embrittlement layer, 129: separation plane, 130: semiconductor substrate after separation, 132: reprocessed semiconductor substrate, 133: separation plane, 251: element region, 252: element region, 254: insulating film, 255: gate electrode, 256: gate electrode, 257: low-concentration impurity region, 258: channel formation region, 259: high-concentration impurity region, 260: channel formation region, 261: sidewall insulating film, 262: sidewall insulating film, 267: high-concentration impurity region, 268: insulating film, 269: interlayer insulating film, 270: wiring, 280: transistor, 281: transistor, 283: element separation layer