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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ANALOG-TO-DIGITAL SIGNAL CONVERTERS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to analog-to-digital (A—D) signal converters.

According to one feature of this invention there is provided an integrating analog-to-digital converter comprising an integrator for integrating an analog voltage to be converted and generating a voltage proportional to the time integration thereof; digital setting means for setting a digital value to determine the time during which said analog voltage is integrated; means for detecting when the level of the integrated voltage is above a pre-determined level; means for converting the output of the detecting means into a digital quantity proportional to the product of said analog voltage and the digital value to which said digital setting means is set said converting means including counter means for counting said digital quantity; and means for resetting said counter means to zero upon coincidence of the count therein with said digital value.

According to another feature of this invention an analog-to-digital converter comprises means providing a reference voltage; switch means for making and breaking connection to the input of an integrator with a source of analog voltage to be converted and with the means providing the reference voltage; means for detecting when the level of the output of said integrator is above a pre-determined level; counter means; a clock pulse generator the output of which is applied to the input of said counter means; a memory circuit for reading and memorizing counts attained by said counter means in response to signals from the level detecting means; and means for detecting coincidence of the count in said counter

means with a digital value set by a digital setting means, the whole arrangement being such that the converted analog voltage is integrated until said counter means, commencing at zero-count, achieves a count which coincides with the digital value set by said digital value setting means, the integrator output being then held until the counter means is filled and then a reference voltage of polarity opposite to that of the analog voltage is integrated, and analog-to-digital conversion is effected by feeding into the memory circuit the count attained by the counter means at the moment when the output of said integrator is returned to said predetermined level.

The accompanying Figure 1 shows a well known dual-slope integration type A—D converter and Figure 1b is a graphical figure explanatory of the operation thereof. The A—D converter of Figure 1 includes an integrator 1, a comparator 2 which detects the output level from the integrator, a gate 3 controlled by the output from the comparator, a counter 4 which counts output pulses from the gate, an oscillator 5 and a control circuit 6. In operation with this arrangement a reset signal from the control circuit 6 first resets the integrator 1 and the counter 4 after which the voltage V_x to be converted is integrated, and when the integrated value exceeds a pre-determined reference level (provided by a D.C. potential source 7), pulses from the oscillator 5 are passed through the gate 3 to the counter 4. When the output of the integrator falls back to the aforesaid reference level, pulses from the oscillator 5 no longer pass through the gate. There is thus obtained a count representative of the input voltage to be converted. A data-transfer signal is then applied from the control circuit 6 to cause the count reached in the counter to be displayed by a suitable display device D and A—D conversion is terminated.

The following equations apply to the arrangement of Figure 1 operated as just described:—

50
55
60
65
70
75
80
85
90

$$T_x = \frac{\bar{V}_x}{V_r} T_r \quad (1)$$

and

$$\bar{V}_x = \frac{1}{T_x} \int_0^{T_x} V_x dt \quad (2)$$

where V_x is the voltage to be converted; T_x is the time commencing at the instant of reaching the reference level, during which the voltage V_x is integrated; V_r is the reference voltage; and T_r is the time in which the reference voltage V_r is integrated and which is given by equation (1). As is known if an alternating current noise or other disturbing alternating voltage is superimposed upon V_r , its disturbing influence can be reduced to a negligible amount by making T_r equal to an integral number of periods of frequency of the disturbance.

Figure 1b shows typical waveforms at various parts of the circuitry of Figure 1. This Figure 1b is thought to be self explanatory in view of the preceding description to the legends on the said figure.

Normal practice with a conventional dual-slope A—D converter as shown in Figure 1 is to make T_x equal to an integral number of periods of the frequency of the superposed disturbance voltage by suitably adjusting the frequency of the oscillator 5. Again normal practice with a conventional A—D converter is to use a mains or other commercial supply for its power source, and accordingly, a stable time base T_x is obtainable by relying on the frequency of the said supply. However, in the case of an A—D converter which is driven by a battery, it is not easy to obtain a simple and stable oscillator. In fact it is difficult to obtain an oscillator of sufficient frequency precision and stability without resorting to a quartz crystal oscillator. However, since the oscillator frequency has to be determined at a value which makes it right for eliminating superimposed disturbance, as above described, low cost mass-produced quartz crystal vibrators such as are commonly employed in colour television sets or quartz crystal timepieces are not suitable for use in a conventional A—D converter as represented in Figure 1. Furthermore, since the control circuit 6 operates independently of the timing of the clock-pulse oscillator 5, the lowest digit of the converted (digital) value displayed flickers and this is displeasing to the user. Furthermore, the oscillator in the control circuit involves the use of a capacitor of relatively large capacitance and if the display device D is of the liquid crystal type, an additional oscillator for driving the liquid crystal is necessary. Thus a conventional A—D converter as illustrated by Figure 1 requires the use of a substantial number of capacitors so that when integrated

circuit construction is employed for the converter, the provision of a substantial number of capacitors which are external to the integrated circuitry is involved. This necessity also militates against the achievement of low cost mass production.

The present invention seeks to provide improved A—D converters which do not have the above-mentioned defects and which can be made cheaply by mass production methods.

Figure 2 is a simplified diagram of one embodiment of this invention and Figures 3a, 3b and 4a are explanatory graphical figures explanatory of operation.

The converter shown in Figure 2 comprises switches S_1 , S_2 and S_3 controlled by a control circuit 6, an integrator 1 across which is a switch S_4 also controlled by the control circuit 6, a comparator 2, a flip-flop circuit 8, a differentiator 9, a clock-pulse oscillator 5, a counter within the broken line block 4, a digital value setting circuit 10, a coincidence detector 11 and a memory circuit 12 for reading the count in the counter by a trigger. The arrangement is such as to derive a digital quantity which is proportional to the product of said analog voltage and the digital value to which the digital setting means is set. This is important since it enables the constant of proportionality to be set at a high value. The switch S_4 is for re-setting the integrator. The oscillator 5 may be adjustable in frequency.

The A—D converter illustrated by Figure 2 will be described on the assumptions that it is to be used in an electronic wrist watch with a digital time display, and that the quartz vibrator 5 is the time standard of the watch and has a frequency of 16384 Hz. It is to be understood however that these assumptions are by way of practical example only and not limiting. It is also assumed again by way of example only, that the maximum count of the counter is 1999.

The quartz oscillator 5 is directly connected to the counter input which always counts and divides the frequency of the pulses from the said oscillator. On the foregoing assumption of a maximum count of 1999 the counter consists of three decimal counter sections 13, 14 and 15, and three binary counter sections 16, 17 and 18. In the binary counter sections, the first section 16 is used for counting the A—D converted value, the next two sections 17 and 18 are used for controlling the switches S_1 , S_2 , S_3 and S_4 through the control circuit 6 by providing the latter with signals.

In operation the converted voltage is integrated during a time starting when the counter is put into its reset state and ending when the count reaches a value N set by the digital value setting circuit. During this time the switch S_1 is closed. When the count reaches the value N, a signal from the coincidence detector 11 is fed to the control circuit 6,

and the switch S₁ is opened. The counter sections 13, 14, 15 and 17 are reset to zero count. At this point a reference voltage of polarity opposite to that of the voltage to be converted is selected by the control circuit 6 and applied to the integrator 1. Integration in the opposite direction commences. Incidentally it should be noted that when the output of the integrator 1 returns to the initial reference level, the comparator 2 is inverted, and the output thereof is read into the flip-flop circuit 8 synchronously with the clock pulse from the oscillator 5. The differentiator 9 is connected to the flip-flop circuit the output of which is therefore differentiated and transmitted as a data transfer signal to the memory circuit 12 in which, accordingly, the count at that time in the counter is memorized. By arranging the flip-flop circuit to be triggered by the rising (leading) edge of the clock pulse and arranging the counter to be triggered at the falling (lagging) edge thereof, it can be ensured that erroneous action due to the simultaneous feeding of the data transfer signal to the memory and the triggering of the counter by the clock pulse is avoided. The count read into the memory circuit and which is a digital quantity corresponding with the analog voltage to be converted is decoded and displayed (by means not shown in Figure 2) and/or fed out and utilised in any other desired manner. Incidentally it should be noted that when the counter sections 13, 14, 15 and 16 are filled, the counter section 18 is set. The output signal from this counter section 18 is fed to the control circuit to cause it to reset the integrator. The A—D conversion is now complete. It is not essential to the invention that the relative timing between the feeding in of data to the counter and feeding in of input to the integrator should be as above described and other timing relations can be adopted. For example, the time during which the voltage to be converted is integrated need not start at the instant when the counter is in the reset state but could be arranged to start when the counter is in a certain pre-determined state, though obviously the adoption of such timing would involve a certain amount of extra complication in the control circuit 6.

If one assumes a superimposed disturbing voltage with a fundamental frequency of 50 Hz or of 60 Hz (these are the mains frequencies commonly used in different parts of the world) it is necessary, in order to get rid of disturbance by such superimposed voltages to make the integral of the converted voltage some integral multiples of 100 msec.

Assuming a full count of 1999 and a quartz vibrator of 16380 Hz are used if the voltage to be converted is integrated over a time commencing when the counter is reset and ending at a full count, the integration time will be about 122.1 msec., and consequently the

desired result of a high degree of elimination of the superposed disturbance will not be obtained. If, however, 1638 is set in the digital value-setting circuit, the integration time for the voltage to be converted will be about 99.98 msec., and the superimposed disturbing voltage will be, in effect, brought down to a value which may be taken to be 0.02% (−74dB) i.e. its disturbing effect will be brought down to a negligible value.

Since the A—D converter above described with reference to Figure 2 is completely synchronous as regards operation of the control circuit, there will be no flickering of the lowest digit of the converted value as is the case with a conventional A—D converter having a clock pulse oscillator which is separate from and independent of the oscillator used for control circuit. A further advantage is that, because since the counter in Figure 2 is always driven by the oscillator 5 an alternating voltage for driving a liquid crystal display and a clock pulse for a multiplexer can be obtained from any divider stage in the counter.

Because of the way in which the voltage to be converted is converted into a digital value, and the way in which the proportion between them is determined, it is obviously simple to obtain a multiplication effect as between the analog quantity and the set digital quantity i.e. the constant of proportionality may be made of high value. By arranging for the reference level to be changed in correspondence with and to suit the digital value-setting circuit, a very high degree of elimination of disturbance by superposed alternating voltage can be obtained whatever the frequency of said superposed alternating voltage by adjusting the set digital value or the reference level or both.

Because, in an A—D converter in accordance with this invention, the integration time of the voltage to be converted can be suitably adjusted, a relatively simple and cheap quartz vibrator such as is commonly used for clock pulse oscillators, can be employed. Moreover, because the counter is always driven by the clock pulses, various alternating voltages (including the control signals for the control circuit 6) which may be desired can be obtained from the counter, so that it is no longer necessary to provide separately oscillators for performing desired functions (including providing control signals for the control circuit 6). This makes it easy to construct an integrated circuit without providing any large capacitance capacitors. As already pointed out, because the control circuit is completely synchronous with the counter, stable analog to digital conversion is obtainable even as regards the lowest digit in the converted digital value. A converter in accordance with this invention is particularly advantageous for use as a battery driven converter since it overcomes the difficulty of obtaining a stable time base. How-

ever the advantages of the invention make it of very wide applicability in practice.

Typical "idealised" wave forms at various points in the circuitry of Figure 2 are shown in Figure 3(a) and (b) which, in view of the legends thereon and of the description already given, will be thought largely self-explanatory. Figure 3(a) is in effect, a time chart illustrative of the general operation of the converter shown in Figure 2. Figure 3(b) is a time chart designed to show what happens when a data transfer signal is generated, the time axis in Figure 3(b) being accordingly extended to be longer than that used in Figure 3(a). Figures 3(a) and 4(a) are alike apart from the fact that the time distribution of the output pulses from the counter section 16 is, in Figure 3(a) a little different from what it is in Figure 4a (where it is uniform throughout) with consequent minor differences between corresponding other parts of the two figures.

WHAT WE CLAIM IS:—

1. An integrating analog-to-digital converter comprising an integrator for integrating an analog voltage to be converted and generating a voltage proportional to the time integral thereof; digital setting means for setting a digital value to determine the time during which said analog voltage is integrated; means for detecting when the level of the integrated voltage is above a pre-determined level; and means for converting the output of the detecting means into a digital quantity proportional to the product of said analog voltage and the digital value to which said digital setting means is set; said converting means including counter means for counting said digital quantity; and means for resetting said counter means to zero upon coincidence of the count therein with said digital value.

2. A converter as claimed in claim 1 and comprising an oscillator of pre-determined frequency from which are derived pulses which are counted by said counter means.

3. A converter as claimed in claim 2 and comprising means for adjusting the frequency of said oscillator.

4. A converter as claimed in claim 1 and comprising means providing a reference voltage; switch means for making and breaking connection of the integrator with the source of analog voltage and with said means for providing said reference voltage; a clock pulse generator the output of which is applied permanently to the input of said counter means; a memory circuit for reading and memorizing counts attained by said counter means in response to signals from the level detecting means; and means for detecting coincidence of the count in said counter means with the

digital value set by the digital setting means, the whole arrangement being such that the converted analog voltage is integrated until said counter means, commencing at zero-count achieves a count which coincides with the digital value set by said digital value setting means, whereupon said counter means is reset, a reference voltage of polarity opposite to that of the analog voltage is integrated, and analog-to-digital conversion is effected by feeding into the memory circuit the count attained by the counter means at the moment when the output of said integrator is returned to said predetermined level.

5. An analog to digital converter comprising means providing a reference voltage; switch means for making and breaking connection to the input of an integrator with a source of analog voltage to be converted and with the means providing the reference voltage; means for detecting when the level of the output of said integrator is above a pre-determined level; counter means; a clock pulse generator the output of which is applied to the input of said counter means; a memory circuit for reading and memorizing counts attained by said counter means in response to signals from the level detecting means; and means for detecting coincidence of the count in said counter means with a digital value set by a digital setting means, the whole arrangement being such that the converted analog voltage is integrated until said counter means, commencing at zero-count, achieves a count which coincides with the digital value set by said digital value setting means, the integrator output being then held until the counter means is filled and then a reference voltage of polarity opposite to that of the analogue voltage is integrated, and analog-to-digital conversion is effected by feeding into the memory circuit the count attained by the counter means at the moment when the output of said integrator is returned to said predetermined level.

6. An analog to digital converter substantially as herein described with reference to the accompanying Figures 2, 3(a) and 3(b).

7. An electronic timepiece having a digital time display and including a converter as claimed in any of the preceding claims.

8. A timepiece as claimed in claim 2 and 7 wherein the oscillator is the time standard oscillator of the timepiece.

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2. A converter as claimed in claim 1 and comprising an oscillator of pre-determined frequency from which are derived pulses which are counted by said counter means.
3. A converter as claimed in claim 2 and comprising means for adjusting the frequency of said oscillator.
4. A converter as claimed in claim 1 and comprising means providing a reference voltage; switch means for making and breaking connection of the integrator with the source of analog voltage and with said means for providing said reference voltage; a clock pulse generator the output of which is applied permanently to the input of said counter means; a memory circuit for reading and memorizing counts attained by said counter means in response to signals from the level detecting means; and means for detecting coincidence of the count in said counter means with the

digital value set by the digital setting means, the whole arrangement being such that the converted analog voltage is integrated until said counter means, commencing at zero-count achieves a count which coincides with the digital value set by said digital value setting means, whereupon said counter means is reset, a reference voltage of polarity opposite to that of the analog voltage is integrated, and analog-to-digital conversion is effected by feeding into the memory circuit the count attained by the counter means at the moment when the output of said integrator is returned to said predetermined level.

5. An analog to digital converter comprising means providing a reference voltage; switch means for making and breaking connection to the input of an integrator with a source of analog voltage to be converted and with the means providing the reference voltage; means for detecting when the level of the output of said integrator is above a pre-determined level; counter means; a clock pulse generator the output of which is applied to the input of said counter means; a memory circuit for reading and memorizing counts attained by said counter means in response to signals from the level detecting means; and means for detecting coincidence of the count in said counter means with a digital value set by a digital setting means, the whole arrangement being such that the converted analog voltage is integrated until said counter means, commencing at zero-count, achieves a count which coincides with the digital value set by said digital value setting means, the integrator output being then held until the counter means is filled and then a reference voltage of polarity opposite to that of the analogue voltage is integrated, and analog-to-digital conversion is effected by feeding into the memory circuit the count attained by the counter means at the moment when the output of said integrator is returned to said predetermined level.

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