

ABSTRACT OF THE INVENTION

MULTILAYER INTERCONNECT STRUCTURE AND METHOD FOR INTEGRATED CIRCUITS

A multilayer interconnect structure is formed by, providing a substrate (40) having thereon a first dielectric (50, 27) for supporting a multi-layer interconnection (39) having lower conductor M_N (22, 23), upper conductor M_{N+1} (34, 35), dielectric interlayer (DIL) (68) and interconnecting via conductor $V_{N+1/N}$ (36, 36'). The lower conductor M_N (22, 23) has a first upper surface (61) located in a recess below a second upper surface (56) of the first dielectric (50, 27). The DIL (68) is formed above the first (61) and second (56) surfaces. A cavity (1263) is etched through the DIL (68) from a desired location (122) of the upper conductor M_{N+1} (34), exposing the first surface (61). The cavity (1263) is filled with a further electrical conductor (80) to form the upper conductor M_{N+1} (34) and the connecting via conductor $V_{N+1/N}$ (36, 36') making electrical contact with the first upper surface (61). A critical dimension (32, 37) between others (23) of lower conductors M_N (22, 23) and the via conductor $V_{N+1/N}$ (36, 36') is lengthened. Leakage current and electro-migration therebetween are reduced.

Fig. 17