1. A 3D semiconductor device, the device comprising;

a plurality of first transistors, overlaid by a plurality of second transistors, overlaid by a plurality of third transistors, overlaid by a plurality of fourth transistors,

wherein said second transistors, said third transistors and said fourth transistors are self-aligned, having been processed following the same lithography step, and

wherein at least one of said first transistors is part of a control circuit controlling at least one of said second transistors, at least one of said third transistors and at least one of said fourth transistors.

2. The device according to claim 1,

wherein said third transistors are junction-less transistors, and

wherein said junction-less transistors comprise a single crystal channel.

3. The device according to claim 1,

wherein said third transistors are junction-less transistors, and

wherein said junction-less transistors comprise a polysilicon channel.

4. The device according to claim 1,

wherein said third transistors are junction-less transistors.

5. The device according to claim 1,

wherein said first transistors comprise a single crystal channel.

6. The device according to claim 1, further comprising:

a memory cell,

wherein said memory cell comprises at least one of said third transistors.

7. The device according to claim 1, further comprising:

a memory peripheral circuit,

wherein said memory peripheral circuit comprises at least one of said first transistors.

8. A 3D semiconductor device, the device comprising:

a plurality of first transistors, overlaid by a plurality of second memory cells, overlaid by a plurality of third memory cells, overlaid by a plurality of fourth memory cells,

wherein said second memory cells, said third memory cells and said fourth memory cells are self-aligned, having been processed following the same lithography step, and

wherein at least one of said first transistors is part of a control circuit controlling at least one of said second memory cells, at least one of said third memory cells and at least one of said fourth memory cells, and

wherein at least one of said second memory cells comprises second transistors, at least one of said second transistors is a junction-less transistor.

9. The device according to claim 8,

wherein said third memory cells comprise at least one junction-less transistor, and

wherein said at least one junction-less transistor comprises a single crystal channel.

10. The device according to claim 8,

wherein said third memory cells comprise at least one junction-less transistor, and

wherein said at least one junction-less transistor comprises a polysilicon channel.

11. The device according to claim 8,

wherein said third memory cells comprise at least one junction-less transistor.

12. The device according to claim 8,

wherein said first transistors comprise a single crystal channel.

13. The device according to claim 8, further comprising:

a memory cells peripheral circuit,

wherein said memory cells peripheral circuit comprises at least one of said first transistors.

14. The device according to claim 8,

wherein at least one of said second memory cells is overlaying said at least one of said first transistors.

15. A 3D semiconductor device, the device comprising:

a plurality of first transistors, overlaid by a plurality of second transistors, overlaid by a plurality of third transistors, overlaid by a plurality of fourth transistors,

wherein said second transistors, said third transistors and said fourth transistors are self-aligned, having been processed following the same lithography step, and

wherein at least one of said first transistors is part of a memory peripheral circuit controlling at least one of said second transistors, at least one of said third transistors and at least one of said fourth transistors, and

a first memory cell,

wherein said first memory cell comprises at least one of said second transistors.

16. The device according to claim 15,

wherein said third transistors are junction-less transistors, and

wherein said junction-less transistors comprise a single crystal channel.

17. The device according to claim 15,

wherein said third transistors are junction-less transistors, and

wherein said junction-less transistors comprise a polysilicon channel.

18. The device according to claim 15,

wherein said third transistors are junction-less transistors.

19. The device according to claim 15,

wherein said first transistors comprise a single crystal channel.

20. The device according to claim 15, further comprising:

a second memory cell,

wherein said second memory cell comprises at least one of said third transistors.