WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor layer comprising one or more first synaptic cores, each first synaptic core comprising a plurality of neural circuits to perform neuromorphic computation;

a second semiconductor layer stacked on the first semiconductor layer and comprising an interconnect forming a physical transfer path between the one/or more first synaptic cores and/or one or more second synaptic cores;

a third semiconductor layer stacked on the second semiconductor layer and comprising the one or more second synaptic cores; and

one or more through electrodes, through which information is transferred between the first through third semiconductor layers,

wherein information from a first synaptic core in the first semiconductor layer is transferred to a second synaptic core in the third semiconductor layer via the one or more through electrodes and the interconnect of the second semiconductor layer; and

wherein each first synaptic core further comprises a local router for determining an information transfer path between the plurality of neural circuits and a local interconnect forming a physical information transfer path in each first synaptic core.

2. The semiconductor device of claim 1, wherein the through electrode is a through silicon via (TSV).

3. The semiconductor device of claim 1 or claim 2, wherein the second semiconductor layer further comprises a router for determining an information transfer path between the synaptic cores.

4. The semiconductor device of any one of claims 1 to 2, wherein each of the first and third semiconductor layers further comprises a router for determining an information transfer path between the synaptic cores.

5. The semiconductor device of claim 4, wherein the synaptic cores further comprise memristers for storing synapse information and performing weight computation

by using the synapse information.

6. The semiconductor device of any one of claims 1 to 5, wherein the neuromorphic computation comprises a computation of nodes having a plurality of layer structures, and a computation result of first nodes belonging to a first layer from among the nodes is provided to second nodes belonging to a second layer,

wherein the first nodes are included in the first synaptic core of the first semiconductor layer, and the second nodes are included in the second synaptic core of the third semiconductor layer.

7. The semiconductor device of any one of claims 1 to 6, wherein first information from the first synaptic core in the first semiconductor layer is transferred to the second synaptic core in the third semiconductor layer through the interconnect of the second semiconductor layer, and

second information from the first synaptic core in the first semiconductor layer is transferred to a third synaptic core in the first semiconductor layer through an interconnect of the second semiconductor layer.

8. The semiconductor device of any one of claims 1 to 7, wherein the semiconductor device comprises N semiconductor layers including the first through third semiconductor layers, where N is an integer greater than 3, and

wherein the N semiconductor layers are implemented such that some of the N semiconductor layers include a synaptic core and some of the N semiconductor layers include an interconnect, wherein the some of the N semiconductor layers including a synaptic core, and the some of the N semiconductor layers including an interconnect, are alternately stacked.

9. The semiconductor device of any one of claims 1 to 8, wherein the one or more through electrodes is formed within at least one of the first, second or third semiconductor layers.

10. A neuromorphic circuit comprising:

a synaptic core layer comprising a plurality of synaptic cores, each synaptic core

comprising a plurality of neural circuits and a memory array storing synapse information;

global routers each configured to determine an information transfer path between the plurality of synaptic cores; and

a global interconnect layer forming a physical transfer path between the global routers,

wherein the synaptic core layer and the global interconnect layer are arranged in a stack structure, and information from a synaptic core of the synaptic core layer is transferred to the global interconnect layer via one or more through electrodes; and

wherein each of the synaptic cores comprises a local router determining an information transfer path between the plurality of neural circuits and a local interconnect forming a physical information transfer path in each of the synaptic cores.

11. The neuromorphic circuit of claim 10, wherein the one or more through electrode is a through silicon via (TSV).

12. The neuromorphic circuit of claim 10 or claim 11, wherein the global routers are integrated in the synaptic core layer with the synaptic cores.

13. The neuromorphic circuit of any one of claims 10 or claim 11, wherein the global routers are integrated in the global interconnect layer along with a global interconnect.

14. The neuromorphic circuit of claim 13, wherein the neuromorphic circuit comprises first through Nth semiconductor layers (where N is an integer greater than 2) including the synaptic core layer and the global interconnect layer, the first semiconductor layer is the synaptic core layer, and the second semiconductor layer is the global interconnect layer, and

the first through Nth semiconductor layers are implemented such that synaptic core and global interconnect layers thereof are alternately stacked.

15. The neuromorphic circuit of claim 14, wherein the synaptic core layer comprises first through third semiconductor layers that have a stacked structure and communicate with each other via through electrodes,

wherein some of a plurality of neural circuits of any one synaptic core are formed in the first semiconductor layer, the local interconnect is formed in the second semiconductor layer stacked on the first semiconductor layer, and other ones of the plurality of neural circuits are formed in the third semiconductor layer.

16. The neuromorphic circuit of claim 15, wherein the local router is formed in the second semiconductor layer along with the local interconnect.

17. The neuromorphic circuit of claim 15 or claim 16, wherein the local router is formed in the first semiconductor layer and the third semiconductor layer along with the plurality of neural circuits.

18. The neuromorphic circuit of any one of claims 10 to 17, wherein the memory array comprises memristers.