ABSTRACT

A semiconductor memory device includes an interface semiconductor die, at least one memory semiconductor die, and through-silicon vias connecting the interface semiconductor die and the memory semiconductor die. The interface semiconductor die includes command pins to receive command signals transferred from a memory controller and an interface command decoder to decode the command signals. The memory semiconductor die includes a memory integrated circuit configured to store data and a memory command decoder to decode the command signals transferred from the interface semiconductor die. The interface semiconductor die does not include a clock enable pin to receive a clock enable signal from the memory controller. The interface and memory command decoders generate interface and memory clock enable signals to control clock supply with respect to the interface and memory semiconductor dies based on a power mode command transferred through the plurality of command pins from the memory controller.

FIG. 1