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DEMODULATOR LOGIC FOR FREQUENCY SHIFT KEYED SIGNALS

This invention relates to demodulator logic for frequency shift keyed (FSK) signals on an RF carrier.

British patent 1,517,121 discloses a radio receiver of the so-called "direct conversion" type, also known as a "zero IF" receiver, in which FSK signals are mixed with a local oscillator to provide quadrature baseband signals which are then applied to a simple demodulating logic in the form of a clocked D-type flip-flop. In a described modification of the basic logic one of the two quadrature signals is applied to the clock input of a first D-type flip-flop and to the D input of a second D-type flip-flop whilst the other quadrature signal is applied to the D input of the first flip-flop and the clock input of the second flip-flop. The Q output of one flip-flop and the Q output of the other flip-flop are then algebraically summed to provide the demodulated output.

According to the present invention there is provided a demodulator logic arrangement for FSK signals on an RF carrier in a direct conversion radio receiver, wherein the received signals are mixed with a local oscillator to provide quadrature baseband signals, characterised in that the demodulator logic comprises two clocked D-type flip-flops, one baseband signal being applied direct to the clock input of one flip-flop and inverted to the clock input of the other flip-flop, the

second baseband signal being applied to the D inputs of both flip-flops, one output from one flip-flop being algebraically combined with one output from the other flip-flop to provide a demodulator signal output of the receiver, the two flip-flop outputs being chosen so that for a given FSK value they always have the same logic value.

Embodiments of the invention will now be described with reference to the accompanying drawings, wherein:-

Figs. 1A and 1B illustrate one demodulator logic arrangement and associated waveforms, and

Fig. 2 illustrates an alternative logic arrangement.

In the arrangement of Fig. 1A the two quadrature baseband signals A and B (corresponding to the A & B signals in Fig. 1 of patent 1,517,121) are applied to two clocked D-type flip-flops FF1 and FF2 in the following manner. The B baseband signal is applied direct to the D inputs of both FF1 and FF2. The A signal, in quadrature with respect to the B signal, is fed direct to the clock input of FF1 and via an inverter 11 to the clock input of FF2. The Q output of FF1 and the Q output of FF2 are each fed, via resistances, to a summing point X. Fig. 1B shows the A & B waveforms for FSK logic level '1' as they are applied to the flip-flops and the Q and $\overline{Q}$ output of FF1 and FF2 respectively. It will be noted that, irrespective of the current FSK value (i.e. whether A leads or lags B by 90°) the two flip-flops are now always clocked 180° out of phase, compared with the arrangement in patent 1,517,121 where they can be clocked 270° apart.

In the arrangement shown in Fig. 2A the B signal is fed direct to the D input of FF1 and inverted to the clock input of FF2. The A signal is fed direct to the clock input of FF1 and inverted to the clock input of FF2. The Q outputs of both FF1 and FF2 are then summed.

The waveforms for FSK logic level '1' are shown in Fig. 2B.

In both arrangements it is to be noted that the two flip-flops are always clocked 180° out of phase, regardless of whether the A signal leads or lags the B signal by 90° (i.e. regardless of whether the FSK logic level is '0' or '1'). In the two flip-flop arrangements disclosed in patent 1,517,121 it is possible for the flip-flops to be clocked 270° apart. The present invention thus reduces the jitter in the demodulated output by the same amount.

It is to be understood that the means whereby the A & B signals are obtained in quadrature is immaterial to the present invention, e.g. they can be produced in a direct conversion receiver in which the 90° phase shift can be obtained in either the r.f. input to the A & B channels, or in the local oscillator input to the A & B channels, or in arrangements where the phase shift is obtained by the use of $\pm$ 45° phase shift network in each channel.

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CLAIMS:-

1. A demodulator logic arrangement for FSK signals on an RF carrier in a direct conversion radio receiver, wherein the received signals are mixed with a local oscillator to provide quadrature baseband signals, characterised in that the demodulator logic comprises two clocked D-type flip-flops, one baseband signal being applied direct to the clock input of one flip-flop and inverted to the clock input of the other flip-flop, the second baseband signal being applied to the D inputs of both flip-flops, one output from one flip-flop being algebraically combined with one output from the other flip-flop to provide a demodulator signal output of the receiver, the two flip-flop outputs being chosen so that for a given FSK value they always have the same logic value.

2. A logic arrangement according to claim 1 characterised in that the second baseband signal is applied direct to the D inputs of both flip-flops and that the normal output of one flip-flop is algebraically combined with the complementary output of the other flip-flop.

3. A logic arrangement according to claim 1 characterised in that both baseband signals are applied direct to the respective inputs of one flip-flop and both baseband signals are applied inverted to the corresponding inputs of the second flip-flop, one output from one flip-flop being algebraically summed with the corresponding output from the other flip-flop.

4. A demodulator logic arrangement for FSK signals substantially as described with reference to Fig. 1A or Fig. 2A of the accompanying drawings.