

ABSTRACT OF THE DISCLOSURE

A vertical memory device includes a plurality of word lines on a substrate, a plurality of word line cut regions extending parallel to each other, a memory cell array comprising a plurality of channel structures extending on the substrate through the plurality of word lines and arranged in a honeycomb structure, a plurality of contacts on the plurality of channel structures, and a plurality of bit lines connected to the plurality of channel structures through the plurality of contacts. The memory cell array comprises a first sub-array and a second sub-array, which are defined by the plurality of word line cut regions and are connected to some identical bit lines from among the plurality of bit lines, and a layout of contacts in the first sub-array from among the plurality of contacts is different from a layout of contacts in the second sub-array from among the plurality of contacts.

FIG. 4