

ABSTRACT

An integrated circuit includes a semiconductor substrate, first through third power rails, and first through fourth clock gate lines. The first power rail through third power rails are formed above the semiconductor substrate, and extend in a first direction and arranged sequentially in a second direction perpendicular to the first direction. The first through fourth clock gate lines are formed above the semiconductor substrate, and extend in the second direction to pass through a first region between the first power rail and the second power rail and a second region between the second power rail and the third power rail. The first clock gate line and the second clock gate line are arranged to be adjacent to each other in the first direction, and the third clock gate line and the fourth clock gate line are arranged to be adjacent to each other in the first direction.

FIG. 1