WHAT IS CLAIMED IS:

1. An image signal processor for generating a converted image based on a raw image provided by an image sensor, the image signal processor comprising:

processing circuitry configured to

store data corresponding to a plurality of lines of a received image in a line buffer;

perform an image processing operation by filtering the data stored in the line buffer based on at least one filter;

determine a number of sub-images into which the raw image is to be divided based on a width of the raw image, a width of the line buffer, and a width of an overlap region, the width of the overlap region being a region shared between at least two adjacent sub-images;

divide the raw image into a plurality of sub-images equal to the determined number of sub-images and request the plurality of sub-images from a memory in which the raw image is stored, such that the plurality of sub-images are sequentially received by the line buffer, a width of each of the plurality of sub-images being less than the width of the line buffer, and the plurality of sub-images being parallel to each other,

image-process the plurality of sub-images in an order in which the plurality of sub-images are received by the line buffer to generate a plurality of converted sub-images; and

merge the plurality of converted sub-images into the converted image having a same size as the raw image, by storing the plurality of converted sub-images in the memory in an order in which the plurality of converted sub-images are generated,

wherein each of the plurality of converted sub-images comprises a converted overlap region, the converted overlap region being an area generated by image-processing the overlap region of the at least two adjacent sub-images, and

wherein the processing circuitry stores a second converted sub-image in the memory after storing a first converted sub-image in the memory, and overwrites a first converted overlap region of the first converted sub-image stored in the memory with data of a second converted overlap region of the second converted sub-image.

2. The image signal processor of claim 1, wherein the processing circuitry is configured to divide the raw image into the plurality of sub-images such that the at least two adjacent sub-images partially overlap each other.

3. The image signal processor of claim 2, wherein the processing circuitry is configured to determine the width of the overlap region based on a size of the at least one filter.

4. The image signal processor of claim 3, wherein the at least one filter comprises a finite impulse response (FIR) filter.

5. The image signal processor of claim 3 or claim 4, wherein the processing circuitry is configured to determine the width of each of the plurality of sub-images based on the width of the raw image, the width of the line buffer, and the width of the overlap region.

6. The image signal processor of claim 1, wherein the processing circuitry is configured to determine an address of a region in which the plurality of converted sub-images are to be stored, such that the plurality of converted sub-images stored in the memory constitute the converted image.

7. The image signal processor of any one of claims 1 to 6, wherein the processing circuitry is further configured to convert a size of the converted image based on a resolution of a display device.

8. The image signal processor of claim 7, wherein

the width of the raw image provided by the image sensor is equal to or less than the width of the line buffer in a first operation mode, and

the width of the raw image provided by the image sensor is greater than the width of the line buffer in a second operation mode.

9. The image signal processor of claim 8, wherein, in the first operation mode, the processing circuitry is configured to image-process the raw image to generate the converted image, and scale the converted image to generate a scaled image.

10. The image signal processor of any one of claims 1 to 9, wherein the memory is configured to store the raw image received from the image sensor and sequentially provide the plurality of sub-images of the raw image to the line buffer in response to the request for the plurality of sub-images.

11. The image signal processor of any one of claims 1 to 10, wherein the memory comprises a buffer included in the image sensor.

12. A method of operating an image signal processor configured to image-process a raw image generated by an image sensor, wherein the image signal processor includes a line buffer having a size smaller than a width of the raw image and at least one filter, the method comprising:

determining a number of stripe images into which the raw image is to be divided based on the width of the raw image, the size of the line buffer, and a width of an overlap region, the width of the overlap region being a region shared between two adjacent stripe images;

dividing the raw image into a plurality of stripe images equal to the determined number of stripe images, a size of each of the plurality of stripe images in a first direction being less than the size of the line buffer, and the plurality of stripe images being parallel to each other;

sequentially image-processing the plurality of stripe images by using the line buffer and the at least one filter to generate a plurality of converted stripe images; and

merging the plurality of converted stripe images into a converted image having a same size as the raw image, by storing the plurality of converted stripe images in a memory,

wherein each of the plurality of converted stripe images comprises a converted overlap region, the converted overlap region being an area generated by image-processing the overlap region of the two adjacent stripe images, and

wherein a second converted stripe image is stored in the memory after a first converted stripe image is stored in the memory, and overwrites a first converted overlap region of the first converted stripe image stored in the memory with data of a second converted overlap region of the second converted stripe image.

13. The method of claim 12, wherein the two adjacent stripe images of the plurality of stripe images partially overlap each other.

14. The method of claim 13, wherein the width of the overlap region is determined based on a size of the at least one filter.

15. The method of any one of claims 12 to 14, wherein the sequentially image-processing of the plurality of stripe images comprises:

sequentially receiving a first stripe image of the plurality of stripe images in units of lines from an external memory of the image signal processor in which the raw image is stored, the sequentially receiving the first stripe image being performed by the line buffer;

filtering data of the first stripe image stored in the line buffer and generating the converted first stripe image, the filtering and the generating being performed by the at least one filter;

sequentially receiving a second stripe image of the plurality of stripe images in units of lines from the external memory upon the generating of the converted first stripe image being completed, the sequentially receiving the second stripe image being performed by the line buffer; and

filtering data of the second stripe image stored in the line buffer and generating the converted second stripe image, the filtering and the generating being performed by the at least one filter.

16. An application processor comprising:

an image signal processor configured to image-process a raw image generated by an image sensor and generate a converted image; and

an image compression encoder configured to compress the converted image,

in a second operation mode, the image signal processor being configured to

determine a number of sub-images into which the raw image is to be divided based on a width of the raw image, a size of a line buffer, and a width of an overlap region, the width of the overlap region being a region shared between at least two adjacent sub-images;

divide the raw image into a plurality of sub-images equal to the determined number of sub-images, sequentially image-process the plurality of sub-images, and generate a plurality of converted sub-images, by storing the plurality of sub-images in a memory,

wherein each of the plurality of converted sub-images comprises a converted overlap region, the converted overlap region being an area generated by image-processing the overlap region of the at least two adjacent sub-images, and

wherein the image signal processor stores a second converted sub-image in the memory after storing a first converted sub-image in the memory, and overwrites a first converted overlap region of the first converted sub-image stored in the memory with data of a second converted overlap region of the second converted sub-image.

17. The application processor of claim 16, wherein, in the second operation mode, the image signal processor is configured to merge the plurality of converted sub-images together into the converted image, the converted image having a same size as the raw image.

18. The application processor of claim 16 or claim 17, wherein

the image signal processor comprises the line buffer configured to store line data, and

in the second operation mode, the width of the raw image is greater than the size of the line buffer.