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(71) Applicant: QUALCOMM INCORPORATED [US/US];
ATTN: International IP Administration, 5775 Morehouse
Drive, San Diego, California 92121-1714 (US).

(72) Inventor: GARG, Manish; 5775 Morehouse Drive, San
Diego, California 92121 (US).

(74) Agent: TERRANOVA, Steven, N.; WITHROW & TER-
RANOVA, PLLC, 106 Pinedale Springs Way, Cary, North
Carolina 27511 (US).

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(54) Title: SEPARATE READ AND WRITE ADDRESS DECODING IN A MEMORY SYSTEM TO SUPPORT SIMULTANEOUS
MEMORY READ AND WRITE OPERATIONS

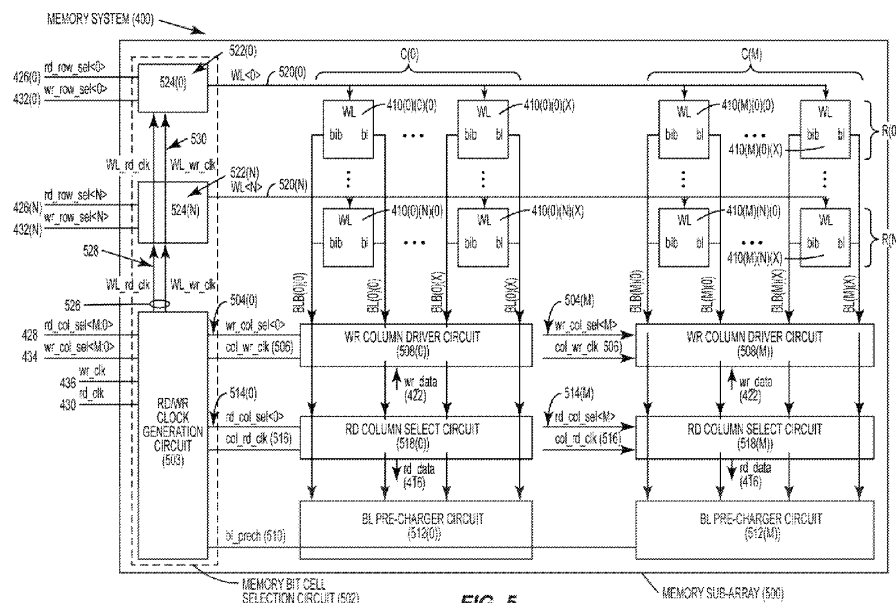


FIG. 5

(57) Abstract: Memory systems that provide separate read and write address decoding to support simultaneous memory read and write operations are disclosed. Separating read and write address decoding can avoid circuit conflicts for a simultaneous memory read and write operation even if employing single port memory bit cells. The read and write addresses of respective read and write operations are separately decoded into read and write row and column selects driven to a memory array so that simultaneous read and write operations are not affected by each other. To avoid a circuit conflict for a simultaneous read and write operation, the memory system is configured to prioritize a write row select over a read row select to drive a row of memory bit cells in the memory array. In this manner, that write operation will always be successful regardless of whether the read and write row select are to the same row.

[Continued on next page]

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